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Intel's 486SL Follows in 386SL's Footsteps

486DX Core With SMM, ISA Interface, and DRAM Memory Controller

By Michael Slater

Intel has unveiled the long-awaited 486SL, aiming to move the portable processor market to the 486 architecture. The 486SL, also known by the code name H4C, is based on a 486DX core that has been modified to add system management mode (SMM) and to provide fully static operation. In addition to the CPU core, the 486SL includes a DRAM controller and an ISA bus interface.

Figure 1 shows a block diagram for a 486SL-based CPU. The 486SL works with the 82360SL I/O chip, originally designed for use with the 386SL, which provides peripheral power management, timers, a real-time clock, interrupt and DMA control, two serial ports, and a parallel port. Intel says that pin limitations, not die-size barriers, kept the I/O functions off the 486SL.

Like the low-voltage version of the 386SL announced earlier this year, the 486SL is designed to operate in mixed-voltage systems. The on-chip logic always runs at 3.3V. Separate groups of power pins control the voltage for the bus and DRAM interfaces, allowing each to run at either 3.3V or 5V. (The ISA bus is currently specified only at 5V, but Intel is working with specific customers on 3.3V bus systems.) Intel is now shipping a 3.3V version of the 82360SL I/O chip to complement its 3.3V SL processors. Because of the limited availability of 3.3V DRAM and peripherals, most early 486SL systems will operate only the CPU core at 3.3V. As a next step, the DRAM will shift to 3.3V, and ultimately the ISA bus and peripherals will follow.

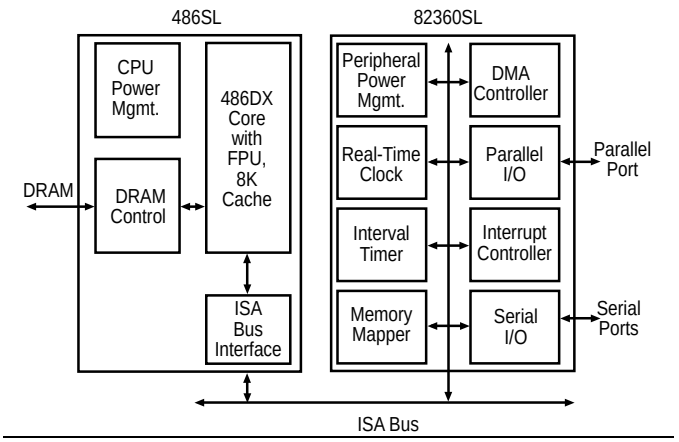

Figure 1. Block diagram of the 486SL CPU.

The 486SL is a natural successor to the 386SL, providing more than twice the performance with about half the power dissipation. (Power dissipation is about the same as the 3.3V 386SL, but all the 386SL systems in production today operate at 5V.) The only drawback, of course, is the price—a 25-MHz 486SL is priced at $269, while a 386SL at the same clock rate is only $86. The 386SL requires two external SRAMs for the cache (for maximum performance), but the total cost for these chips is under $15. Compared to the 486DX, however, the 486SL is a bargain—despite the fact that it includes everything on the 486DX and more, it is priced $48 lower than the 25-MHz 486DX.

The 486SL is available in the same 196-pin PQFP as the 386SL, but the pinout is different because the external cache RAM interface is eliminated and the width of the DRAM data bus is doubled to 32 bits. The 486SL is also offered in a smaller 208-pin SQFP (Slim Quad Flat Pack) that has a finer lead pitch. Even with the standard PQFP package, the total board space required is reduced (compared to the 386SL) because there is no need for external cache RAMs or an FPU (or FPU socket). The 486SL is also available in a 227-lead LGA (Land Grid Array).

Figure 2 shows Intel's estimate of the power reduction in moving from a 386SL system to a 486SL system. The power consumption of the 486SL itself is 940 mW typical for a system with a 3.3V DRAM interface and a 5V ISA bus. The power consumed by the display and other peripherals remains constant when switching from a 386SL to a 486SL, while the motherboard power drops 50% (assuming the best-case situation of 3.3V CPU, DRAM, VGA controller, and VGA memory). The net effect is a 25% reduction in "full-on" system power (com-

pared to a 5V 386SL system), resulting in a 25% increase in battery life from about 3 to 4 hours (or a 25% decrease in battery size if battery life is kept constant).

The figures above assume that no power-management features are active; the system is always in the full-on state. Intel projects that battery life under normal operation will increase even more, bringing the typical battery life from 8 hours up to 12 hours. The reason is that the faster processor will be idle more of the time, so the reduced-power states will be a larger fraction of the total time.

Like the 386SL, the 486SL provides a high-speed peripheral interface (PI) bus that uses the 16-bit data path of the ISA bus interface but with a separate set of control signals. This frees speed-critical peripherals, such as display controllers, from the antiquated timing constraints of the ISA bus. Intel expects PI-bus peripherals to be a significant part of 486SL system designs, since the ISA bus is a major bottleneck with a processor of this performance.

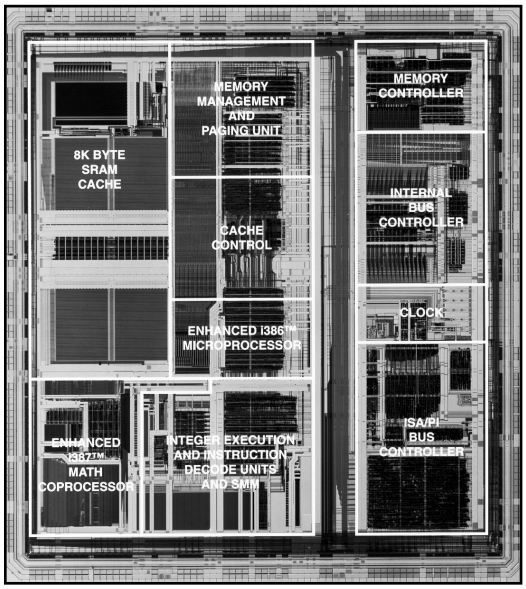

Figure 3. Intel's 486SL, which includes 1.4 million transistors on a 13.5 × 12.4 mm (532 × 488 mil) die.

Don't Confuse Cost and Price

As Figure 3 shows, the 486SL die looks very similar to a 486DX, but with an extra strip of logic on the right side. While the 386SL is fabricated in Intel's 1-micron, two-level-metal process, the 486SL will use the more advanced 0.8-micron, three-level-metal process that is used for the 50-MHz 486DX and the 486DX2 products. As a result of the more advanced process, the 1.4-million-transistor 486SL die is about the same size as the 850,000-transistor 386SL. (The 386SL is about 169 mm^2, compared to 167 mm^2 for the 486SL.)

The more revealing comparison, however, is with the 0.8-micron 486DX, which is a mere 82 mm^2—half the size of the 486SL. The large die size of the 486SL is due, in part, to a much larger pad ring that includes high-current drivers for the DRAM and ISA bus. This means that the production cost of the 486SL will be much higher than that of the 486DX. This is not reflected in the pricing, however.

While it makes no technical sense for the 486SL to cost less than the 486DX, there is a marketing reason: others will soon be making 486DX-compatible chips, and Intel hopes to move the thriving portable market to the 486SL, which is likely to remain proprietary to Intel. Intel has used the same approach with the 386SL, which is now priced below the 386SX even though it is a much larger die.

Competition from Within and Without

Systems based on the 386SL systems took much longer to reach the market than Intel expected, but the 486SL should have a quicker ramp. One key barrier faced by the 386SL was the difficulty of writing the BIOS code to exploit SMM; the 486SL should not suffer from this. While there are some initialization differences, the vast majority of 386SL BIOS code should be usable in 486SL systems. The key issue is simply price. With the 486SX selling for well under $100, the 486SL carries a stiff price premium for its additional capabilities. For users who don't care about floating-point, a 486SX combined with a $30 system-logic chip set provides a comparable solution at less than half the price of a 486SL and 82360SL. With AMD and Cyrix expected to have 486SX pin- and function-compatible chips on the market early next year, this is going to be a competitive market, and prices are sure to drop rapidly.

The advantage of the 486SL in this case is presumably its lower power consumption and SMM capabilities. While the 486SX is not offered by Intel in a static version, AMD's version will be static, as will Cyrix's offering. Both AMD and Cyrix are likely to offer some sort of system management mode. Intel already offers a 3.3V version of the 486SX and has hinted at plans for a static version with SMM.

Intel originally considered offering a version of the 486SL with the on-chip FPU disabled—*a la* the 486SX—but these plans have been dropped. It seems that such a

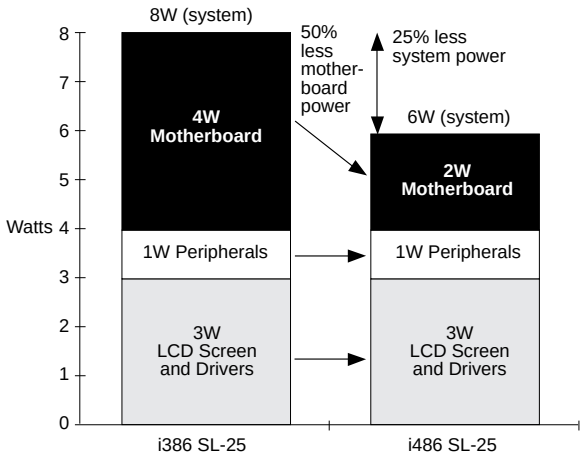

Figure 2. Power reduction from switch from 386SL to 486SL.

Price & Availability

The 25-MHz 486SL in the PQFP package is available now and is priced at $269 in thousands. A 33-MHz version, as well as LGA and SQFP package versions, will be sampled in December and in production in 1Q93; pricing has not been released. The 82360SL I/O chip is in production now in 5V and 3.3V versions; both are priced at $32 in thousands.

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part would give Intel a better competitive position against enhanced 486SX-type processors from Cyrix and AMD, but Intel can always introduce such a version if the competitive situation demands it. Intel may have been influenced by the market's response to the 486SX. Not only has the 486SX been widely (though unfairly) derided as if it were somehow a fraud because initial production used 486DX chips with a disabled FPU, but it has also encountered a lukewarm reception from system purchasers. Even though most users don't use applications that are sensitive to floating-point performance, many are willing to spend an extra few hundred dollars to be sure that they have the capabilities they may need in the future.

If Intel were to remain the only player in the 486 market, the 486SL would be assured of a dominant role in portable computers. The world has changed, however, and with AMD, Cyrix, and Texas Instruments in the picture—and possibly others before long—the 486SL is going to have to fight for its market share. The 486SX and compatible products will be strong competitors for users who don't require floating point. Other processor vendors may offer a more complete set of on-chip functions, such as a PCMCIA interface or a display controller. The fact that Intel is already pricing the relatively huge 486SL below the 486DX shows its determination to make this part a success, and while Intel may succeed, it will be with much lower profit margins that those to which it has been accustomed. ♦

