

Literature Watch

Buses

BTL transceivers enable high-speed bus designs. Joel Martinez, National Semiconductor Corporation; EDN, pg 107, 5 pgs.

SPARC chip sets provide Mbus expandability for high-performance SPARCstations. Ray Weiss; EDN, 8/6/92, pg. 65, 3 pgs.

Development Tools

Board level bus analysers for VMEbus and beyond. An outline of the uses of board level analysers for VMEbus and its extensions. Laurie J. Burger, Silicon Control; Microprocessors and Microsystems, v16 #3, 1992, pg 159, 4 pgs.

High-end simulation vendors with HDLs hear siren call of powerful PCs. The biggest breakthrough for simulators running on PCs is their ability to use hardware description languages (HDLs). William Twaddell; Pers. Eng. and Inst. News, 8/92, pg 24, 8 pgs.

DSPs

Real-time AC motor modeling with the TMS320C25 signal processor. Olli Vainio, Signal Processing Laboratory, Seppo J. Ovaska, KONE Elevators, Research Center, Micro-

processors and Microsystems, v16 #3, 1992, pg 125, 7 pgs.

Consumer applications: a driving force for high-level synthesis of signal-processing architectures. Rob Woudsma, Jef L. van Meerbergen; Philips Research Laboratories, IEEE Micro, 8/92, 20, 14 pgs.

To DSP or not to DSP: will a RISC chip do it better? M.R. Smith; The Computer Applications Journal, 8-9/92, pg 14, 12 pgs.

Graphics

Teleconferencing invades the desktop. Chip pair combines real-time video and computer graphics technologies for broadcast-quality PC displays. Milt Leonard; Electronic Design, 8/16/92, pg 47, 4 pgs.

Miscellaneous

Three-step method evaluates neural networks for your application. Jeannette Lawrence, Peter Andriola, California Scientific Software; EDN, 8/6/92, pg 93, 7 pgs.

CMOS technology trends and economics. Armin W. Wieder, Franz Neppi, Siemens AG; IEEE Micro, 8/92, pg 10, 10 pgs.

Processors

\$27 buys a 16-MHz embedded SPARClite microprocessor. Ray Weiss, EDN, 8/6/92, pg. 70, 2 pgs.

A comparison of three current superscalar designs. The designs studied are the Metaflow Lightning SPARC, the IBM RS/6000, and the Intel i960MM. Michael Laird, Clemson University, Computer Architecture News, 6/92, pg 14, 8 pgs.

Design and implementation of the 'Tiny RISC' microprocessor. The design and implementation of 'Tiny RISC' a 16-bit RISC-style microprocessor designed at UC Irvine. Arthur Abnous, Chnstopher Christensen, Jeffrey Gray, John Lenell, Andrew Naylor, and Nader Bagherzadeh, Department of Electrical and Computer Engineering, University of California, Irvine; Microprocessors and Microsystems, v16 #4-1992, pg187, 7 pgs.

Programmable Logic

Designing with programmable logic Charles R. Conkling, Jr.; The Computer Applications Journal, 8-9/92, pg 58, 10 pgs.