Most Significant Bits

Compaq, SCO Drop ACE Plans

Signaling the end of the ACE initiative as it was originally proposed, Compaq Computer and the Santa Cruz Operation have both backed away from their plans to develop ACE products. When the ACE initiative was conceived, Compaq was the leading supplier of IBM-compatible PCs, and thus gave ACE a PC-market presence. Since then, Compaq has fallen on hard times, and the company has been retrenching and cutting costs. The ACE program involved substantial R&D expenses for Compaq, while revenues were likely to be small for some time, making it hard to justify in Compaq's belt-tightening mode. Rod Canion's ouster from Compaq earlier this year was apparently a turning point in the company's commitment to building MIPS-based systems.

The Santa Cruz Operation's Open Desktop (ODT) was to be the standard UNIX for the ACE initiative, with SCO providing both Intel and MIPS versions. SCO's previous UNIX products have all been Intel-based, and while the company had ported some of its user-interface code to MIPS, the ODT on MIPS demonstrations that were given used MIPS Computers Systems' RISC/os kernel. ODT for MIPS was supposed to be based on OSF/1 technology provided to SCO by DEC, but this work has now been terminated, and SCO no longer plans to produce a MIPS-based version of ODT.

SCO's enthusiasm for MIPS has been waning for some time, and Compaq's withdrawal was the last straw. Most of the remaining ACE players have their own UNIX strategy based on a version of USL's SVR4, leaving SCO without many interested customers.

The loss of SCO's ODT, while probably less significant than the loss of Compaq, is symbolic of the failed aspirations of the ACE initiative. When the ACE initiative was announced, one of its key aspects from a UNIX perspective was the standardization on SCO's ODT, to which DEC, MIPS, and most other ACE proponents were promising to migrate. All ACE systems were to use the little-endian byte ordering, providing data compatibility with Intel-based systems, and the ODT environment (with all its APIs) was supposed to be identical for both Intel and MIPS platforms, making porting easy.

There were signs of trouble in achieving standardization on ODT and little-endian byte ordering from the start. A splinter group of ACE members, originally known as the Apache group, remained committed to USL's SVR4, using big-endian byte ordering. Univel, a joint venture of USL and Novell, was formed to provide a shrink-wrapped UNIX for both Intel and MIPS platforms, adding another option to the ACE UNIX assortment. To further confuse matters, DEC withdrew from its plan to use SCO's ODT, introducing its own OSF/1 implementation. The end result is an assortment of incompatible UNIXes that is no more cohesive than it would have been without ACE. Software developers still will have to provide several versions of their applications to support all major MIPS-based systems.

What remains of ACE is the ARC (Advanced RISC Computing) specification—the standard for MIPS-based systems that will run Microsoft's Windows NT as well as several flavors of UNIX. (See cover story for details on the first systems based on this specification.) As the first RISC platform for Microsoft Windows, this is a significant achievement-- despite the collapse of the overambitious initiative that surrounded it. Without some hardware standardization, MIPS-based systems would not have been a viable target for Windows.

A core group of companies—including MIPS/SGI, Acer, Olivetti, NEC, and Sony—remains committed to building ARC systems. ACE collapsed because it tried to accomplish too much; now it can focus on establishing ARC systems as a standard Windows NT platform, which has been the most meaningful element from the beginning but almost got lost among all the posturing and deal-making.

ARM Announces ARM600 Variant

ARM has announced the development of the ARM610, a cost-reduced version of the ARM600 that deletes the coprocessor interface to reduce die size and pin count. It is packaged in a 144-pin thin quad flat pack (TQFP). Both VLSI Technology and GEC Plessey have fabricated the part, but neither has formally announced it. VLSI expects to be in production this quarter. ARM will say only that it was designed in response to "customer input," but it seems clear that this part is destined for Apple's forthcoming "personal digital assistant" that will be produced in collaboration with Sharp.

SiS Offers EISA Chip Set

Taiwan-based fabless semiconductor vendor Silicon Integrated Systems is introducing its PC chip set products to the U.S. market. Founded in 1987, the company has been highly successful in their home market selling both chip sets and consumer-oriented devices such as ROMs. They have about 130 employees, and last year's revenues were $32M ($19M from chip sets). Their foundries are Toshiba, LSI Logic, and TSMC.

From their Sunnyvale office, they are offering AT-compatible chip sets for 386SX, 386DX, and 486 processors at speeds up to 50 MHz. Their most interesting product is a 486-based EISA chip set with support for a direct-mapped, second-level, copyback cache. The six-

chip SiS/EISA 486 solution supports paging, interleaving, and 2-1-1-1 bursts (i.e., the 486's maximum burst transfer rate). Priced aggressively at $60 in 10K-unit quantity, the chip set is sampling now and is scheduled for production availability in May.

Sun Announces "Silicon Product Program"

In an attempt to assure current and prospective makers of SPARC-compatible systems that key Sun technology will be made available in a timely fashion, Sun announced a formal commitment to making chips that it designs available to other manufacturers. In the past, Sun-designed processors, system-logic chip sets, and SBus interface chips have been offered through semiconductor vendors, so there doesn't appear to be much substance in Sun's announcement—for the most part, it is announcing something that has been going on for some time. Sun was no doubt motivated, in part, by a widespread perception than Sun's dominance of the SPARCstation market makes it difficult for other companies to compete.

Sun has said that it intends to make chips available to other manufacturers as soon as possible, no later than concurrently with the announcement of Sun products, and this *would* be a new development. Sun did not make its system-logic chip sets available for licensing until many months after it was shipping systems in volume, and this supposedly will not be repeated. Even if Sun is sincere in its intent to allow the chip suppliers to offer new chips to others in a timely fashion, however, the realities of the marketplace will often prevent others from getting chips at the same time as Sun.

The forthcoming SuperSPARC chip from Texas Instruments, for example, will initially be offered only to SPARC International executive members, with general-market availability lagging by several months. This is not due to any restrictions Sun has placed on TI, but to the simple fact that Sun will soak up every chip TI can produce for some time.

One new chip was revealed along with the licensing program: a stereo codec for audio I/O. While hardly part of Sun's core technology, it is nevertheless a potentially significant chip that could find applications in a variety of systems. (In fact, its first appearance was in the standard ARC system design from MIPS!) This chip has not yet appeared in a Sun product, but it is expected to be used in the SPARCstation 3, due to be announced later this month.

Sun codeveloped the chip with Analog Devices and Crystal Semiconductor, both of which will market it; Analog Devices calls it the AD1849, and Crystal calls it the CS4215. The 44-pin chip provides stereo (two-channel) A/D and D/A converters, each with 16 bits of resolution and sample rates of 4 to 48 kHz; programmable gain for the analog inputs; programmable attenuation for the analog outputs; on-chip smoothing and anti-aliasing filters; and a serial digital interface. It also offers 8-bit A-law or μ-law compression and expansion. Pricing is $30 in thousands, and production quantities are available now.

At the same time, NCR revealed that it is developing with Sun two highly integrated SBus I/O subsystem chips. One chip acts as an SBus master, and it includes a 7990-compatible Ethernet interface, a 53C90 SCSI interface, a parallel port, a DMA controller, counter/timers, an interrupt controller, and reset logic. The second device is an SBus slave, and it combines an 85C30-compatible dual-channel serial port, an 82077-compatible floppy disk controller, hardware cursor logic, and an 8-bit I/O bus for additional peripherals.

These two chips represent one of the first efforts to integrate workstation I/O functions, and they will slash the chip count of SPARC-based systems, reducing the entire I/O and peripheral controller subsystem to little more than two chips. Availability, pricing, and product details have not been released.

Backers Pull Plug on Tera

Tera Microsystems has become the first semiconductor company casualty of the SPARC market. After exhausting $6.8 million in venture capital, the company had not completed its SPARCstation chip set, and its investors declined to provide the additional funding needed. The company has ceased operation, and its technology is being offered for sale. Tera's design was focused on low cost, and its business plan was based on the emergence of a large market for Sun-compatible systems in which minimum cost would be crucial.

Tera did ship its basic two-chip set, but it ran into difficulty completing its microBUS-to-SBus interface chip. This left systems using Tera's chip set without any expansion capability, limiting its market.

Tera followed an unconventional design approach (see μPR 8/7/91, p. 1), using its own "microBUS" memory bus design instead of the standard MBus. Tera also integrated the cache RAM on the same chip as the cache controller, DRAM controller, and bus interface. This limited the cache size to 8K bytes, keeping the system from reaching its performance potential. Combined with the integration of cache and MMU functions in the chip set, the proprietary microBUS meant that Tera's chip set was limited to first-generation SPARC processors and lacked the flexibility of being able to work with any MBus processor module.

According to Henri Uehara, one of Tera's founders, the delay in completing the SBus interface chip was not the fatal problem; rather, it was the relatively small size of the Sun-compatible market that made it impossible to show the venture capitalists the kind of growth potential needed to justify continued investment. ♦