Literature Watch

Buses

Analyzers fine-tune high-performance buses. *As standard buses increase in number and complexity, bus analyzers have progressed from simple logic analyzers to specialized, protocol-specific machines.* Warren Andrews; Computer Design, 4/92, pg 75, 6 pgs.

Embedded PC bus standard gains ground. Warren Andrews; Computer Design, 4/92, pg 50, 2 pgs.

Streaming-data protocol extends IEEE-488 standard to 5 Mbytes/sec. Dan Strassberg; EDN, 3/30/92, pg 84, 2 pgs.

System cabling for the SCSI bus: past, present, and future.

The proposed SSBLT standard doubles the VME64 transfer rate. Jack Regula, Force Computers, Inc; IEEE Micro, 4/92, pg 64, 8 pgs.

Memory

A design and yield evaluation technique for wafer-scale memory. Koichi Yamashita, Shohei Ikehara, Fujitsu Laboratories Ltd.; Computer, 4/92, pg 19, 9 pgs.

DRAM/SRAM combo chip cures headaches. Dave Wilson; Computer Design, 4/92, pg 34, 2 pgs.

Memory-CPU interface speeds up data transfers *(Rambus).* Dave Bursky; Electronic Design, 3/19/92, pg 137, 5 pgs.

Miscellaneous

A glut of standards slows multimedia. *Blizzard of protocols and data formats frustrates cross-platform compatibility.* Lawrence Curran; Electronics, 3/92, pg 34, 2 pgs.

Fuzzy Logic is anything but fuzzy. Tom Williams; Computer Design, 4/92, pg 113, 13 pgs.

Level-3 PC-board connectors edge toward high-speed applications. *Decreasing semiconductor switching speeds need connectors as transmission lines.* Matt Sucheski, AMP Inc.; Electronic Design, 3/19/92, pg 97, 3 pgs.

Multimedia—here today, not tomorrow. Dave Wilson; Computer Design, 4/92, pg 56, 3 pgs.

Multimedia's new motto: partner to profit. *Consumer and computer companies are teaming up to deliver what neither can do alone.* Jack Shandle; Electronics, 3/92, pg 30, 3 pgs.

No end in sight to the notebook surge. *Price cuts and performance boosts mean 50% market growth this year for the tiniest PCs.* Lawrence Curran; Electronics, 3/92, pg 41, 2 pgs.

Prospects for WSI: a manufacturing perspective. <Wojciech Maly, Carnegie Mellon University; Computer, 4/92, pg 58, 8 pgs.

Wireless data links broaden LAN options. *Vendors and regulatory bodies confront limited-bandwidth and interface problems.* Milt Leonard; Electronic Design, 3/19/92, pg 51, 5 pgs.

Peripheral Chips

Chip makers take aim at multimedia market. Jack Shandle; Electronics, 3/92, pg 36, 1 pg.

Processors

Configuring a wafer-scale two-dimensional array of single-bit processors. *This overview of Europe's ELSA project shows how new hardware and software techniques can be used to achieve greater defect tolerance.* Ahmed Boubekeur, Jean-Luc Patry & Gabriele Saucier of Nat'l Polytechnic Inst.—Grenoble; and, Jaques Thrilhe of SGS-Thomson; Computer, 4/92, pg 29, 11 pgs.

Digital's Sun killer also rises. Dave Wilson; Computer Design, 4/92, pg 46, 3 pgs.

ICs: the brains of a workstation. *Fast central processors need a supporting team of complimentary chips, including graphics, I/O, and cache memory ICs.* Philip Koopman Jr., United Technologies Research Center; and Daniel Siewiorek, Carnegie Mellon University; IEEE Spectrum, 4/92, pg 52, 3 pgs.

Is RISC or DSP best for your application? *RISC processors have already kicked CISC out of more than a few embedded sockets. Now, DSPs are trying to prove they can be just as useful in embedded applications.* Dave Wilson; Computer Design, 4/92, pg 65, 6 pgs.

Organization of the Motorola 88110 superscalar RISC microprocessor. Keith Diefendorff, Michael Allen, Motorola Inc.; IEEE Micro, 4/92, pg 40, 24 pgs.

The Mips R4000 processor. Sunil Mirapuri, Michael Woodacre, and Nader Vasseghi, Mips Computer Systems; IEEE Micro, 4/92, pg 10, 13 pgs.

The message-driven processor: a multicomputer processing node with efficient mechanisms. William J. Dally, J.A. Stuart Fiske, J.S. Keen, R.A. Lethin, M.D. Noakes, & P.R. Nuth of MIT Artificial Intelligence Lab; R.E. Davison of Davison Des.& Dev. Corp; & G.A. Fyler of Intel; IEEE Micro, 4/92, pg 23, 17 pgs.

Third-generation RISC processors. *Mainframe and supercomputer design techniques are pushing the performance of third-generation RISC processors to 70 VAX MIPS and beyond.* Ray Weiss; EDN, 3/30/92, pg 96, 11 pgs.

Programmable Logic

FPGAs race for the gold in product development. *Gate arrays and standard-cell ASICs are still the big winners when it comes to product development, but FPGAs are closing in with competitive benefits such as flexibility, reduced cost and quicker time-to-market.* Barbara Tuck; Computer Design, 4/92, pg 88, 10 pgs.