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MIPS Announces First ARC Systems

R4000-Based Systems to be Sold by MIPS Through OEMs

By Michael Slater

MIPS Computer Systems has announced its first systems designed specifically to the ARC (Advanced RISC Computing) specification. The ARC specification, which is part of the ACE initiative, defines the required characteristics of MIPS-based desktop computers to establish a base-level target for software developers. A key goal of the ARC effort is to enable PC makers to add a MIPS-based system to their product line, exploiting as much of the existing PC infrastructure as possible and creating a high-volume platform for shrink-wrapped software.

Last November, MIPS announced its ARCSystem licensing program, enabling system makers to get into the ARC system business quickly by licensing a complete system design (called the ARCSystem 100) with the supporting ROM code, operating-system drivers, and ASICs. Some manufacturers will build this design as-is, and others will use it as a base for their own enhancements. The R4000 systems that have been shown by MIPS, Olivetti, and Acer are prototypes of the ARCSystem 100 design. Rumors are that the design has its roots in a Windows NT development platform created at Microsoft.

Now, MIPS has announced the "Magnum 4000," an OEM system based on the ARCSystem 100 design, and the "Millennium 4000," a deskside server version. Both are offered in versions with or without a 1-Mbyte secondary cache. As in the past, MIPS will sell its systems only through OEMs and VARs. MIPS currently has agreements with CDC, Tandem, and AT&T to market these systems.

Eventually, systems similar to these have the potential to compete in the mainstream PC market, but they are too expensive to do so today. Their target audience is not PC users, but UNIX and Windows NT software developers and traditional workstation users.

The entry-level model is the 40-SPECmark Magnum 4000 PC-50, which costs $9,990 (reseller list price) and includes a 15-inch, $1024 \times 768 \times 8$ color display, and 8 Mbytes of DRAM, but no disk. A version with a 200-Mbyte hard disk plus CD-ROM and floppy disk drives is available to software developers at a special price of $5995. To be a real contender in the mainstream PC market—putting aside the software issues—the normal retail price of this machine needs to drop well below the special developer price.

The desktop system with secondary cache lists for $14,990—a steep 50% premium over the entry-level model, keeping its price/performance about the same (since its SPECmark performance is about 50% higher). The deskside models are called the Millennium 4000 series; they use the same circuit boards as the desktop systems but in a larger box with a bigger power supply, and they cost $2,000 more.

Continued on page 6

In This Issue

MIPS ARC Systems

Continued from front page

In addition to offering the Magnum and Millennium systems as OEM products, MIPS will provide the circuit board design—for a hefty fee. The basic manufacturing package costs $500,000 (as prepaid royalties of $100 each for the first 5000 units), and it includes paper schematics, binaries for the ROM and HAL code, and Gerber tapes for the PC board. (HAL stands for Hardware Abstraction Layer; it is the set of I/O drivers and other low-level routines that creates a standard operating-system interface, hiding the specifics of individual hardware designs.) Source code for the software and the CAD database for the hardware (required if you want to make major modifications to the design) cost another $500,000. Royalties drop to $10 per system in high volume.

The MIPS systems are designed to run Windows NT, but this operating system isn't expected to ship in an end-user version until the end of this year at the earliest. For now, the primary operating system is MIPS' SVR4-compliant RISC/os 5.0 UNIX implementation. SCO has recently abandoned its plans to provide Open Desktop for the R4000, and it is now clear that there won't be one "standard" UNIX for ARC systems. DEC is continuing with its OSF/1 implementation, using the little-endian byte ordering, while essentially all the other MIPS system makers are using USL's SVR4 with the big-endian byte ordering. System makers can license the MIPS port of this operating system (RISC/os) now; by year-end, the USL/Novell joint venture, Univel, expects to offer a shrink-wrap version of SVR4 for MIPS machines. The Univel software may be offered in both big- and little-endian versions; the ARCSystem hardware is designed to support either. The goal—or perhaps it is a fantasy—of a single binary standard for MIPS-based UNIX applications remains as elusive as ever.

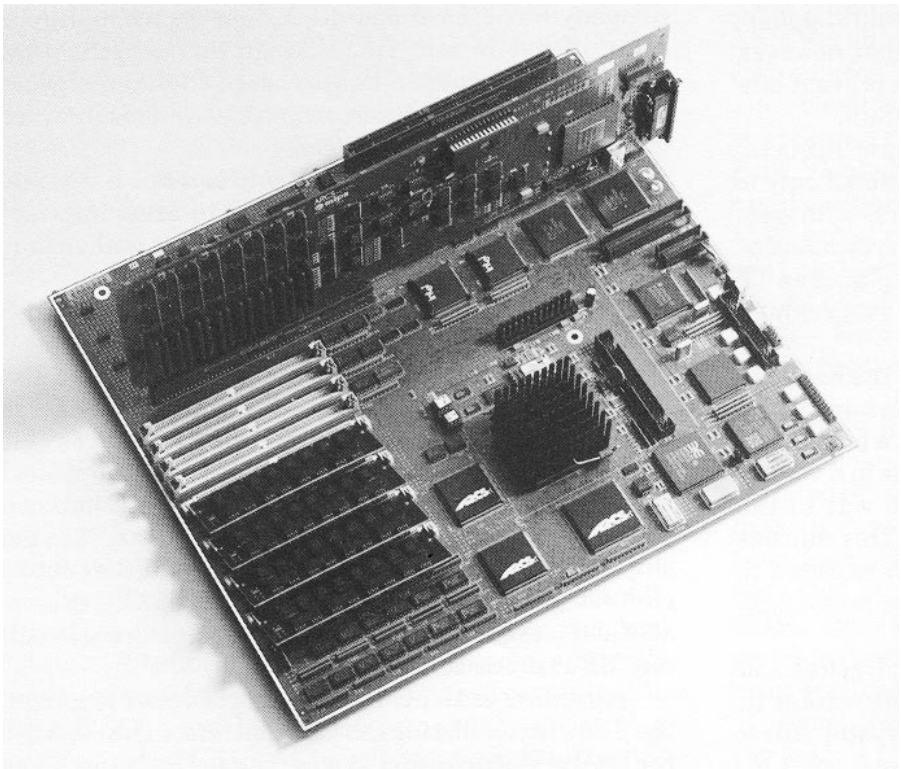

Figure 1. An ARCsystem 100/MIPS Magnum system board. The rear edge is to the right; the EISA connectors are mostly hidden behind the graphics card. The R4000 is in the center of the board with a finned heat sink.

System Design

Figure 1 shows a photo of the Magnum system board, and Figure 2 shows a block diagram of the ARCSystem 100/MIPS Magnum design. At the heart of the system are two MIPS-designed ASICs (the R4020 and R4030) that will be available from NEC and Toshiba. Currently, these chips are available only to licensees of the MIPS design package. By the end of this quarter, the two ASICs are supposed to become available as standard products from NEC and Toshiba, and anyone will be able to purchase them.

The system uses two R4020 data path controllers and one R4030 address path controller. This three-chip set provides interfaces for three buses: the R4000's native 64-bit address/data bus, a 128-bit (plus parity) DRAM data bus, and a 32-bit bus with 386-style timing. The 386-like bus serves as the interface for all I/O devices except the display controller, which shares a 64-bit data path from the DRAM bus. By using the 386 bus protocol, other devices designed to connect to a 386 (such as an EISA chip set or an Ethernet controller) can easily be interfaced.

The two ASICs are high-pin-count devices because they interface to three wide buses. The R4020 is a 25,000-gate chip and is packaged in a 208-pin PLCC; each chip provides half of the 64-bit data path required for the R4000. The 45,000-gate R4030 is in a 240-pin package, and it provides address buses for the DRAM, VRAM, and 386-like bus. The R4030 also includes most of the system control logic, including:

- Slave-mode R4000 bus interface
- DRAM controller
- 386-style master and slave bus interface
- I/O device control logic
- I/O logical to memory physical ad-

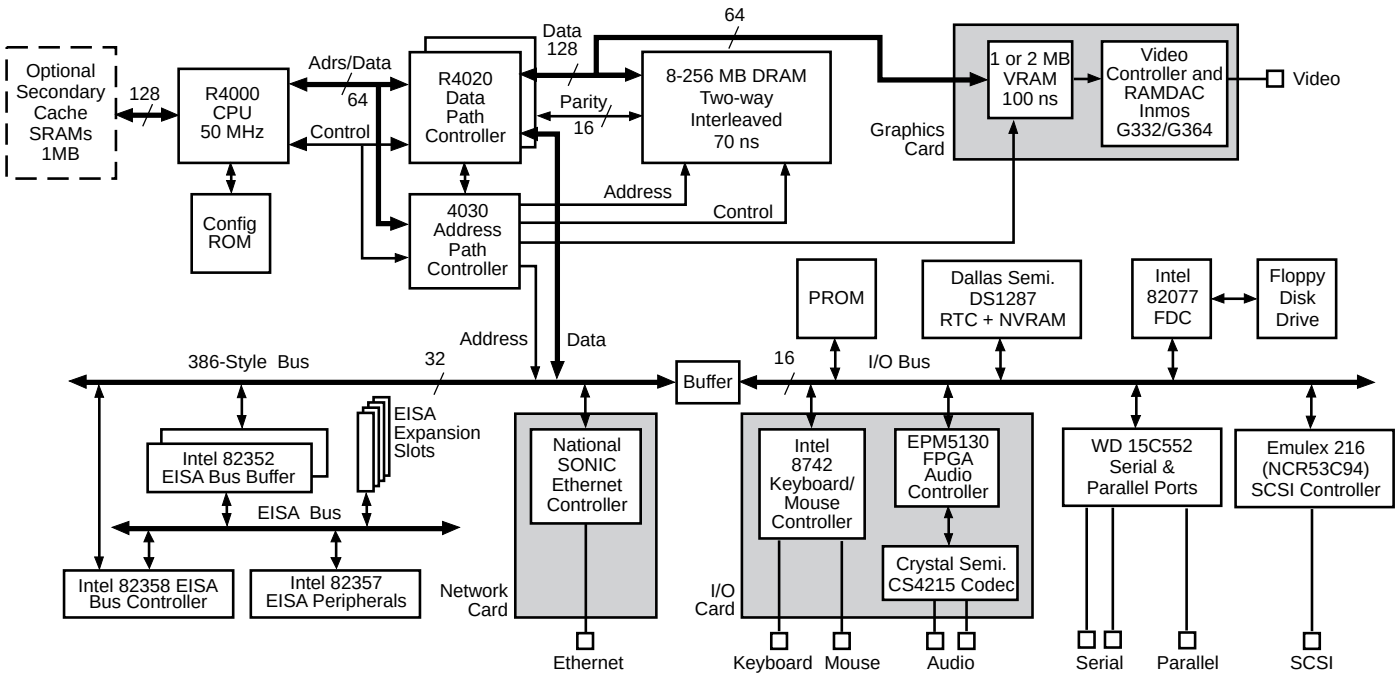

Figure 2. Block diagram of the ARCsystem 100/MIPS Magnum.

dress translation for DMA
- I/O cache controller and address tags for eight 32-byte blocks
- Video interface controller
- Interval counter
- 8-channel DMA controller

The DRAM interface provides two 64-bit data paths to support two-way-interleaved memory. MIPS rates the bandwidth at 94 Mbytes/s (32 bytes every 17 cycles) for block reads and 25 Mbytes/s for partial reads. For accesses to the EISA bus, burst-read bandwidth is 16.7 Mbytes/s and burst-write bandwidth is 33.3 Mbytes/s.

The board has eight SIMM slots, each 36 bits wide, and the system requires a minimum of four SIMMs to form two, 64-bit-wide banks (with parity). Standard memory configurations are 8 or 16 Mbytes using 1-Mbit chips and 32 or 64 Mbytes using 4-Mbit chips. Using 16-Mbit chips, the system will support 128 or 256 Mbytes.

The EISA interface uses Intel's EISA chip set, which connects to the emulated 386 bus provided by the R4020/R4030 chip set. The EISA interface requires four large chips, primarily because it must provide PC-style interrupt and DMA controllers as well as compatibility with several generations of PC bus protocols. EISA bus masters can take control of the R4030-generated 386-style bus for direct access to the system DRAM, VRAM, or peripherals.

Since the video, LAN, SCSI, audio, floppy, serial, and parallel interfaces are included on the system board (or on daughterboards), most users will have no need for the EISA interface, which adds roughly $100 to the component cost, and some low-end systems may eliminate it entirely. The ARC specification does not include any I/O bus in the basic system requirements. The spec includes appendices for both EISA and TurboChannel, but only DEC appears to be following the TurboChannel path. TurboChannel is both simpler and faster, and the interface is significantly less costly, but MIPS was swayed by the endless variety of add-in cards available for EISA (especially since all PC/AT cards can be used as well). This abundance of I/O cards may be illusory, however, because cards without an ARC version of their driver software—which is essentially all cards today—cannot easily be used in an ARC system.

The graphics card is available in two versions: one with 1 Mbyte of VRAM to provide 1024×768 resolution, and a higher-end model with 2 Mbytes of VRAM for 1280 × 1024 resolution. Both provide 8 bits per pixel. The 64-bit data path provides a high-bandwidth interface to the CPU. In principle, at least, a variety of different video cards can be implemented, including 24-bit-color and accelerated graphics controllers.

With the exception of the audio interface, the peripheral interfaces use common PC-type peripheral chips. The audio I/O interface uses the CS4215 codec from Crystal Semiconductor, which, ironically, was designed by Crystal in collaboration with Sun Microsystems. Control logic for the audio I/O interface is implemented in a 3000-gate EPM5130 Altera FPGA. The audio interface offers 8- or 16-bit resolution with samples rates from 8 to 44.1 kHz.

Processor		R4000PC	R4000SC	486DX	486DX2	486DX
Clock Rate (MHz)		50/100	50/100	33.3	25/50	50
External Cache		none	4M	256K	256K	256K
System		Magnum	*Simulated*	Intel	Intel	Intel
Integer	gcc	28.5	46.0	19.0	22.7	28.5
	espresso	40.6	53.9	16.7	23.5	25.0
	li	48.5	66.0	26.4	35.8	39.8
	eqntott	45.5	54.1	15.6	21.7	23.4
Floating Point	spice2g6	24.8	42.4	13.8	16.9	20.8
	doduc	35.7	49.4	8.1	11.5	12.2
	nasa7	42.0	55.5	14.0	17.1	21.1
	matrix300	172.1	277.8	19.2	25.1	29.1
	fpppp	32.6	54.7	9.8	13.2	14.7
	tomcatv	37.0	58.4	11.0	14.6	16.5
Geometric Means	SPECmark89	42.6	62.5	14.5	19.2	21.9
	SPECint89	30.0	54.5	19.0	25.4	28.5
	SPECfp89	44.5	68.5	12.2	15.9	18.3

Table 1. SPEC benchmark ratings for R4000 and 486 systems. The R4000 data is measured on the Magnum system for the PC versions, but as of press time MIPS was unwilling to release measured SPEC data for the secondary cache version. The Intel data is from Intel's 486DX2 benchmark report.

The ARCSystem is designed to use existing PC packaging. The system board is the same size as a standard PC/AT: 12.1" x 13.8". There are three separate I/O daughterboards in the system: the video controller, the LAN interface, and a "combo" card that provides the audio, keyboard, and mouse interfaces. The video is on a separate board so it can be easily changed. The LAN and other I/O functions were put on daughterboards primarily because it was the simplest way to provide the I/O connectors at the appropriate place for the vertical "slot" openings on the back of a standard PC enclosure. Of the 8 slots supported by a typical PC enclosure, the ARCSystem uses four for EISA connectors and three for the I/O daughterboards. The daughterboards are positioned like EISA add-in cards, but they have fewer pins and have customized, dedicated interfaces (e.g., 386-style bus for the LAN card, I/O bus for the I/O card).

Total power dissipation of the electronics is 55 W, of which the video accounts for 15 W.

Price and Performance

The driving force behind MIPS-based ACE systems has been the promise of two to three times the performance of an Intel-based system at the same price. In general, the claimed performance ratio is borne out by the SPEC results, depending on what one chooses as the basis of the comparison.

Table 1 shows the SPEC89 benchmark rating for the R4000 compared to the 486, and Figure 3 provides a graphical summary. On overall SPECmarks, the basic R4000 (with no second-level cache) provides twice the performance of the 50-MHz 486 and three times the 33-MHz 486. (The "clock doubler" 486DX-50, operating at 25 MHz externally and 50 MHz internally, is in-between the 486DX-33 and 486DX-50. We haven't included the 486DX2-66, since this part won't be available until later this year and thus should probably be compared to the 67-MHz R4000 to be fair.)

The R4000's performance edge over the 486 is highly variable from one benchmark to another, as the table shows. Comparing the integer-only results, the R4000PC is only 40% faster than the 486DX-50 and just over twice the performance of a 486DX-33. An R4000 with a second-level cache is 3.7 times the performance of a 486-50 on the floating-point portion of the SPEC suite.

In the PC market battle, what matters is how fast the system seems to a Windows NT user, and it remains to be seen how well this will correlate with the SPEC results. The high-bandwidth frame-buffer interface should produce a noticeably faster display than typical "SuperVGA" PC displays, and this performance gain is not represented in the SPEC ratings. High-end PCs are starting to use linearly addressed frame buffers connected to the processor's local bus, bringing their display performance closer to that of the ARC system, but such systems are likely to have only a 32-bit data path to the VRAM and are not yet part of the PC mainstream.

When a secondary cache is added to the R4000, performance jumps almost 50%. If this secondary cache adds a $5000 premium, however, as it does in the MIPS Magnum list pricing, then systems with second-level cache really aren't competitors to 486-based systems. Nearly all 486 systems include a second-level cache, which is much cheaper to add to a 486 than to an R4000. Cache-less R4000 systems will be competing against 486-based systems with cache.

Based on the MIPS Magnum diskless price of $10K, 486-based systems still have an enormous price advantage over ARC systems. If you compare the Magnum with an IBM or Compaq 486 machine with comparable display, I/O, and memory systems, the prices would be in the same ballpark. The vast majority of the volume in the PC market, however, is at much lower price points, due to a combination of less-capable typical configurations (AT bus instead of EISA, smaller memory, lower-resolution display) and lower profit margins.

As an example of what it takes to compete with the PC clone market, a glance at the San Jose Mercury News shows several dealers advertising 486-33 systems with 1024 × 768 color displays, 120+ Mbyte hard disk drives, and 1 Mbyte of DRAM for under $1800.

Even adding another $1500 for 8 Mbytes of RAM, audio I/O, and an Ethernet adapter, a comparably equipped 486 system sells for well under half the list price of the MIPS Magnum—without a disk drive. ARC system prices will drop over the next 18 months as multiple vendors begin shipping systems, but they have a long way to go to meet PC pricing head-on.

Much of the system price difference in the example above can be traced to the relatively high profit margins and lack of high-volume efficiencies in the workstation market. Looking at component costs rather than system price, 486-based and R4000-based systems aren't too far apart for equivalent configurations. Referring back to Figure 1, only the CPU/cache/DRAM complex at the upper left changes for a 486-based system. The R4000 processor itself is considerably more expensive than a 486, and it is not yet clear how far the $1000 sample prices for R4000 chips will fall when they reach mass production; estimates range from $300 to $600 in 1993. A 33-MHz 486DX sells for $406 today in quantities of 1,000, and the 50-MHz version is $570. As the R4000 price drops, the 486 price is likely to stay well below the R4000, but future cost-reduced versions of the R4000 (see below) could reverse this relationship.

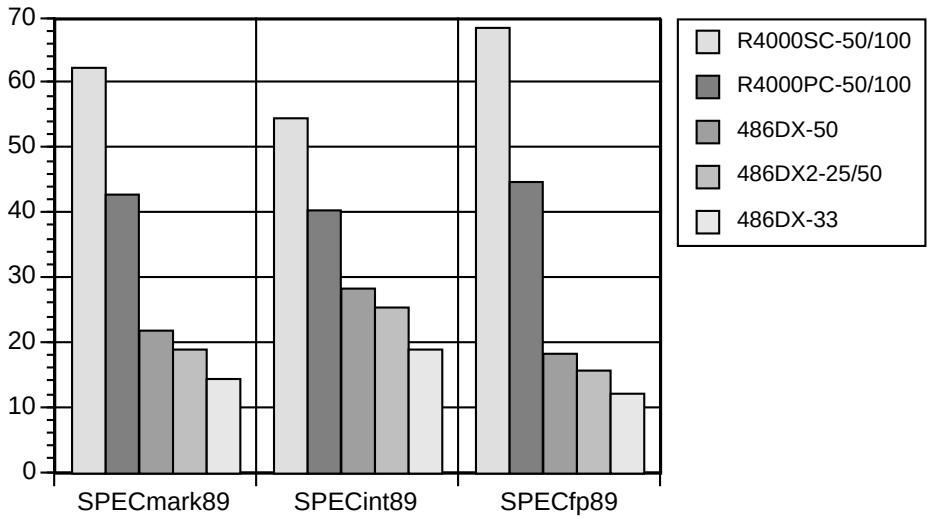

Figure 3. SPECmark performance for R4000 and 486 systems.

The 486 system has a number of cost advantages (and performance disadvantages) beyond the processor itself. It is likely to use a 32-bit-wide memory system, rather than 128; it has a 32-bit processor data bus, instead of 64; and its bus interface functions are much simpler. As a result, the bus interface and memory control logic for a 486-based system fits in smaller packages and uses smaller chips.

Another factor in the comparison is the minimum system configuration. The minimum ARCSystem 100 has 8 Mbytes of RAM, which is a high-end configuration for the PC market. As Windows continues to displace DOS as the mainstream PC environment, however, typical PC configurations will creep up to 8 Mbytes, and with 16-Mbit chips moving into production, the cost premium for 8 Mbytes over 2 or 4 Mbytes will shrink. Even today, 8 Mbytes of RAM at retail costs less than $300. Furthermore, using Windows NT on a 486 will require the same 8-Mbytes of memory, so when comparable operating-system environments are compared, Intel- and MIPS-based systems are on equal footing with regard to the high minimum memory size.

Futures

These price and performance comparisons are, of course, only snapshots in time. By the end of this year, Intel should be shipping the P5 and the MIPS partners plan to be shipping 67- and 75-MHz R4000s and R4000As. (See µPR 4/15/92, p. 11 for the MIPS processor roadmap.) It remains to be seen when each of these devices will be ready for volume production and how their prices will compare—both are sure to be at the high end of the microprocessor price spectrum, and it will be surprising if the P5 is not considerably more expensive than the R4000. Intel has consistently positioned its P5 as being slightly faster than the 50-MHz R4000. The 75-MHz R4000A, with a 50% higher clock rate and twice the cache size of the original R4000, should be considerably faster than the P5—although the P5 is also sure to move up in frequency over the course of 1993.

Separately from the high-end battle, which will be taken over by the R4000A and the R5000 as Intel approaches the release of the P6, a potentially much more important arena is low-cost, low-power derivatives of the R4000. At least two such designs are underway. QED, a startup staffed with senior MIPS chip designers, is working under contract to IDT to create one low-power version; this device will be manufactured by IDT, Siemens, and Toshiba as part of their collaborative agreements. Another low-power design is underway at MIPS, under contract to NEC, for a design code-named VRX that initially will be sold by NEC and later licensed to MIPS' other semiconductor partners. These devices promise near-P5 performance (based on projections from Intel and MIPS) at 386 prices, but they won't ship until the second half of 1993.

Continued on page 21

Viewing the embedded control market as a single large market open to any microprocessor would be the same mistake as viewing the microprocessor-as-a-CPU market as a single entity. The embedded control market may be open to any-architecture, but it isn't open to any microprocessor. For the convenience of this discussion, I'll divide the embedded control market into two segments: commodity and boutique. The commodity market segment is characterized by very low margins, very low average selling prices, and very high volumes. The commodity market is over a billion units. To compete in the commodity market, you must have an excellent custom design and high-volume manufacturing capability. The boutique market segment is everything else and represents approximately zero percent of the embedded control market.

The current SPARC and MIPS designs, even in their embedded control costumes, don't qualify to compete in the commodity segment of the embedded control market. Still, the boutique segment of the embedded control market is millions of units and has more opportunity than the high-end any-architecture segment of the CPU market. But here the SPARC and MIPS chips, designed for the high-end any-architecture CPU market where performance is king and cost and power are secondary, are being adapted to compete in the embedded control market, where cost, function, and power consumption are often more important than raw performance. Motorola, National, AMD, Intel, and others design microprocessors for specific segments of the embedded control market. I doubt they view competition from adapted SPARC and MIPS designs with much trepidation. Further, prices for embedded control microprocessors don't have the advantage of the artificially inflated price floor characteristic of the CPU market (supported by the high profit margins Intel is able to command) to help amortize development costs. It's a tough market for SPARC and MIPS; even if they sell in the boutique segment of the embedded control market, these designs will never make the transition to the commodity segment.

There's one more market opportunity to look at: the low-power segment of the CPU market. The pen-based notebook computer market may be substantial someday, but the architecture window is probably closing with the three candidates being ARM, Hobbit, and the x86. For this market, power dissipation is king and everything else is secondary. The current SPARC and MIPS designs don't qualify to enter this segment, but at least they are not yet locked out.

The situation looks bleak, but I'm impressed: these companies are trying everything they can and I don't hear any blubbering and complaining. At least they are going to die like men in the grand tradition of fighter pilots. ♦

MIPS ARCsystems

Continued from page 9

Conclusions

These first-generation ARC systems should be competitive in the workstation market, but other than serving as software development vehicles, they have little to do with the PC business because of their high prices and lack of appropriate application software. It is a shame that MIPS didn't price the systems more aggressively, but the company can't afford to buy market share.

In the next two years , MIPS should finally be able to reach mainstream PC price points while offering significantly higher performance. By then, of course, there will be a half dozen or more makers of x86-compatible microprocessors, and it is hard to know just what the QED and VRX chips will be up against. At a minimum, they will have to compete with 486-based systems at the low end and P5-based systems at the high end—not to mention SPARC-based systems and the other RISC competitors.

So far, only Acer, Olivetti, and a start-up called Carrera Computers (Laguna Hills, CA) have been announced as ARCSystem licensees. Of the 90 system vendors that ACE claims to have in its camp, few have demonstrated any level of commitment to building ARC systems. Just as with SPARC-based systems, there is a promise of numerous PC makers manufacturing ARC systems, creating a competitive market for binary-compatible RISC workstations. So far, more companies have failed than have succeeded trying to do this with SPARCstations, and few have achieved a volume of even a thousand units a month—tiny by the standards of the PC market.

At the moment, there are few companies with a demonstrated, serious commitment to making ARC systems, and it remains to be seen whether or not it will reach critical mass as a standard. Compaq's recent decision to shelve its ACE plans leaves the initiative without a first-tier PC maker, and DEC's religious pursuit of Alpha has raised serious questions about its commitment to MIPS-based systems. SGI's proposed purchase of MIPS further clouds the issue, though it seems that this is the least of ACE's problems.

While it seems very unlikely that ARC systems will ever become a dominant standard, it is too early to count it out as one of the top few survivors of the early 1990s. While ACE has largely collapsed, its core—a standard for MIPS-based systems that will run Windows NT as well as UNIX—is progressing reasonably. There won't be any quick victories in the battles to take some of Intel's market share, but there will probably be some slow, hard-fought successes, and MIPS, SPARC, and PowerPC remain the top contenders. ♦