Most Significant Bits

386 Prices Fall

As promised, Intel has slashed its 386 prices effective April 1, and AMD has responded in turn. Intel cut its 386DX-25 price over 30%, from $150 to $104, and it also introduced a plastic-packaged version for $99. Intel's 386DX-33 price dropped 34%, from $190 to $125, with the new plastic version priced at $119. (The table below shows the complete price matrix for all vendors.)

Intel's 386SX-16 price dropped only 16%, from $56 to $49, but its 386SX-20 price was cut 28%, from $82.50 to $59. Intel's 386SL prices were reduced similarly. The cuts get smaller as the performance level increases; the 486SX-16 was cut 19%, but the 20- and 25-MHz versions were reduced only about 10%. The 486DX-33, which is probably Intel's profit leader and has no direct competition yet, was trimmed by only 2.6%, from $417 to $406. Look for 486DX prices to follow the 386 price trend later this year, as AMD and Cyrix begin shipping competitive chips and Intel rolls out the P5.

Processor	Clock (MHz)	Package	Voltage	Intel	AMD	C&T ('00/'05)	Cyrix
386SX	16	PQFP	5 V	$49	—	$52/$60	—
	20	PQFP	5 V	$59	$59	$63/$72	—
	25	PQFP	5 V	$78.50	$59	$68/$78	—
		PQFP	3.3 V	—	$69	—	—
	33	PQFP	5 V	—	$69	—	—
386SL	20	PQFP	5 V	$101	—	—	—
	20-no cache	PQFP	5 V	$84	—	—	—
	25	PQFP	5 V	$122	—	—	—
386DX	20	PQFP	5 V	$99	$101	$98/$113	—
	25	PGA	5 V	$104	$101	$112/$129	—
		PQFP	5 V	$99	$94	$103/$119	—
			3.3 V	—	$101	—	—
	33	PGA	5 V	$125	$101	$128/$147	—
		PQFP	5 V	$119	$101	$119/$137	—
	40	PGA	5 V	—	$116	$149/$172	—
		PQFP	5 V	—	$101	—	—
486SLC	20	PQFP	3 V	—	—	—	$119
	25	PQFP	5 V	—	—	—	$119
		PQFP	3 V	—	—	—	$135
486SX	16	PGA	5 V	$163	—	—	—
		PQFP	5 V	$144	—	—	—
			3.3 V	$174	—	—	—
	20	PGA	5 V	$213	—	—	—
		PQFP	5 V	$201	—	—	—
			3.3 V	$243	—	—	—
	25	PGA	5 V	$293	—	—	—
		PQFP	5 V	$282	—	—	—
			3.3 V	$341	—	—	—
486DX	25/33	PGA	5 V	$406	—	—	—
	50	PGA	5 V	$570	—	—	—
486DX2	50	PGA	5 V	$517	—	—	—

Thousand-piece, second-quarter '92 pricing for the full spectrum of 386/486-architecture microprocessors. Note that while AMD's chips have identical performance to Intel's on a clock-by-clock basis, C&T's are offered in the 38600 version that is claimed to be 10% faster and a 38605 version that is claimed to be 40–50% faster, at the same clock rate. Cyrix's 486SLC is pin-compatible with the 386SX but is claimed to be 20–60% faster at the same clock rate.

AMD followed Intel's lead and has undercut Intel at almost every price point. AMD is offering its 40-MHz version for the same price as its 33-MHz part—$101. C&T is maintaining a price premium over Intel's parts, since it offers higher performance at the same clock rate, but negotiated volume prices are likely to be at or below Intel's level.

Intel Announces Its First 3.3-V Processors

In coordination with the 486DX2 rollout, Intel announced 3.3-V versions of the 486SX. The low-voltage versions carry a price premium of about 20% over the standard version. Intel is offering samples now and promising production for July. A 3.3-V version of the 486DX will be offered in the second half of the year. Versions of the 386SL specified for 3.3-V operation are on approximately the same schedule as the 486SX, but have not been announced; it appears that Intel accelerated the 486SX 3.3-V announcement to take advantage of the 486DX2 event.

AMD announced 3.3-V versions of its processors last fall, claiming a substantial lead over Intel. It now appears that both companies will be in production at about the same time, and availability of DRAMs and other system components specified for the lower supply voltage will remain in the critical path. By year-end, however, the shift to 3.3-V systems for portables should begin in earnest, resulting in a substantial increase in battery life.

Toshiba Reveals RDRAM, Sync DRAM Plans

Toshiba announced that it will begin sampling a 4-Mbit Rambus DRAM (RDRAM) in October of this year, with a 16-Mbit device to follow in 1993. (See µPR 3/4/92, p. 15 for details on Rambus.) Toshiba also made the first announcement of a synchronous DRAM, which is another device aimed at increasing memory bandwidth. A JEDEC committee has been working on a synchronous DRAM standard, which is not yet final, and several vendors are expected to produce the devices. Toshiba plans to sample a 16-Mbit synchronous DRAM in October 1993.

Synchronous DRAMs (SDRAMs) replace the asynchronous RAS/CAS interface with a synchronous interface. The row address is clocked in on one cycle, and successive column addresses can be clocked in on successive cycles; column access is

pipelined, so one access does not need to complete before another can begin. The RAM is divided internally into two banks, allowing internal interleaving. An 8-bit-wide interface combined with a 100-MHz clock results in a 100 Mbyte/s maximum transfer rate; initial latency is six clock cycles, or 60 ns.

RDRAMs, in contrast, have a longer initial latency but five times as much bandwidth (500 Mbytes/s). RDRAMs have an advantage in small systems, since their packet-oriented bus allows a single RDRAM (or a few RDRAMs) to serve as the entire memory system; multiple chips are not needed to achieve a 32-bit or wider word size. SDRAMs, on the other hand, will typically be used in larger systems with wide memory banks, enabling them to achieve higher bandwidth than a system with a single Rambus.

AMD 29005 Used in Apple Laser Printer

AMD has scored a major design win for its 29000 microprocessor in Apple's new Personal LaserWriter NTR. This $2195 printer replaces the Personal LaserWriter NT, which had a 68020-based controller, and it is likely to be Apple's highest-volume printer. The printer uses the same 4-ppm Canon engine as its predecessor, and it includes Adobe's PostScript Level 2 as well as HP LaserJet IIP emulation. Apple calls the printer "five times faster" than the NT, but real-world speed improvements are likely to be somewhat less. It also includes, for the first time in an Apple printer, a parallel port—a concession to the PC world. Apple is marketing the printer for PCs as well as for Macintoshes.

This is Apple's first use of a non-68000-family processor in its laser printers. Apple already uses the 29000 in its 8•24GC accelerated graphics card, but the printer has a much greater volume potential. Hewlett-Packard also uses the 29000, but only in its high-end LaserJet IIIsi. HP ships about 50% of all laser printers, so they are a critical design win; all of HP's mainstream printers are still 68000-family-based.

It is interesting to note that the Apple design uses the slowest of all 29000 processors—the 16-MHz 29005, which is a 29000 whose branch target cache and MMU are not functional. HP's LaserJet IIIsi actually runs its 29000 processor at 12 MHz, even though the slowest chip on AMD's price list is 16 MHz. For the mainstream laser-printer market, it seems that RISCs need lower prices, rather than higher performance.

HP Forms PA-RISC Support Organization

Hewlett Packard has announced the formation of PRO, the Precision RISC Organization, to promote the PA-RISC architecture and coordinate activities among the companies using it. The founding companies are HP, Convex Computer, Hitachi, Hughes Aircraft, Mitsubishi Electric, Oki Electric Industry, Prime Computer, Sequoia Systems, and Yokagawa Electric.

Both Hitachi and Oki are licensed to make PA-RISC chips and are developing embedded control PA-RISC chips due in 1993. Hitachi is also developing a processor for high-end workstations as well as a family of workstations and multiuser systems. Samsung (a PA-RISC licensee but not a PRO member) and Mitsubishi are planning to make or remarket PA-RISC systems, but they are not currently developing processor chips for the merchant market.

HP has close relationships with system makers Sequoia Systems and Convex Computer. HP is codeveloping a fault-tolerant PA-RISC system with Sequoia, and PA-RISC recently ousted the MIPS R4000 from a massively parallel supercomputer under development at Convex. (HP also made an equity investment in Convex.) Yokagawa Electric will develop industrial automation products using PA-RISC, Prime Computer will resell HP's servers and port some of its software to PA-RISC, and Hughes Aircraft will make Tempest versions of HP's systems for the military.

PRO joins ACE, SPARC International, and 88open as RISC architecture booster organizations. (In addition, IBM, Motorola, and Apple are expected to launch an organization for the PowerPC architecture.) All of these enterprises have one thing in common—the desire to foster the common interests of multiple companies (which are often competitors) using a particular microprocessor architecture. Like the other three organizations, PRO plans to establish hardware and software standards, establish an API and an ABI for "shrink wrapped" software, and license a trademark "seal of approval" for compliant products. PRO will also perform compliance testing for hardware and software.

Beyond these similarities, however, each organization is very different. Because of HP's more cautious approach and its decision to open up its architecture relatively late in the game, HP has had to take a different approach to establishing a standard. Rather than signing up half-a-dozen semiconductor companies and scores of system vendors to battle it out in the marketplace, HP has quietly built a small web of partners with little competition among themselves. While HP has signed up semiconductor licensees, it has not offered its leading-edge "Snakes" or PA-7100 chips through them. HP is, however, making these chips available to its partners, including Sequoia Systems and Convex Computer, in chip and module form.

HP has been constrained in its ability to offer its Snakes chip set because of limited supplies of the FPU chip, which is manufactured by TI. The high clock rates also require special circuit-board design techniques, and HP was not prepared to support chip-level customers. With the emergence of the 7100 chip, however, HP has been seeking a partner to supply and support it for the merchant market. ♦