MIPS Lays Out R4000 Roadmap

By Michael Slater

In a bid to keep up with its competitors in the microprocessor "airwars," MIPS has revealed its plans for the next two generations of R4000 microprocessors. The roadmap includes speed upgrades, cache size increases, a high-end version with branch prediction, and a low-cost, low-power version, all due to sample by the end of next year.

The first upgrade to appear will be a 67-MHz (133 MHz internal) version of the existing R4000 design, which will begin shipping in the third quarter. At least some of the R4000 vendors have sufficient yield from the existing design to select parts for this clock rate without requiring any redesign or a chip "shrink." NEC is also expected to ship a 75-MHz version using its own shrink of the current design.

MIPS is currently modifying the R4000 design to double the cache size to 16K bytes each for instructions and data (32K total) and to trim critical speed paths. Tape-out of this device, called the R4000A, is scheduled for the third quarter, with samples late in the year and production early in 1993. Fabricated in 0.6-micron CMOS, performance is projected to be close to 100 SPECmarks with a 75-MHz (150 MHz internal) clock.

The next-generation part, which will carry the R5000 designation and will be fabricated in a 0.45-micron process, will double the cache sizes again to 64K total and add branch prediction. No major changes to the pipeline or instruction-dispatch capabilities are planned. The R5000 is expected to run at 100 MHz (200 MHz internal) and performance is projected to be 130–150 SPECmarks. This part is currently in the final definition stages, and samples are expected in the second half of 1993. The R5000 should be performance-competitive with the 21064 Alpha chip and HP's PA-7100, but it appears to be about 18 months behind in its production schedule.

A team of 15 to 18 people is already at work on the generation beyond the R5000, code-named the T5 (and sometimes referred to as the R10000), which will be a completely new microarchitecture and will also add some instruction-set enhancements. In particular, a multiply-add instruction is expected to be included, as well as superscalar issue capabilities. Production is planned for early 1995 using a 0.35-micron process. The processor is expected to sustain more than two instructions per clock cycle at a "250+ MHz" clock rate.

Independently of the R5000 and T5 projects, another high-end processor code-named "TFP" is being developed by SGI, in collaboration with Toshiba, with an emphasis on floating-point performance. No details have been made available, other than the claim that it will offer "Cray YMP-like" performance and be sampled in 1993. Like the T5, it will be a superscalar design and will include some instruction-set extensions.

While the evolution described above is focused on performance, a separate team is developing a new implementation, code-named VRX, which will not support secondary cache or multiprocessor configurations. (The existing R4000PC does not support these capabilities either, but this is just a packaging option; the chip includes all the logic for these functions.) The VRX project is being funded by NEC, with MIPS engineers performing much of the design work under contract. NEC has a one-year exclusive on making the device, but it eventually will be multiple-sourced.

The VRX will provide an R4000-compatible bus interface so it can exploit system-logic chip sets being developed for the current R4000. The instruction cache will be doubled to 16K, but the data cache will probably stay at 8K. The FPU is being redesigned to reduce die size, and FP latencies will be somewhat longer. Power consumption is expected to be less than 2 W with an 80/160-MHz clock rate, and suspend/resume support will be included. NEC's target price is under $50 in high volume, with production in the second half of 1993 using 0.45-micron process technology.

Although its existence has not yet been formally disclosed, another series of R4000 derivatives aimed at low-cost, low-power desktop and portable systems is under development at QED. QED was started last year by several senior designers who left MIPS, including Earl Killian, Tom Riorden, and Ray Kunita. QED is working under contract to IDT, which expects to begin sampling designs from QED during the second half of 1993, with volume production in early '94. Operating with a 50-MHz external clock, the chip is expected to consume less than 2 W and deliver over 60 SPECmarks using an internal clock rate of "more than twice" the external rate. Caches will be "significantly larger" than for the original R4000, but the die size is claimed to be less than half that of the R4000 in equivalent process technology. IDT has partnerships with Siemens and Toshiba, who will both supply the part, and it is rumored that Toshiba—a bitter competitor of NEC's—has heavily backed the QED project.

The VRX and QED designs are key to MIPS' future in the ACE initiative, at least in terms of being a volume alternative to x86-based systems. These chips promise to deliver P5-class performance at prices that are suitable for the high-volume segment of the PC market. Whether or not the software side of the equation will be there as well, however, remains more of an unknown. ♦