6x86/PENTIUM™ (P54C) BUS INTERFACE DIFFERENCES

REVISION 2.3

Revision History

No.	Release Date	Description of Changes
1.2	11/1/93	Eliminated unnecessary pull-ups/pull-downs from Table 2-3. Deleted '3.5 Cache Inquiry Cycles'. Modified description of SMM differences. Additional minor changes including correcting title of document.
1.3	12/15/93	Deleted single cycle bus operations.
1.4	2/11/94	Update misaligned accesses that cross 64-bit boundary.
1.5	3/25/94	Update for 296 PGA pinout. Added burst order differences.
1.6	4/11/94	Changed pin Y35 from NC to *reserved*.
1.7	5/2/94	Added requirement for "1+4" burst mode compatibility. All bytes supplied to the CPU during the "1" read must be valid if KEN#=0 for that cycle.
1.8	6/17/94	Updates to reflect changes in APICEN active level and recommendations for common socket pin Z34.
1.9	8/31/94	Updated definition of pins W35, X34 and Y33 in table 2-3.
2.0	9/19/94	Updated pin Y33 (CLKMUL) common socket implementation.
2.1	11/22/94	Changed 'PRDY#' to 'PRDY'.
2.2	1/3/95	Modified SMM description to remove MMAC functionality.
2.3	5/3/95	Clarifications in Table 2-3.

1. Overview

This document discusses the 6x86/Pentium™ (P54C) bus interface differences and a common socket specification for a single processor system. The bus interface differences include the functional differences in the bus protocol and the physical differences in the pinout between the two parts. The common socket specification is a physical interface specification for a 296-pin PGA socket that is capable of hosting either the Cyrix 6x86 or Intel Pentium processor. This specification is intended to be a guideline to eliminate conflicts due to pinout differences and does not address register or electrical (AC/DC) differences that may exist.

For additional 6x86 information, please refer to the 6x86 Bus Interface Specification or contact Cyrix Corporation. Information in this document is subject to change without notification. All Pentium information is available in the Pentium Processor User's Manual and the Pentium Processor 90/100MHz data sheet. Any functions not disclosed in the referenced manual are NOT covered by the scope of this discussion.

2. Pin Differences

Table 2-1 lists the Pentium pins that are not supported on the 6x86. Table 2-2 lists the 6x86 pins that are not supported on the Pentium.

Table 2-1. Pentium Pins Not Supported on 6x86

Pin Name	Pin Function
[BF]	Bus Frequency Select
BP(3:2), BP/PM(1:0)	Breakpoint, Performance Monitor Outputs
CPUTYP	CPU Type Indicator
D/P#	Dual/Primary Processor Indicator
FRCMC#, IERR#, PEN#, BUSCHK#	Data Integrity, Error Checking
LINT1 (NMI)*, LINT0 (INTR)*	Local Interrupt (0:1)
PHIT#, PHITM#, PBGNT#, PBREQ#	Interprocessor signals for dual processor implementation
PICCLK, PICD0 [DPEN#], PICD1 [APICEN]	APIC Interface Signals and Dual Processor Enable
PRDY	Probe Ready
R/S#	Run/Stop Control
STPCLK#	Stop Clock Request

* The NMI and INTR functions of these pins are supported on the 6x86.

Table 2-2. 6x86 Pins Not Supported on Pentium

Pin Name	Pin Function
BHOLD, DHOLD, LBA#, QDUMP#	Scatter/Gather Interface Pins
PMON0, PMON1, PMC	Performance Monitor Outputs
SUSP#, SUSPA#	Suspend Mode Control
CLKMUL	Core/Bus Clock Frequency Ratio Control
TEST	Test Control Input
Reserved	Reserved for future use.

Table 2-3 lists the 6x86/Pentium 296-pin PGA pinout differences. In addition, the common socket column indicates the recommended state of the pins for a socket that supports both the 6x86 and Pentium. For a common socket implementation, the listed pins should not be connected to any signal and should be either pulled high, pulled low or left unconnected as shown in the table.

It may be possible to implement a variation of the common socket that supports a specific feature, such as a socket supporting 6x86 suspend (SUSP#, SUSPA#). Care must be taken when implementing common socket variations to eliminate pinout conflicts and ensure proper system operation.

Table 2-3. 6x86/Pentium Pinout Differences

Pin Location	6x86 Pin Definition	Pentium Pin Definition	Common socket Implementation	6x86 Internal pull-up/pull-down
H34	NC	PICCLK (I)	Don't care for 6x86.	none
J33	*Reserved*	PICD0 [DPEN#] (I/O)	10K Ohms pullup	20K Ohm pull-up
L35	NC	PICD1 [APICEN] (I/O)	10K Ohm pulldown	none
P4	NC	IERR# (O)	Don't care for 6x86.	none
Q3	PMON0 (O)	PM0/BP0 (O)	No signal.	none
Q35	NC	CPUTYP (I)	Dont' care for 6x86.	none
R34	BHOLD (I)	NC	No signal.	none
R4	PMON1 (O)	P6x86/BP1 (O)	No signal.	none
S3	PMC (O)	BP2 (O)	No signal.	none
S33	*Reserved*	NC	No signal.	none
S35	DHOLD (I)	NC	No signal.	none
S5	LBA# (O)	BP3 (O)	See note 1.	none
V34	SUSP# (I)	STPCLK# (I)	See note 2.	20K Ohm pull-up
W33	SUSPA# (O)	NC	See note 2.	none
W35	TEST (I)	NC	No signal.	20K Ohm pull-up
X34	TEST (I)	NC	No signal.	none
Y33	CLKMUL (I)	[BF] (I)	No signal. See note 5.	20K Ohm pull-down
Y35	*Reserved*	FRCMC# (I)	10K Ohm pullup	20K Ohm pull-up
Z34	NC	PEN# (I)	See note 4.	none
AA3	*Reserved*	PHIT# (I/O)	No signal.	none
AC3	*Reserved*	PHITM# (I/O)	No signal.	none
AC5	NC	PRDY (O)	Dont' care for 6x86.	none
AC35	NC	R/S# (I)	Dont' care for 6x86.	none
AD4	NC	PBGNT# (I/O)	Dont' care for 6x86.	none
AE3	NC	PBREQ# (I/O)	Dont' care for 6x86.	none
AE35	NC	D/P# (O)	Dont' care for 6x86.	none
AL19	*Reserved*	NC	No signal.	none
AL7	QDUMP# (I)	BUSCHK# (I)	10K Ohms pullup. See note 3.	20K Ohm pull-up
AN35	TEST (I)	NC	No signal.	20K Ohm pull-down

NC = No Connect

Notes:

1. LBA# is driven to a logic high during the RESET high-to-low transition and can be used to identify the presence of an 6x86.
2. The SUSP# input may be driven by the chipset provided it supports the Cyrix Suspend Mode. If it does, SUSPA# may then be monitored by the chipset. If Suspend Mode is not used, these pins should not be enabled.
3. The QDUMP# pin must be pulled high during the RESET high-to-low transition to disable the scatter/gather interface pins.

4. The Pentium PEN# (Parity Enable) may not be used in all systems. If parity is not used, this signal should be pulled high through a 10K Ohm pullup. If parity is used, this signal need only be driven low if a Pentium is installed.
5. The CLKMUL input pin controls the core/bus clock ratio. A logic low on this pin corresponds to 2:1 core/bus clock ratio operation. A logic high corresponds to 3:1 core/bus clock ratio operation. This pin has an internal pulldown to default to 2:1 mode.

3. Functional Differences

The following paragraphs describe functional differences for signals that are common to both the 6x86 and the Pentium.

3.1 Misaligned Accesses

The Pentium processor defines a misaligned access for any non-cacheable cycle as any 16, 32, or 64-bit access that crosses a 32-bit boundary. The Pentium processor always issues two bus cycles for non-cacheable memory reads/writes or I/O cycles that cross a 32-bit boundary. Pentium drives/reads the bytes corresponding with the highest address first (indicated by address and byte enables.

In contrast, the 6x86 processor behaves as follows:

1) For transfers within a 64-bit boundary, the 6x86 processor issues only a single cycle, with the appropriate byte enables valid, for all accesses requiring data within a 64-bit quadword. This difference results in lower bus utilization for the 6x86.

2) For transfers that cross the 64-bit boundary, the 6x86 processor issues the cycle for the lower address first, followed by the cycle for the higher address.

3.2 Cycles Resulting from INVD Instruction

The Pentium processor invalidates the contents of its internal caches as the result of executing an INVD instruction. This invalidation occurs even if modified data exists in the data cache. This could potentially result in a data incoherency. In contrast, the 6x86 processor always writes all modified data to external memory prior to invalidating the internal cache contents.

3.3 WM_RST Function

Assertion of the WM_RST signal causes the 6x86 to complete the current instruction and then places the 6x86 in a known state. WM_RST differs from RESET in that the contents of the on-chip cache, the write buffers, the configuration registers, and the floating point registers remain unchanged. This functionality is similar to the Pentium INIT pin. The only difference is that the INIT signal does not reset the Pentium 'model specific registers' whereas the WM_RST does not reset the 6x86 configuration registers. The Pentium 'model specific registers' are not supported on the 6x86. The 6x86 configuration registers are not supported on the Pentium.

3.4 Pins Sampled at RESET

If FLUSH# or WM_RST is sampled asserted at the RESET falling edge, the 6x86 enters tri-state test mode or enters built-in self-test, respectively. This functionality is consistent with the Pentium functionality. The 6x86 also samples the QDUMP# pin at the RESET falling edge. If QDUMP# is sampled asserted (logic low), the 6x86 enables the scatter/gather interface pins. If this 6x86 unique feature is not supported, the QDUMP# input pin should be driven inactive at RESET.

Additionally, the Pentium samples APICEN (PICD1), DPEN# (PICD0), FRCMC#, BRDYC#, BUSCHK#, CPUTYP and BE(0:3) at the falling edge of RESET to enable various functions. The 6x86 does not support these functions.

3.5 System Management Mode (SMM)

If System Management Mode (SMM) is enabled on the 6x86 (USESMI bit in CCR1 is set), SMIACT# is asserted as the result of servicing a System Management Interrupt (SMI# pin). This functionality is consistent with the Pentium functionality. Additionally, the 6x86 asserts SMIACT# as the result of executing the SMINT instruction or when the SMAC bit (6x86 CCR1 register) is set.

The SMINT instruction provides a mechanism for software to initiate an SMI. The SMAC bit allows software to access SMM space without servicing an SMI. The SMAC bit may be used to initialize system management memory. The Pentium does not support the SMINT instruction or the SMAC bit functionality.

After servicing an SMI, both the 6x86 and Pentium negate the SMIACT# signal as the result of executing the RSM

(Resume) instruction.

3.6 Burst Cycle Address Sequence

When performing burst cycles, the Pentium processor only issues the first address for the burst cycle. The remaining three addresses of the burst are not issued by the processor but are assumed to follow the sequences shown in Table 3-1.

Table 3-1. Pentium Burst Sequences

BURST CYCLE FIRST ADDRESS	ASSUMED BURST CYCLE ADDRESS SEQUENCE
0	0-8-10-18
8	8-0-18-10
10	10-18-0-8
18	18-10-8-0

The 6x86 does not strictly follow the burst cycle address sequence shown in Table 3-1 but provides two different burst modes. The 6x86 burst cycle address sequence modes are referred to as "1+4" and "linear". After reset, the 6x86 default burst mode is "1+4". The burst sequences for the "1+4" mode are shown in Table 3-2.

Table 3-2. 6x86 "1+4" Burst Address Sequences

BURST CYCLE FIRST ADDRESS	SINGLE READ CYCLE PRIOR TO BURST	ASSUMED BURST CYCLE ADDRESS SEQUENCE
0	None.	0-8-10-18
8	Address 8.	0-8-10-18
10	None.	10-18-0-8
18	Address 18.	10-18-0-8

In "1+4" mode, the 6x86 performs a single read cycle, prior to the burst cycle, if the desired address is (...xx8) or (...xx18). Performing this single read cycles allows the 6x86 to read the critical data. In addition, the 6x86 samples the state of KEN# during this cycle. If KEN# is active, the 6x86 then performs the burst cycle with the address sequence shown in Table 3-2. The 6x86 CACHE# output is not asserted during the single read cycle prior to the burst. Therefore, CACHE# must not be used to qualify the KEN# input to the processor. If the 6x86 CACHE# output is not used to qualify the KEN# input, this burst mode is compatible with chipsets designed for the Pentium. In addition, if KEN# is returned active for the “1” read cycle in the “1+4”, all bytes supplied to the CPU must be valid.

The address sequences for the 6x86's linear burst mode are shown in Table 3-3. Operating the 6x86 in linear burst mode is recommended since it minimizes processor bus activity translating to higher system processor/system performance. Linear burst mode can be enabled through the 6x86 configuration registers.

Table 3-3. 6x86 Linear Burst Address Sequences

BURST CYCLE FIRST ADDRESS	ASSUMED BURST CYCLE ADDRESS SEQUENCE
0	0-8-10-18
8	8-10-18-0
10	10-18-0-8
18	18-0-8-10