

---

# List of Figures

---

## 1 Microprocessors, Platforms, and Systems 1

---

<b>Figure 1.1</b>	Design Process	<b>5</b>
<b>Figure 1.2</b>	3D Graphics PC Platform	<b>36</b>
<b>Figure 1.3</b>	Photograph of a 3D Graphics Motherboard	<b>37</b>

## 2 A Microarchitecture Case Study 63

---

<b>Figure 2.1</b>	K6 Die Photograph and Overlay	<b>68</b>
<b>Figure 2.2</b>	K6 3D Block Diagram	<b>69</b>
<b>Figure 2.3</b>	RUX and RUY Execution Units	<b>81</b>
<b>Figure 2.4</b>	Upper and Lower Portions of the Processor	<b>87</b>
<b>Figure 2.5</b>	Instruction Buffer, Instruction Registers 1 & 2, and the Decoders	<b>114</b>
<b>Figure 2.6</b>	Instruction Buffer Index 0 Multiplexer	<b>115</b>
<b>Figure 2.7</b>	Predecoder Logic	<b>116</b>
<b>Figure 2.8</b>	Decoder OpQuads and Scheduler OpQuads	<b>127</b>
<b>Figure 2.9</b>	The Scheduler and Its Centralized Buffer	<b>130</b>
<b>Figure 2.10</b>	OpQuad ROM, Vector Decoder, and Exception Decoder	<b>139</b>
<b>Figure 2.11</b>	Displacement Buses from Decoder	<b>149</b>
<b>Figure 2.12</b>	Integer and Single-Cycle MMX RUX/RUY Pipeline Stages	<b>159</b>
<b>Figure 2.13</b>	Generic Pipeline Stages	<b>160</b>
<b>Figure 2.14</b>	2-Cycle MMX and 3D RUX/RUY Pipeline Stages	<b>163</b>
<b>Figure 2.15</b>	LU Pipeline Stages	<b>164</b>
<b>Figure 2.16</b>	The LU Intermediate or Execution Pipeline Stages	<b>165</b>
<b>Figure 2.17</b>	Sources of Segment Base and Limit, Scaled Index, and Displacement Values	<b>166</b>
<b>Figure 2.18</b>	SU Pipeline Stages	<b>167</b>
<b>Figure 2.19</b>	The Intermediate or Execution SU Pipeline Stages and Store Queue Access	<b>168</b>
<b>Figure 2.20</b>	Store Commit Pipeline Stages	<b>169</b>

<b>Figure 2.21</b>	The BRU Pipeline Stages	<b>175</b>
<b>Figure 2.22</b>	System Interface Unit	<b>180</b>

### **3 The K6 3D Microarchitecture** **183**

---

<b>Figure 3.1</b>	Example of One Bit of a Static Field	<b>187</b>
<b>Figure 3.2</b>	Example of One Bit of a Dynamic Field	<b>191</b>
<b>Figure 3.3</b>	Common Pipeline Stages for All RegOps, LdOps, and StOps	<b>221</b>
<b>Figure 3.4</b>	Op Issue Selection	<b>230</b>
<b>Figure 3.5</b>	Scan Chain Style Implementation of Op Selection	<b>231</b>

### **4 Technology Components of Platform Architecture** **315**

---

<b>Figure 4.1</b>	PC Platform Categories and Subcategories	<b>323</b>
<b>Figure 4.2</b>	Example ATX Motherboard Layout	<b>341</b>
<b>Figure 4.3</b>	Example ATX Connector Placement Viewed From Rear of Board	<b>341</b>
<b>Figure 4.4</b>	Device Bay Conceptual Drawings	<b>345</b>
<b>Figure 4.5</b>	Comparison of Thick and Thin Coaxial Cables used for Ethernet	<b>356</b>
<b>Figure 4.6</b>	Comparison of Ethernet Types	<b>359</b>
<b>Figure 4.7</b>	Common Ethernet Connectors and Cables	<b>360</b>
<b>Figure 4.8</b>	Bandwidth of Channels and Links (Bandwidth in Mbits per second, Logarithmic Scale)	<b>363</b>
<b>Figure 4.9</b>	Expected Growth in Microprocessor Clock Speed	<b>369</b>
<b>Figure 4.10</b>	Microarchitectural Performance vs Time	<b>370</b>
<b>Figure 4.11</b>	Example USB Interconnect Use in a Small System	<b>373</b>
<b>Figure 4.12</b>	USB Connector and Port	<b>373</b>
<b>Figure 4.13</b>	Drawing of USB Connector and Port Internal Detail	<b>373</b>
<b>Figure 4.14</b>	Six-Wire External Port and Plug Connector	<b>376</b>
<b>Figure 4.15</b>	Common SCSI Connectors	<b>379</b>
<b>Figure 4.16</b>	View of 8-bit ISA Card Edge Adjacent to 8-bit Portion of ISA Card Slot	<b>382</b>
<b>Figure 4.17</b>	Views of PCI Card Slots and PCI Card Edge	<b>391</b>
<b>Figure 4.18</b>	Comparison of Popular Card Slots	<b>392</b>
<b>Figure 4.19</b>	Matrix of PCI Card Types and Associated Compatible Slots	<b>398</b>
<b>Figure 4.20</b>	AGP Card Types and Associated Compatible Connectors	<b>408</b>
<b>Figure 4.21</b>	Views of AGP Slot and AGP Card Edge	<b>409</b>
<b>Figure 4.22</b>	321-pin SPGA Package	<b>411</b>

<b>Figure 4.23</b>	AMP ZIF	<b>412</b>
<b>Figure 4.24</b>	Same Scale Comparison of Sockets 4, 5 and 7	<b>413</b>
<b>Figure 4.25</b>	Split Power Planes for Dual-Supply Processors	<b>416</b>

## **5 Platform Memory Technology** **427**

<b>Figure 5.1</b>	Asynchronous DRAM Block Diagram	<b>429</b>
<b>Figure 5.2</b>	Abstract View of DRAM Analog Core	<b>429</b>
<b>Figure 5.3</b>	Simplified Asynchronous DRAM Read Timing	<b>433</b>
<b>Figure 5.4</b>	Primary Elements of a Rambus-Based System	<b>436</b>
<b>Figure 5.5</b>	Topology Details of the Rambus Channel	<b>438</b>
<b>Figure 5.6</b>	Rambus Channel Signaling	<b>439</b>
<b>Figure 5.7</b>	Example Rambus Interface with Memory Controller	<b>440</b>
<b>Figure 5.8</b>	The AMD-640 System Controller (A North-Bridge)	<b>445</b>
<b>Figure 5.9</b>	All SDRAM Bank Configuration of the AMD-640	<b>445</b>
<b>Figure 5.10</b>	DRAM Control Registers in the AMD-640 System Controller	<b>447</b>
<b>Figure 5.11</b>	SDRAM Operating Modes	<b>450</b>
<b>Figure 5.12</b>	Bank-Pairing	<b>451</b>
<b>Figure 5.13</b>	Mapping of Physical Address Bits to Row and Column Address Bits in the AMD-640 System Controller	<b>457</b>

## **6 Platform Optimization Techniques and Directions** **463**

<b>Figure 6.1</b>	Rate Degradation	<b>474</b>
<b>Figure 6.2</b>	Roles of Platform Components in 3D Graphics	<b>482</b>
<b>Figure 6.3</b>	3D Graphics Pipeline Stages (The Geometry Stage)	<b>486</b>
<b>Figure 6.4</b>	3D Graphics Pipeline Stage (The Rendering Stage and The Display Stage)	<b>487</b>
<b>Figure 6.5</b>	Methods of Connectivity	<b>496</b>
<b>Figure 6.6</b>	Variations in Internet Bandwidth	<b>496</b>
<b>Figure 6.7</b>	66MHz Socket 7 Bus Platform	<b>503</b>
<b>Figure 6.8</b>	A 100MHz Super 7 Bus Platform	<b>503</b>
<b>Figure 6.9</b>	A 100MHz Super 7 Bus Platform with Backside Cache	<b>504</b>
<b>Figure 6.10</b>	AMD-K7 Processor	<b>507</b>
<b>Figure 6.11</b>	Communications Bandwidth Ascension	<b>509</b>
<b>Figure 6.12</b>	Internet-Connected Computation	<b>511</b>
<b>Figure 6.13</b>	Intranet-Connected Computation	<b>512</b>

