Table of Contents

Am186CC ISDN Router Schematics

Reference Design

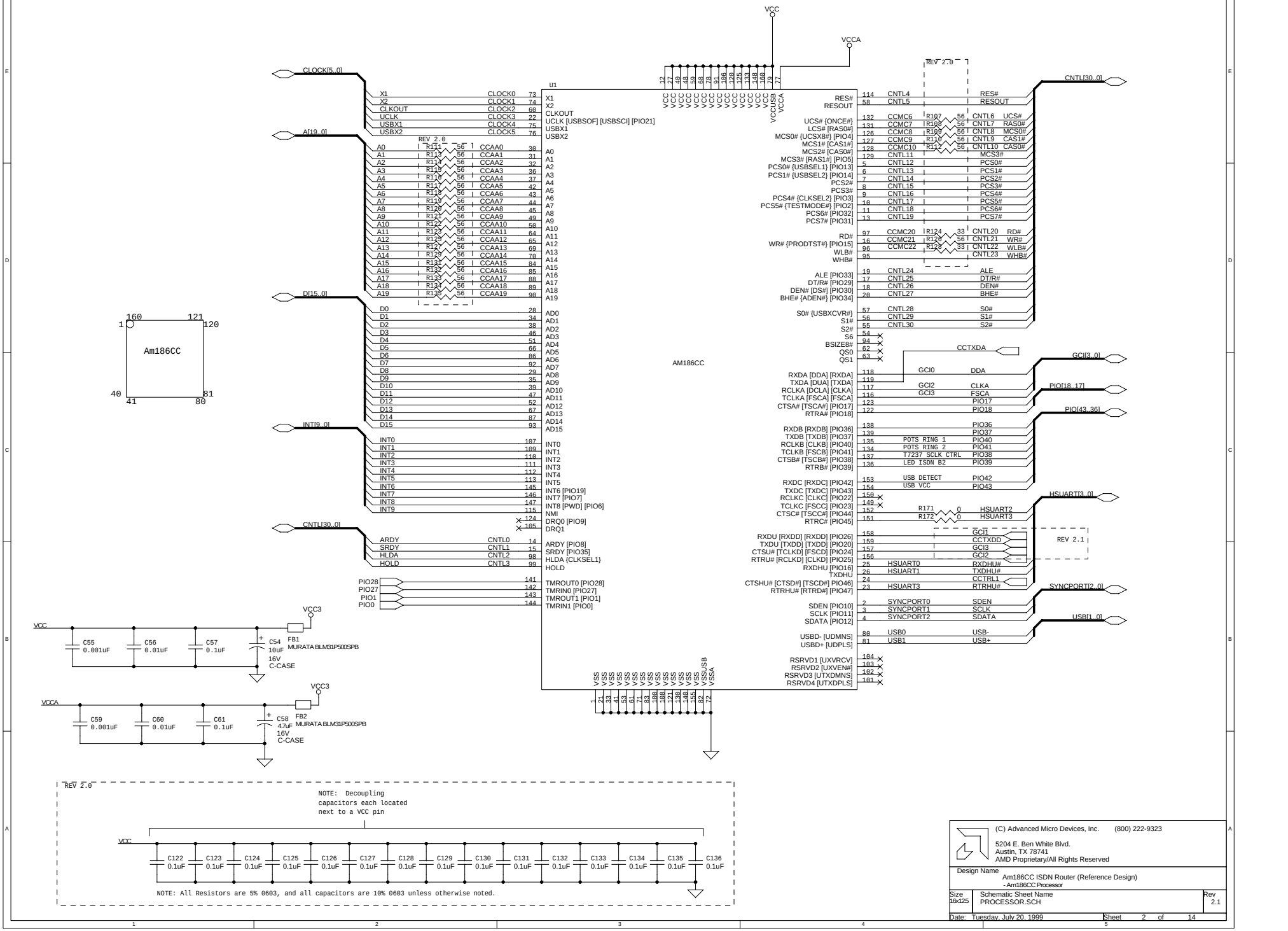
Rev 1.0: Original design
Rev 1.1: Updated design
Rev 2.0: Updated design
Rev 2.1: Updated design

5204 E. Ben White Blvd.
Austin, TX 78741

Design Name
Am186CC ISDN Router (Reference Design) - Cover Page

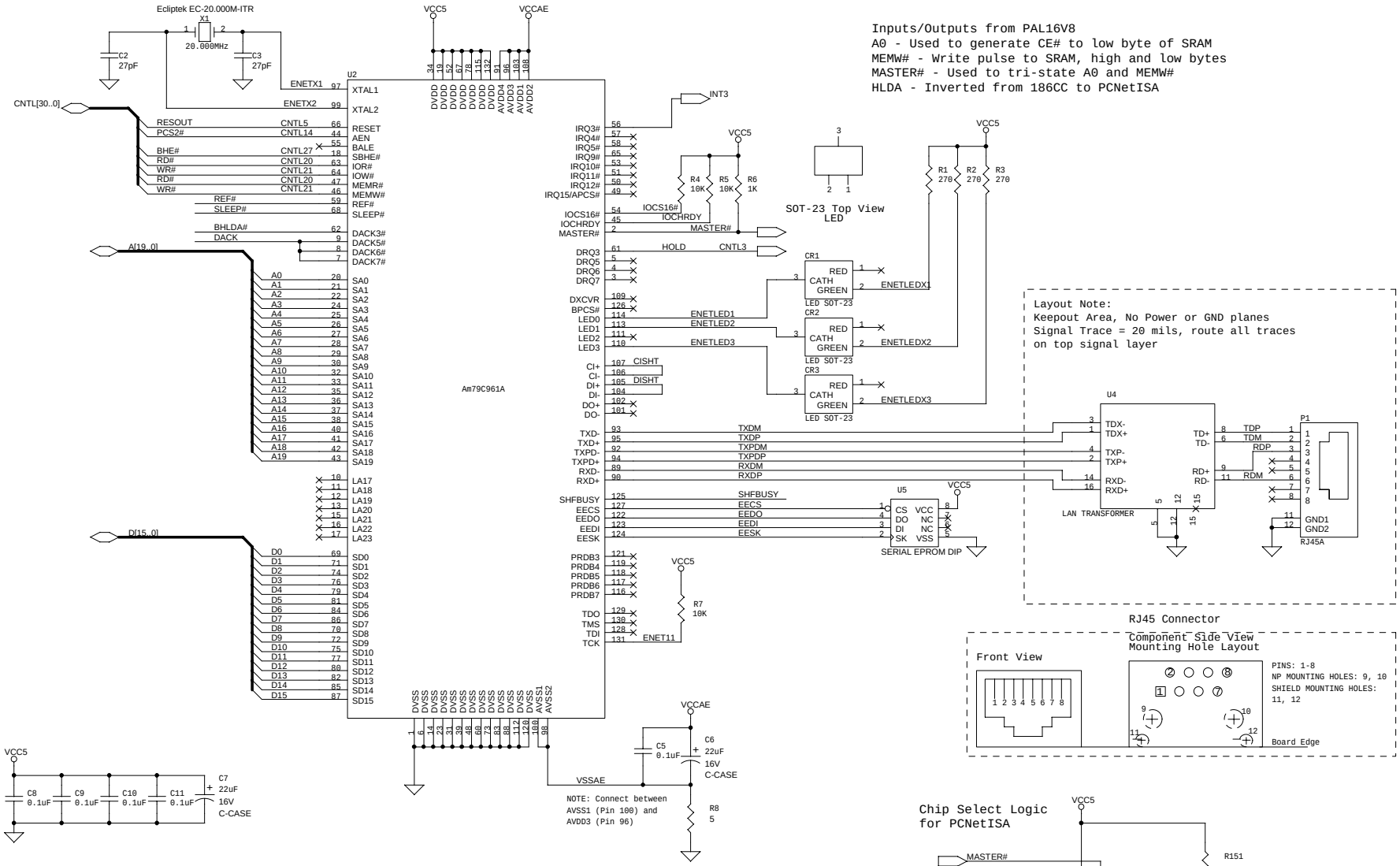
Size	Schematic Sheet Name	Rev
16x125	COVER.SCH	2.1

Date: Tuesday, July 20, 1999 Sheet 1 of 14



Design Name	Am186CC ISDN Router (Reference Design) - Am186CC Processor
Size 10x125	Schematic Sheet Name PROCESSOR.SCH
Rev	2.1
Date: Tuesday, July 20, 1999	Sheet 2 of 14

Inputs/Outputs from PAL16V8
A0 - Used to generate CE# to low byte of SRAM
MEMW# - Write pulse to SRAM, high and low bytes
MASTER# - Used to tri-state A0 and MEMW#
HLDA - Inverted from 186CC to PCNetISA



Design Name
Am186CC ISDN Router (Reference Design) - PCNetISA

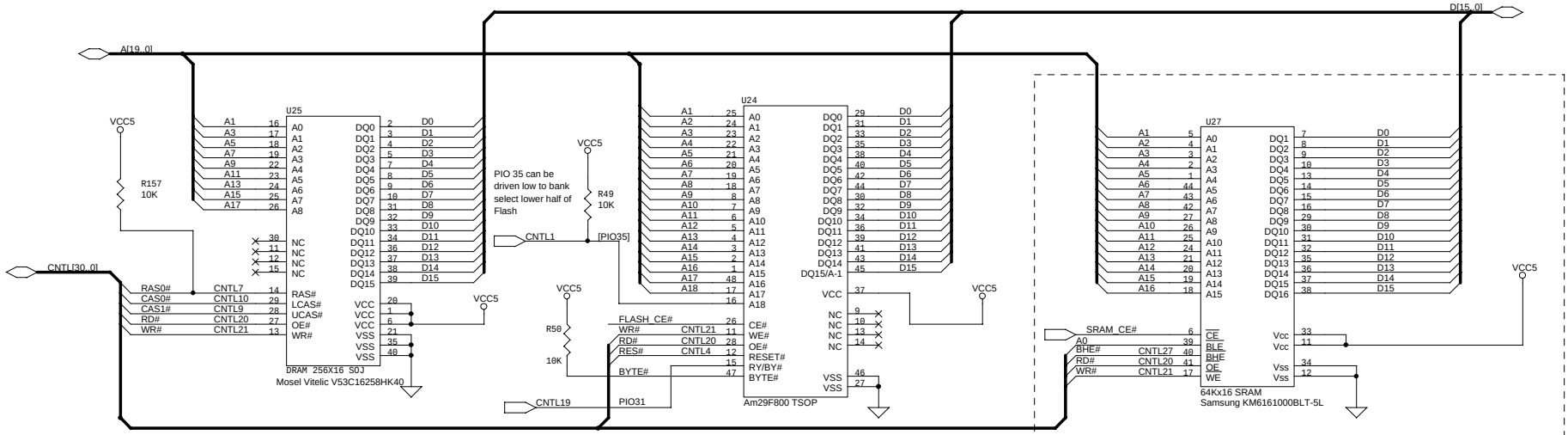
Size	Schematic Sheet Name	Rev
10x125	ETHERNET1.SCH	2.1

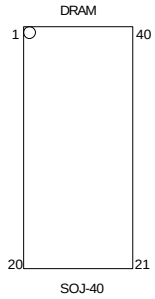
Date: Tuesday, July 20, 1999 Sheet 3 of 14

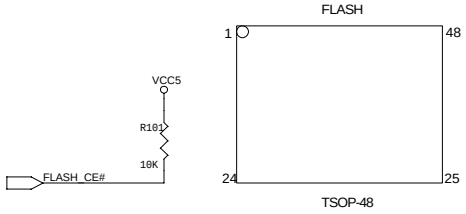
Am186CC DRAM - System RAM

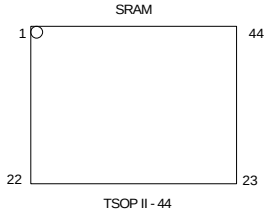
Am186CC Flash - System ROM

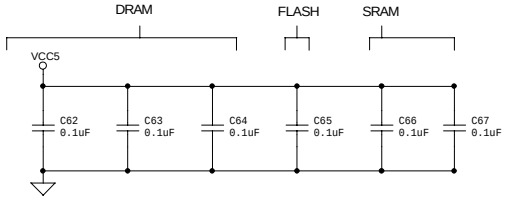
PCNetISA SRAM - Packet Buffer





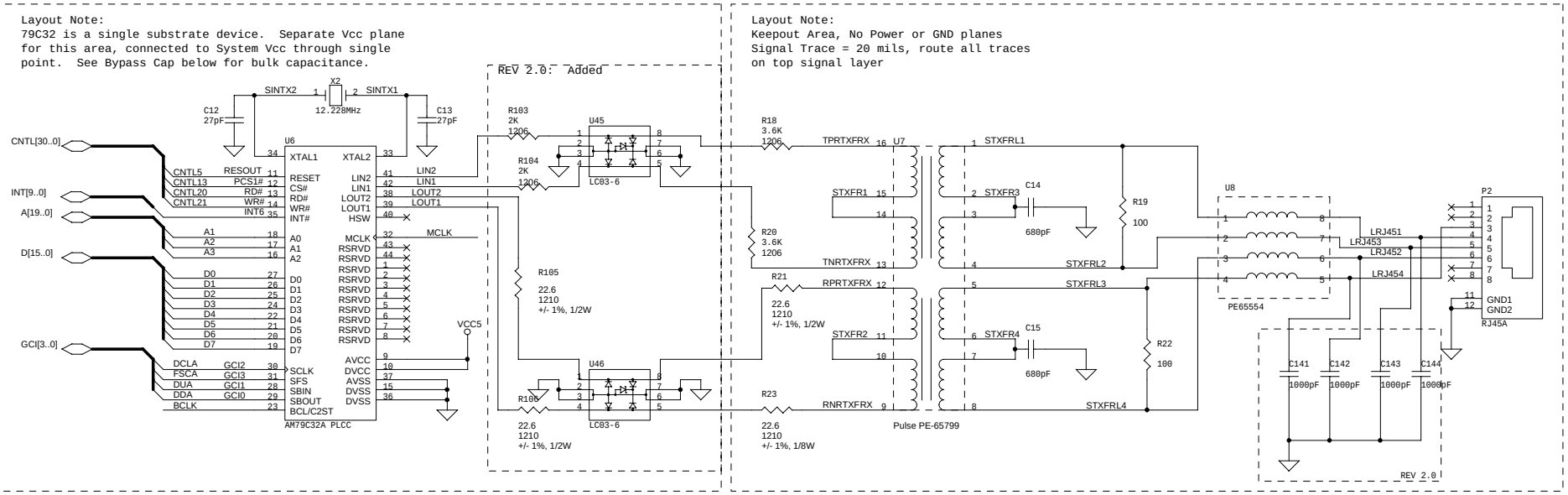


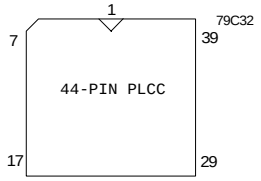


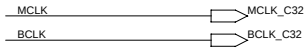


Design Name: Am186CC ISDN Router (Reference Design) - System Memory		
Size: 16x125	Schematic Sheet Name: SYSTEM_MEMORY.SCH	Rev: 2.1
Date: Tuesday, July 20, 1999	Sheet 4 of 14	

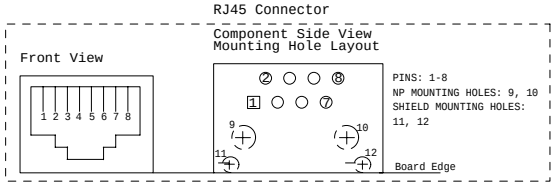
AM79C32 - ISDN S Interface

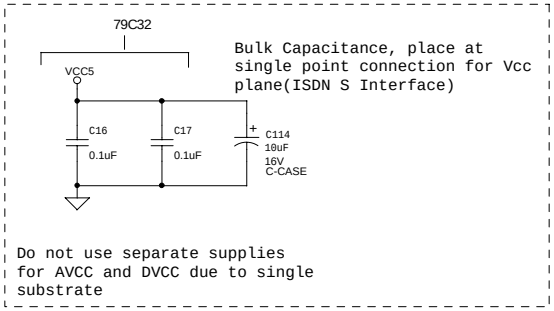


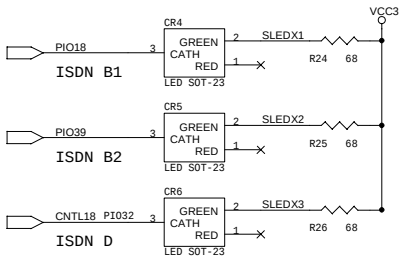




MCLK_32 is synchronized with GCI/IOM-S FS and PCLK to support timing requirements of the DSLAC. BCLK_C32 is also use to synchronize MCLK_32







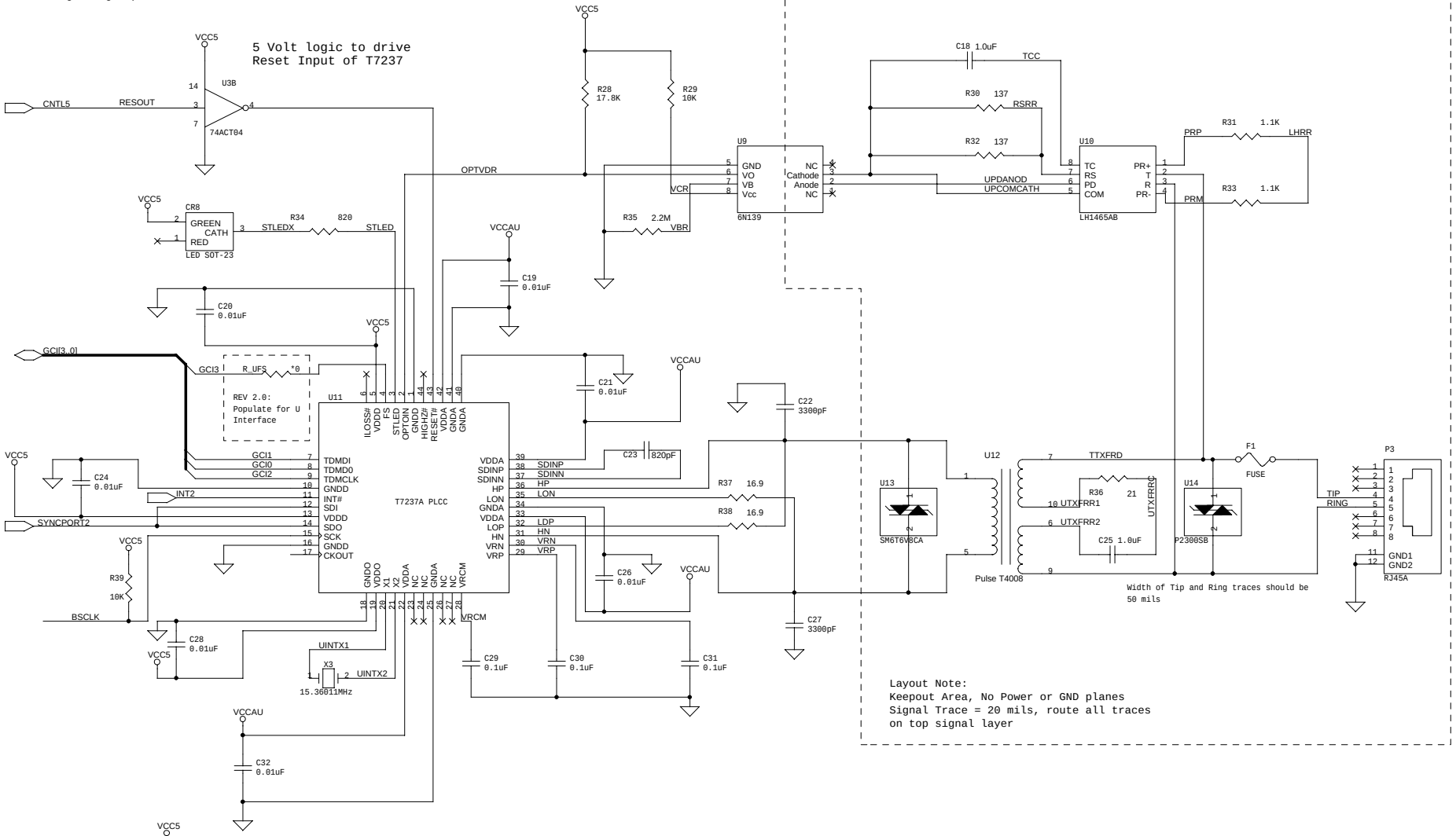
Design Name: Am186CC ISDN Router (Reference Design)- ISDN S Interface

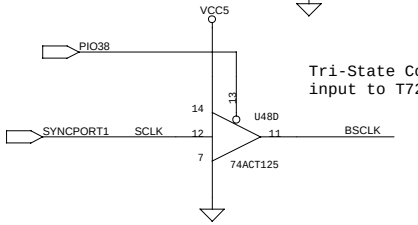
Size	Schematic Sheet Name	Rev
16x125	ISDN_S.SCH	2.1

Date: Tuesday, July 20, 1999 Sheet 5 of 14

U Interface

Layout Note:
Separate Vcc plane for this area,
includes all components on right
half of page. Connect to system Vcc
through single point.

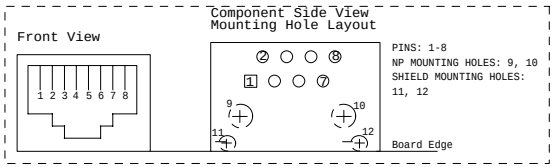




Tri-State Control for SCLK
input to T7237

BSCLK - From PAL16V8.
PIO38 is used to
tri-state(with pull-up)
SCLK when T7237 is not
accessed by AM186CC.

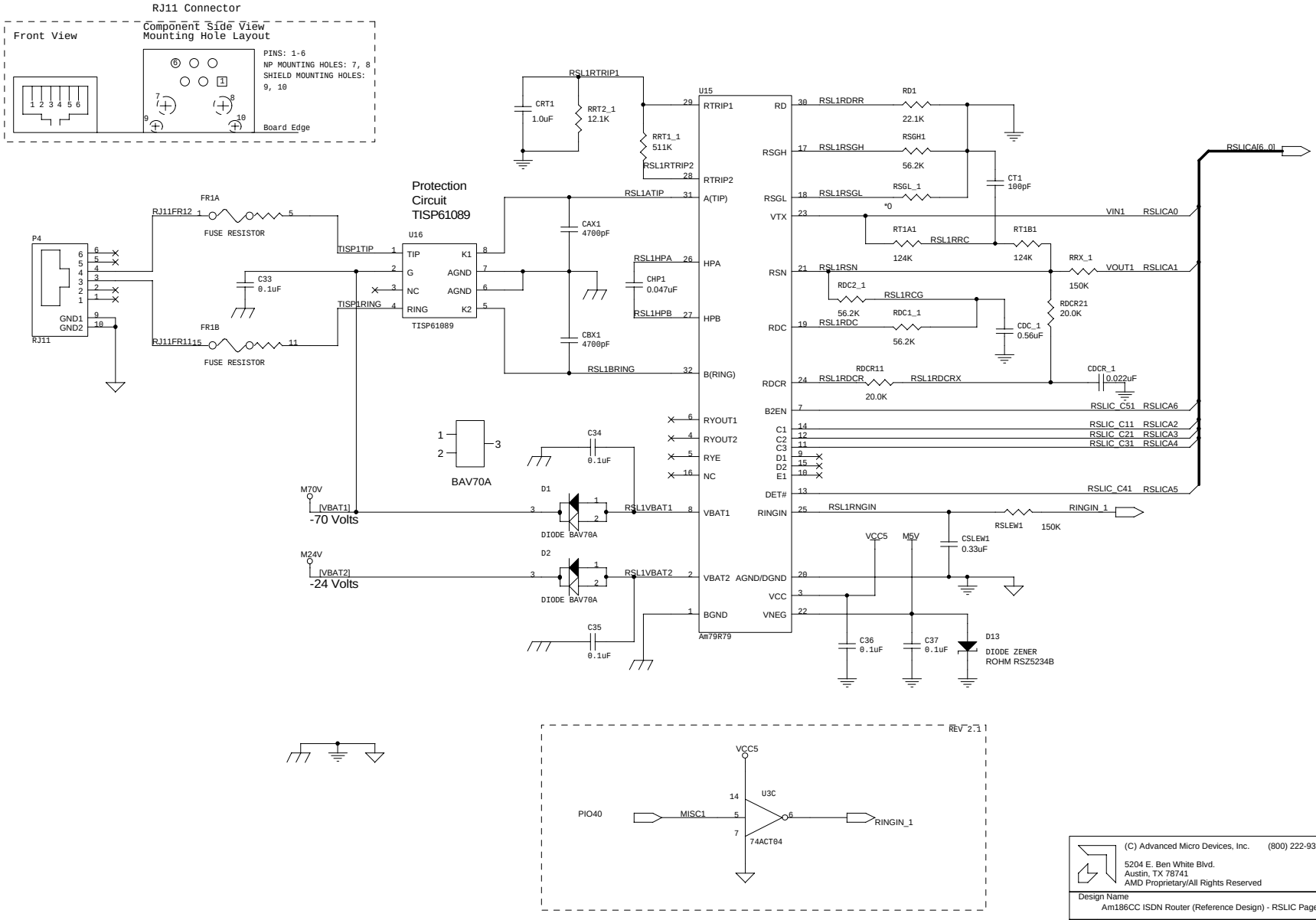
RJ45 Connector
Component Side View
Mounting Hole Layout



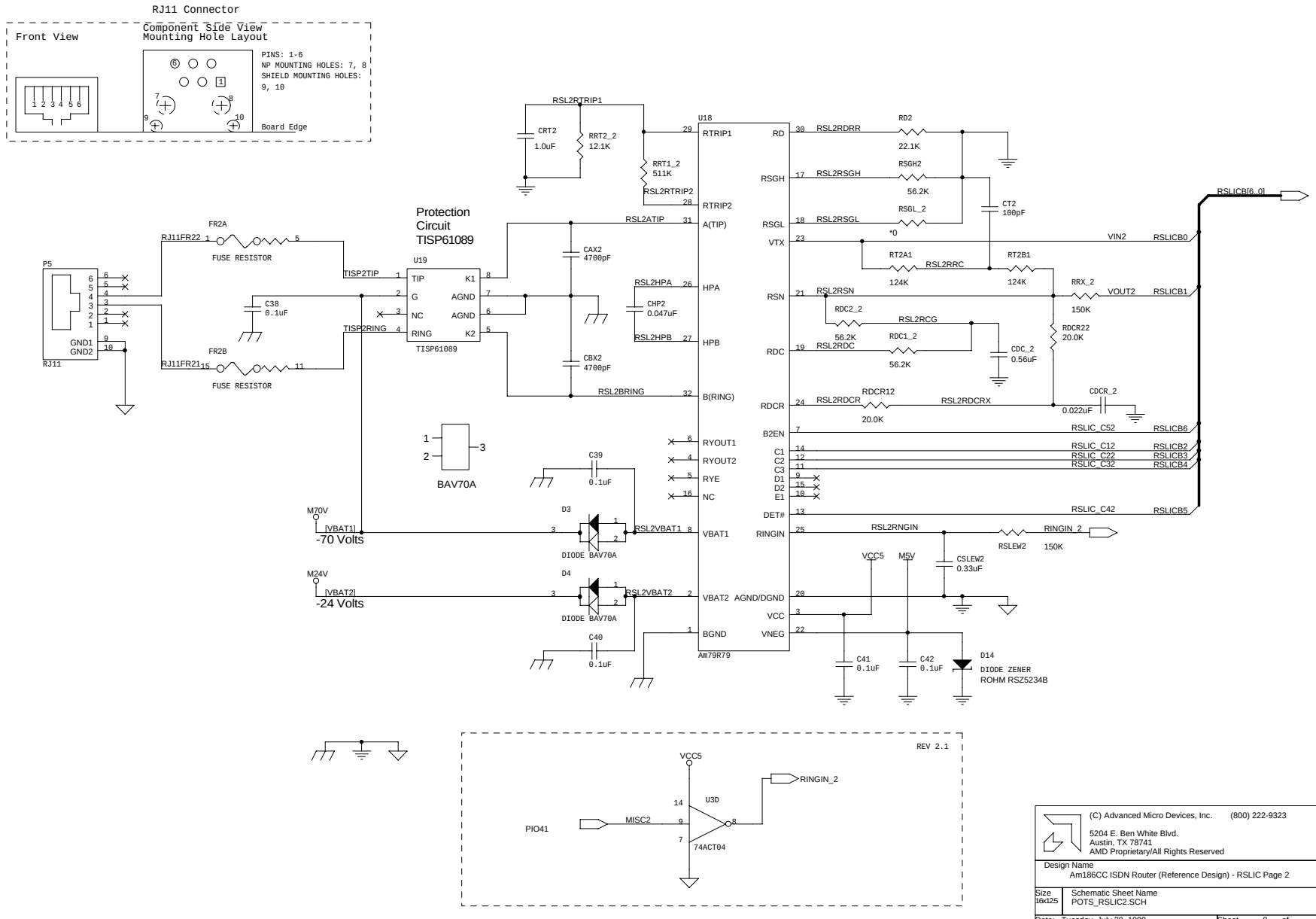
Design Name
Am186CC ISDN Router (Reference Design) - ISDN U Interface

Size	Schematic Sheet Name	Rev
16x125	ISDN_U.SCH	2.1

Date: Tuesday, July 20, 1999 Sheet 6 of 14



Design Name: Am186CC ISDN Router (Reference Design) - RSLIC Page 1		
Size: 16x125	Schematic Sheet Name: POTS_RSLIC1.SCH	Rev: 2.1
Date: Tuesday, July 20, 1999	Sheet 7 of 14	


RJ11 Connector
Component Side View
Front View
Mounting Hole Layout
PINS: 1-6
NP MOUNTING HOLES: 7, 8
SHIELD MOUNTING HOLES: 9, 10
Board Edge
Protection Circuit TISP61089
TISP61089
BAV70A
DIODE BAV70A
DIODE BAV70A
DIODE ZENER ROHM RSZ5234B
FUSE RESISTOR
FUSE RESISTOR
RJ11
Am79R79
74ACT04
-70 Volts
-24 Volts
REV 2.1
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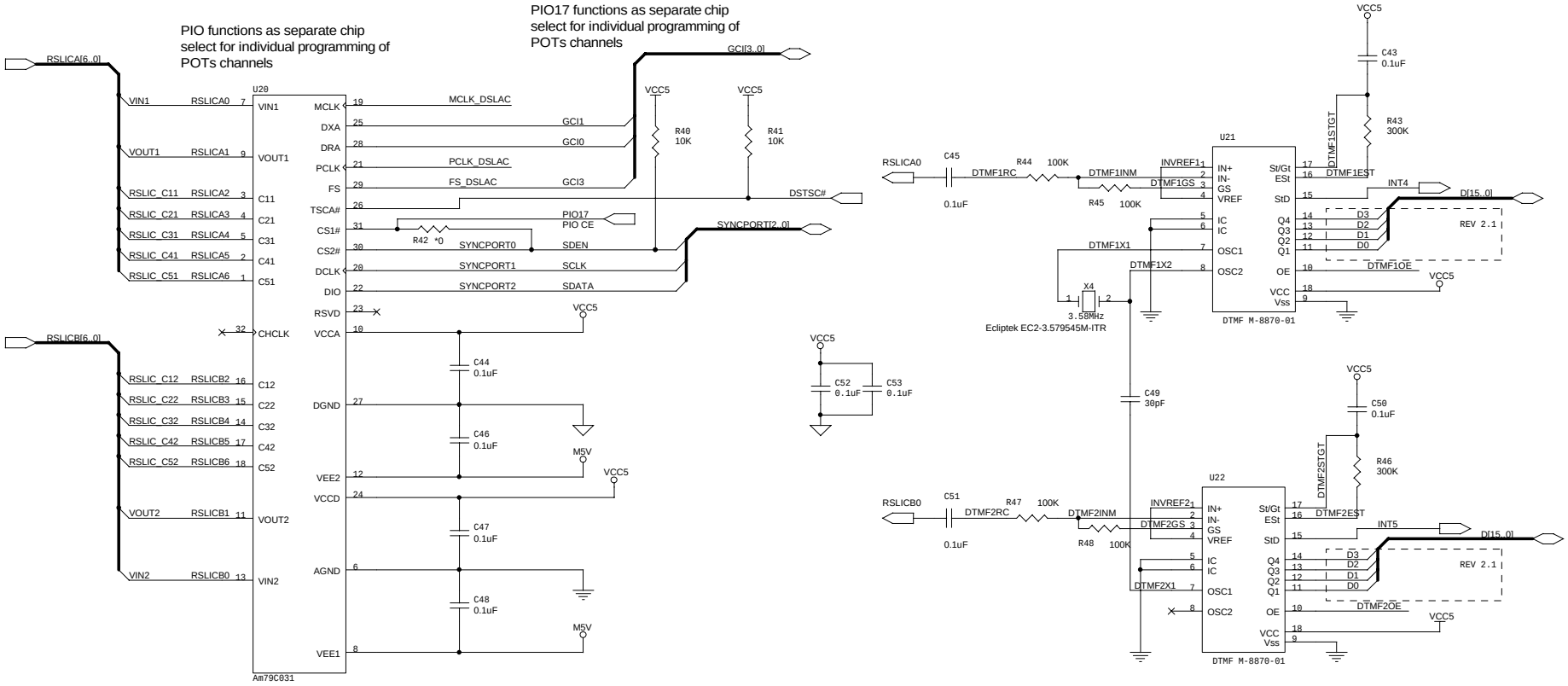
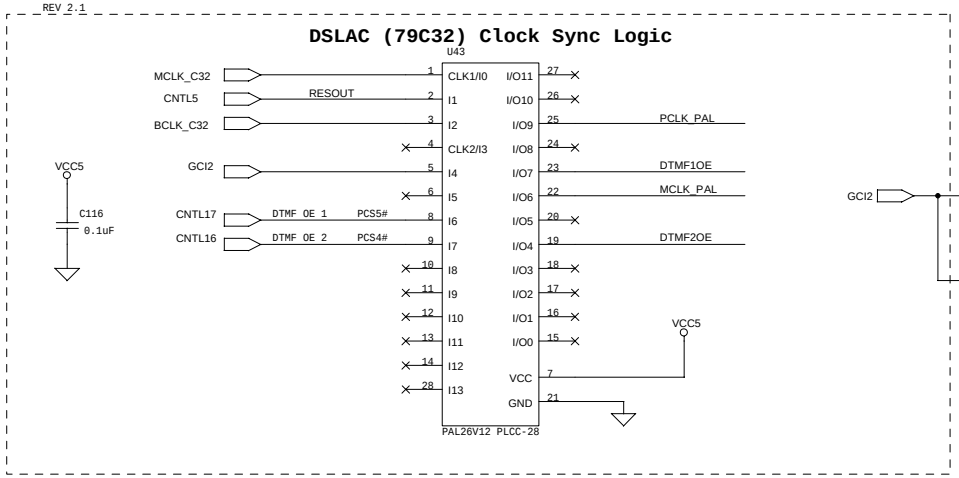
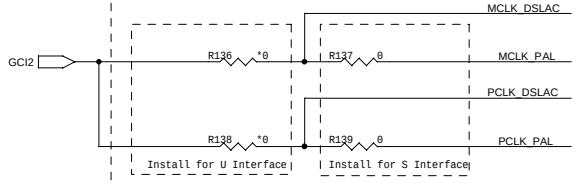
Design Name
Am186CC ISDN Router (Reference Design) - RSLIC Page 2
Schematic Sheet Name
POTS_RSLIC2.SCH
Rev 2.1
Date: Tuesday, July 20, 1999
Sheet 8 of 14







POTs Functionality with S or U Transceivers

ISDN U Interface: The T7237 does not tri-state FS. When using the 79C32 for ISDN S Interface, remove R_UFS. For ISDN U Interface, populate R_UFS. (See schematic page 6)

ISDN S Interface: The 79C32 GCI Port must be synchronized with MCLK_C32. Jumper MCLK_PAL to MCLK_DSLAC and PCLK_PAL to PCLK_DSLAC for operation with the 79C32

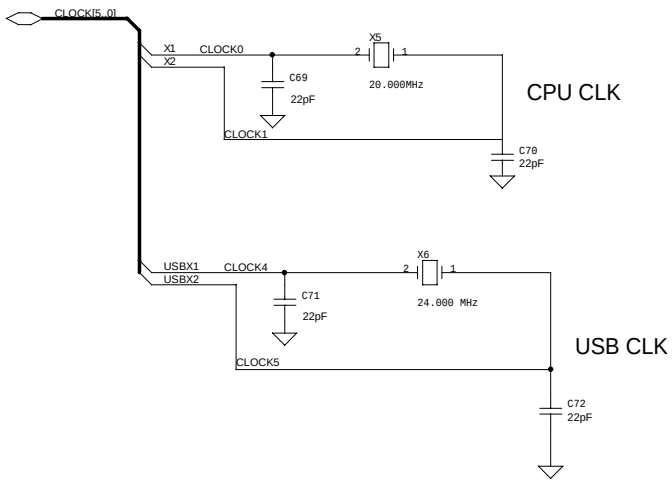
ISDN U Interface: The T7237 can drive both MCLK_DSLAC and PCLK_DSLAC using TDMCLK. Jumper GCI2 with MCLK_DSLAC and PCLK_DSLAC for operation with the T7237

Design Name: Am186CC ISDN Router (Reference Design) - DSLAC

Size: 16x125 | Schematic Sheet Name: POTS_DSLAC.SCH | Rev: 2.1

Date: Tuesday, July 20, 1999 | Sheet 9 of 14

CPU, USB AND UART CLOCKS

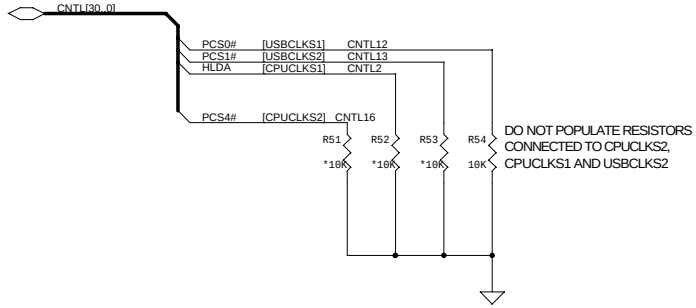


CPU PLL CLK MODES

CPUCLKS1	CPUCLKS2	CPU PLL MODE
1	1	2X PLL (DEFAULT)
1	0	4X PLL
0	1	1X PLL
0	0	PLL BYPASS

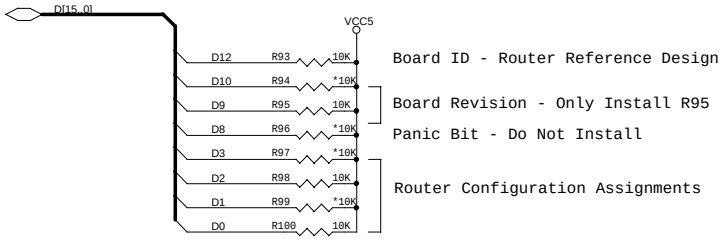
USB PLL CLK MODES

USBCLKS1	USBCLKS2	USB PLL MODE
1	1	USE CPU CLK, USB PLL DISABLED
1	0	4X PLL
0	1	2X PLL (DEFAULT)
0	0	PLL BYPASS

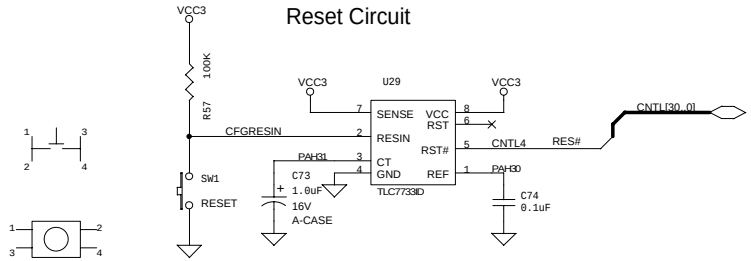


Reset Configuration

Populate D0, D2 and D12



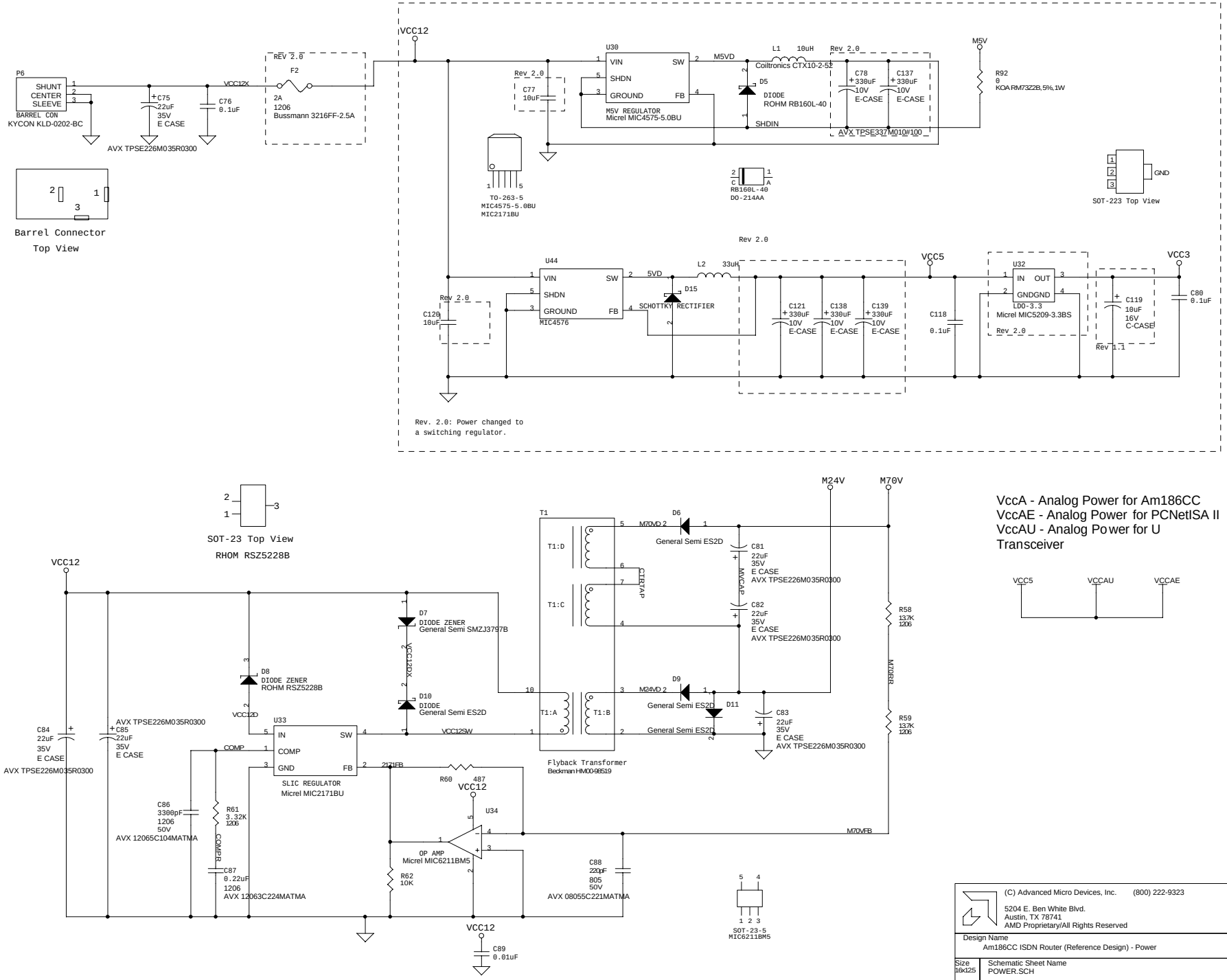
Reset Circuit



Design Name
Am186CC ISDN Router (Reference Design) - Clock/Configuration

Size	Schematic Sheet Name	Rev
16x125	CLOCK_CONFIGURATION.SCH	2.1

Date: Tuesday, July 20, 1999 Sheet 10 of 14


P6
SHUNT
CENTER
SLEEVE
BARREL CON
KYCON KLD-0202-BC
C75
22uF
35V
E CASE
AVX TPSE226M035R0300
C76
0.1uF
VCC12X
REV 2.0
F2
2A
1206
Bussmann 3216FF-2.5A
VCC12
U30
VIN
SW
SHDN
GROUND
FB
M5V REGULATOR
Micrel MIC4575-5.0BU
M5VD
L1 10uH
Rev 2.0
Coiltronics CTX10-2-52
D5
DIODE
ROHM RB160L-40
SHDIN
C78
330uF
10V
E-CASE
C137
330uF
10V
E-CASE
AVX TPSE337M010#100
M5V
R92
0
KOA RM73Z2B,5%,1W
Rev 2.0
C77
10uF
TO-263-5
MIC4575-5.0BU
MIC2171BU
RB160L-40
DO-214AA
SOT-223 Top View
GND
Barrel Connector
Top View
Rev 2.0
U44
VIN
SW
SHDN
GROUND
FB
MIC4576
5VD
L2 33uH
D15
SCHOTTKY RECTIFIER
C120
10uF
C121
330uF
10V
E-CASE
C138
330uF
10V
E-CASE
C139
330uF
10V
E-CASE
VCC5
C118
0.1uF
U32
IN
OUT
GNDGND
LDO-3.3
Micrel MIC5209-3.3BS
Rev 2.0
VCC3
C119
10uF
16V
C-CASE
Rev 1.1
C80
0.1uF
Rev. 2.0: Power changed to
a switching regulator.
SOT-23 Top View
RHOM RSZ5228B
M24V
M70V
VccA - Analog Power for Am186CC
VccAE - Analog Power for PCNetISA II
VccAU - Analog Power for U
Transceiver
VCC5
VCCAU
VCCAE
VCC12
T1
T1:D
T1:C
T1:A
T1:B
CT12VAP
D6
General Semi ES2D
M70VD 2
C81
22uF
35V
E CASE
AVX TPSE226M035R0300
MV5CAP
C82
22uF
35V
E CASE
AVX TPSE226M035R0300
R58
137K
1206
M70RR
R59
137K
1206
D7
DIODE ZENER
General Semi SMZJ3797B
VCC12DX
D8
DIODE ZENER
ROHM RSZ5228B
VCC12D
D10
DIODE
General Semi ES2D
D9
M24VD 2
General Semi ES2D
D11
General Semi ES2D
C83
22uF
35V
E CASE
AVX TPSE226M035R0300
Flyback Transformer
Beckman HM0098519
C84
22uF
35V
E CASE
AVX TPSE226M035R0300
C85
22uF
35V
E CASE
AVX TPSE226M035R0300
U33
IN
SW
COMP
GND
FB
SLIC REGULATOR
Micrel MIC2171BU
VCC12SW
2171FB
R60 487
C86
3300pF
1206
50V
AVX 12065C104MATMA
R61
3.32K
1206
COMPR
C87
0.22uF
1206
AVX 12063C224MATMA
R62
10K
U34
OP AMP
Micrel MIC6211BM5
C88
220pF
805
50V
AVX 08055C221MATMA
M70VFB
SOT-23-5
MIC6211BM5
C89
0.01uF
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Design Name
Am186CC ISDN Router (Reference Design) - Power
Size
16x125
Schematic Sheet Name
POWER.SCH
Rev
2.1
Date: Tuesday, July 20, 1999
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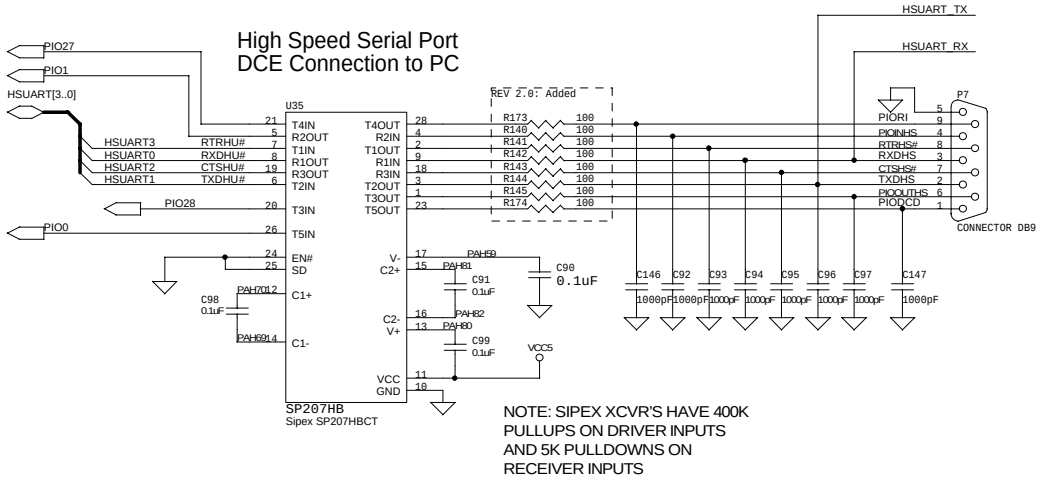
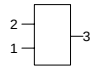
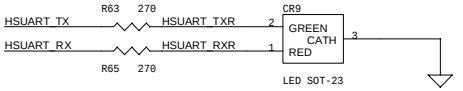


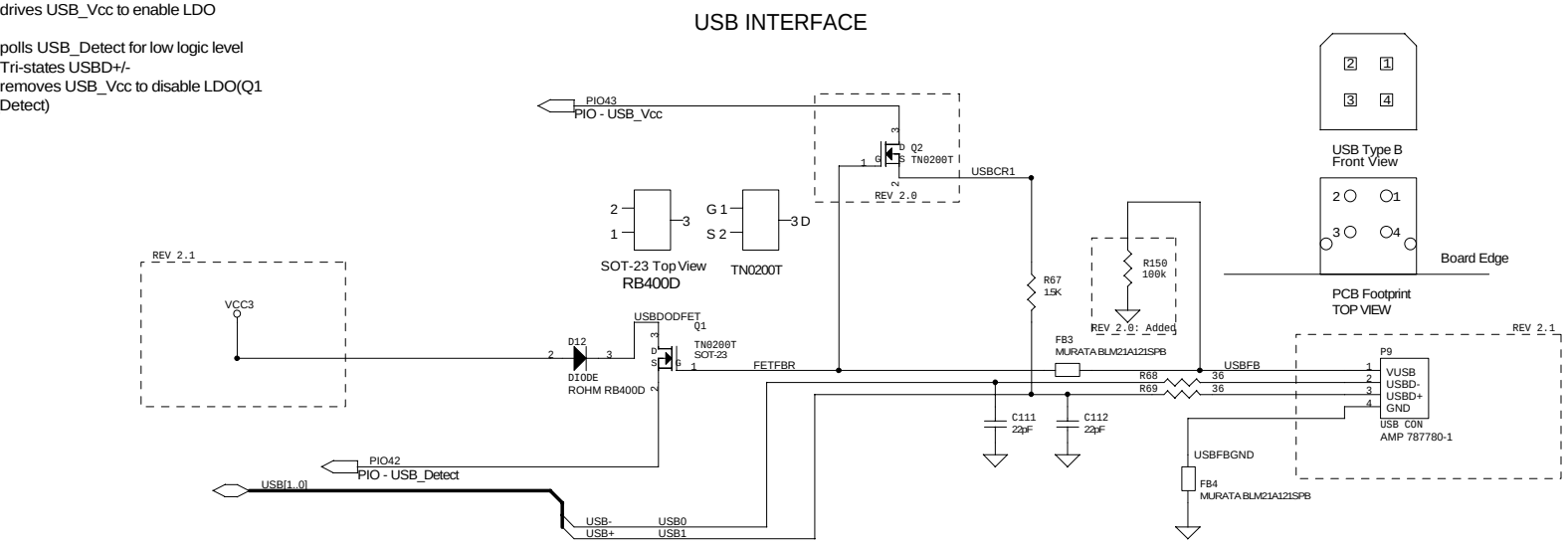




Am186CC USB Attach/Detach

Attach
1) Am186CC polls USB_Detect for high logic level
2) Am186CC drives USB_Vcc to enable LDO

Detach
1) Am186CC polls USB_Detect for low logic level
2) Am186CC Tri-states USBD+/-
3) Am186CC removes USB_Vcc to disable LDO(Q1 isolates USB_Detect)

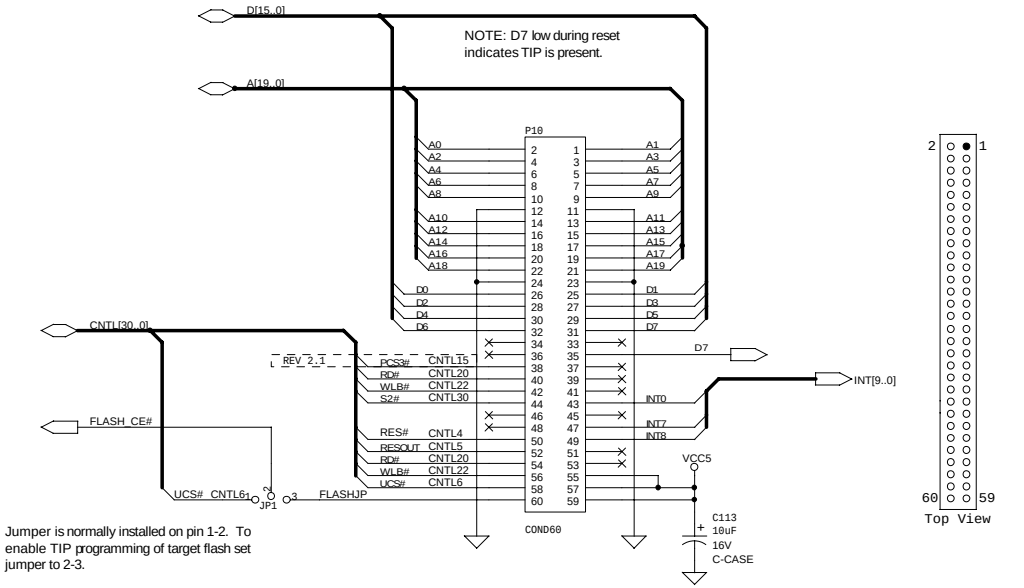


Design Name
Am186CC ISDN Router (Reference Design) - Serial and USB Ports

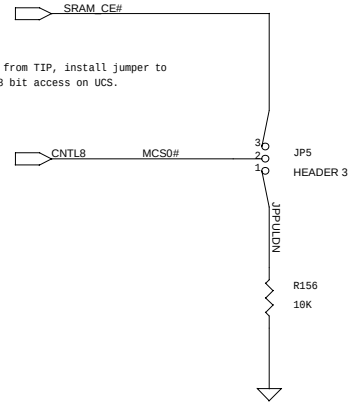
Size	Schematic Sheet Name	Rev
16x125	SERIAL_USB.SCH	2.1

Date: Tuesday, July 20, 1999 Sheet 12 of 14

Tip Conn.



Jumper is normally installed on pin 1-2. To enable TIP programming of target flash set jumper to 2-3.



PIO RESOURCE ASSIGNMENTS

PIO	SIGNAL	FUNCTIONALITY
PIO35	SRDY	FLASH BANK SELECT
PIO31	PCS7#	FLASH RY/BY# INPUT
PIO42	RXD_C	USB_DETECT
PIO43	TXD_C	USB_VCC
PIO18	RTRA	LED ISDN B1
PIO39	RTR_B#	LED ISDN B2
PIO32	PCS6#	LED ISDN D
PIO8	ARDY	LED USB
PIO17	CTSA	CE FOR DSLAC
PIO28	TMROUT0	HSUART PnP - DSR
PIO27	TMRIN0	HSUART PnP - RI
PIO1	TMROUT1	HSUART PnP - DTR
PIO0	TMRIN1	HSUART PnP - CD
PIO38	CTS_B	T7237 SCLK CNTL
PIO40	RCLK_B	POTS LINE 1 RINGING SIGNAL
PIO41	TCLK_B	POTS LINE 2 RINGING SIGNAL
PIO2	PCS5#	DTMF1 OE
PIO3	PCS4#	DTMF2 OE
PIO44	CTSC#	HSUART CTSHU#
PIO45	RTRC#	HSUART RTRHU#

CHIP SELECT ASSIGNMENTS

CHIP SELECTS	DEV ICE	INTERFACE
UCS#	FLASH	16 BIT
LCS#/RAS0#	DRAM	16 BIT
MCS1#/CAS1#	DRAM	16 BIT
MCS2#CAS0#	DRAM	16 BIT
MCS0#	SRAM	16 BIT
PCS1#	79C32	8 BIT
PCS2#	PCNetISA II	8 BIT
PCS3#	TIP	8 BIT

INTERRUPT ASSIGNMENTS

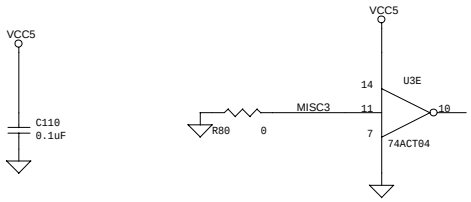
INTERRUPT	DEVICE	POLARITY
INT6	79C32	ACTIVE LOW EDGE
INT2	T7237	ACTIVE LOW EDGE
INT3	PCNetISA II	ACTIVE HIGH EDGE
INT0	TIP ETHERNET	ACTIVE HIGH EDGE
INT7	TIP SERIAL PORT 1	ACTIVE HIGH EDGE
INT8	TIP SERIAL PORT 0	ACTIVE HIGH EDGE
INT4	DTMF 1	ACTIVE HIGH
INT1	DTMF 2	ACTIVE HIGH
INT5	USB	INTERNAL

Design Name
Am186CC ISDN Router (Reference Design) - TIP/PIO/Termination

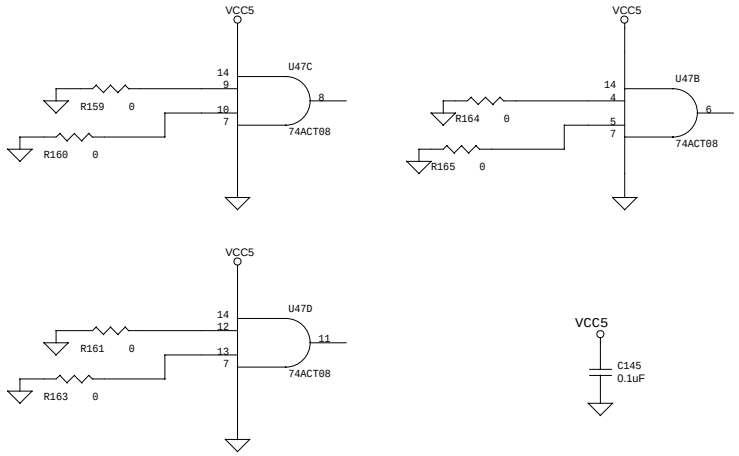
Size	Schematic Sheet Name	Rev
16x125	TIP_PIO_TERMINATION.SCH	2.1

Date: Tuesday, July 20, 1999 Sheet 13 of 14

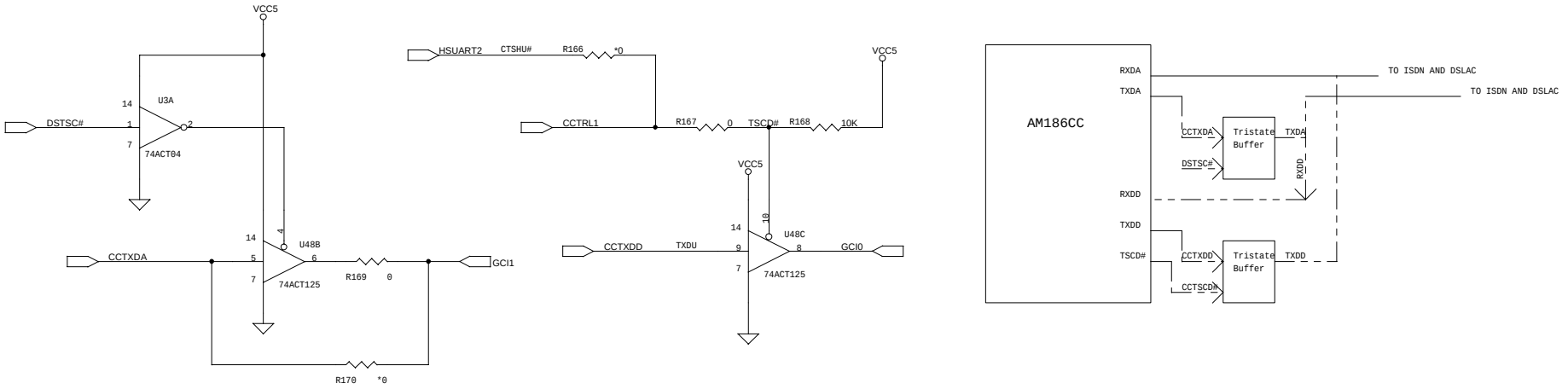
74ACT04 Connected to VCC5



74ACT08 Connected to VCC5



74ACT125 Connected to VCC5



Design Name: Am186CC ISDN Router (Reference Design) - Miscellaneous		
Size: 16x125	Schematic Sheet Name: MISC.SCH	Rev: 2.1
Date: Monday, August 09, 1999	Sheet 14 of 14	