AMD 186CC/CH/CU

Revision C1 (PRL 4005H) Errata and Documentation Defects/Enhancements

Note: **All Errata in this errata sheet apply to Silicon Revision C1 of the Am186CC/CH/CU.**
All production packages will be marked C1. This errata sheet applies to all parts marked C1.
Note: Am186CC/CH/CU User's Manual Amendment (PID # 21914/1) and Register Set Manual Amendment (PID# 21916/1) are here:
http://www.amd.com/epd/techdocs/index.html

Revision History:
11/29/2000 - Created . (Note: Rev C0 never went to production)
02/21/2001 - Changed Rev Status of erratum #C1-01
Fixed a spelling error in the text of Doc defect #4
Inserted Rev Status on Doc Defects #4 and #5
Added Doc Defect #6
10/26/2001 - Added Doc Defect #7, #8

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Errata:

#C1-01 - /PCM_TSC_A signal generated incorrectly when toggling EN of TSACON

Errata # C1-01	*/PCM_TSC_A signal generated incorrectly when toggling EN of TSACON*			
Revision:	**All**			
Status:	**Affected**			
System Symptom:	**Setup:** HDLC Channel A is configured as Raw PCM Highway and HDLC B is configured as multiplexed PCM mode. The EN bit for channel A (in TSACON) is set to a zero (channel A disabled) while the /PCM_TSC_A signal is low. The /PCM_TSC_A signal will remain low (instead of going high). It will continue to drive the pin low until TSA channel A is re-enabled. The same problem can occur if HDLC channels C or D are configured as multiplexed PCM mode. **Symptom:** The /PCM_TSC_A signal will remain low until HDLC Channel A is enabled again. When the EN bit for Channel A (in TSACON) is set to one (channel A enabled), the /PCM_TSC_A signal will go high.			
Errata Description:	When the TSA for HDLC Channel A is disabled, the /PCM_FSC_A clock is disabled, preventing the signal on /PCM_TSC_A from being updated to allow it to drive high.			
HW / SW Work Around:	**1.** Disable the TSA for channel x (where x is B, C, or D) in the TSxCON register, by setting the EN bit to a zero. **2.** Program the TSA channel x BPSTART field in the TSxSTART register with a value that exceeds the maximum bit position possible for the time division multiplexed (TDM) frame. **3.** Enable the TSA for channel x in the TSxCON register by setting the EN bit. **4.** This procedure will allow /PCM_TSA_A to go high. There will be no data comming from this channel x even though it is enabled.			

Documentation Defects/Enhancements:

1. AM186/AM188 Instruction Set Manual PID # 21267A
Page 4-17 change the SF Flag bit settings as follows:
SF=1 if result is 0 or positive - (should be SF = 0)
SF=0 if result is negative - (should be SF = 1)

2. Instruction Set Manual - MOV Instruction Clock Count Incorrect
On page 4-153 of the "Am186 and Am188 Family Instruction Set Manual", the MOV instruction is discussed. The first 4 line items with the MOV instruction, list incorrect clock cycles to execute the instruction. The correct # of cycles for specific MOV instruction types is listed below.

Form :	**Opcode**	**Description:**	**Am186**	**Am188**
MOV r/m8,r8	88/r	Copy register to r/m byte	2/12	2/12
MOV r/m16,r16	89/r	Copy register to r/m word	2/12	2/16
MOV r8,r/m8	8A/r	Copy r/m byte to register	2/9	2/9
MOV r16,r/m16	8B/r	Copy r/m word to register	2/9	2/13

3. Available New Documents:
Am186CC/CH/CU Microcontrollers Register Set Manual Amendment #21916b-1 February 2000
Am186CC/CH/CU Microcontrollers User's Manual Amendment #21914b-1 February 2000
For all other documentation available, please see: http://www.amd.com/epd/techdocs/index.html

4. UART/HSUART Data Write to Shift Register

Documentation Update	*Data Write to Shift Register is based off the Divided clock in LSUART/HSUART*
System Symptom:	Two back to back data byte writes cannot safely be written to the LS/HS Uart hold ing register when the Transmitter Empty bit (TEMT) is set. This breaks compatibil ity with previous 186 parts where it has always been safe to write two bytes of data to the transmitter when TEMT bit is set. Note: This applies to HS UART only when the txt FIFO is disabled.
Description Not covered in Documentation:	Data written to the transmit holding register for the UART/HSUART is moved into the shift register based on the divided clock rather than on the processor clock. This means that, when TEMT is active, data written to the holding register does not move into the shift register for one full bit time.
HW / SW Work Around not covered in documentation:	Do not perform back to back writes to the Txt holding reg when the TEMT bit is set. Wait for the THRE (transmit holding register empty) bit to be set before writing the next data byte.

5. Smart DMA Ring Buffer Reads/Writes do not Function Correctly

Documentation Update	*Smart DMA Ring Buffer Reads/Writes do not Function Correctly when Rings are Located in 8 bit SRAM*
System Symptom:	Setup Using 8 bit SRAM for Smart DMA Ring Buffer memory. Symptom: Smart DMA data transfers do not occur at all OR they are transferred to/from the wrong addresses.
Description not covered in documentation:	When the Smart DMA Ring Buffers are located in 8 bit memory, the Descriptor Reads and/or Writes to this buffer area are not done correctly. Instead of two 8 bit transfers only one 16 bit transfer occurs which results in garbage being read or written into the upper 8 bits of the descriptor word. The Smart DMA controller was architected to ONLY perform 16 bit Ring buffer reads/writes. Memory size is not accounted for and assumed to be 16 bit. **NOTE:** If ONLY the Data buffers (not the Ring buffers) are located in 8 bit memory the transfers work fine. This ONLY affects the Ring memory access.
HW / SW Work Around not covered in documentation:	Work Around Do not Use 8 bit SRAM for Smart DMA. Use 16 bit DRAM or SRAM.

6. Number of Interrupts Supported by Am186CH and CU

Change the following statements in the 5th paragraph on page 7-1 of the User's Manual.

1. In the 2nd Sentence regarding the CH:
From: 14 internal maskable interrupts To: 13 internal maskable interrupts
2. In the 3rd sentence regarding the CU:
From: 13 internal maskable interrupts To: 12 internal maskable interrupts

7. Data Sheet (186CC PID # 21915B) – page 22 – TMROUT0 and TMROUT1 pin descriptions correction

Page 21 for Am186CH Data Sheet (PID # 22024B) and Am186CU Data Sheet (PID # 22025B)

Page	Item	Original Text	Change To	Comment
22	[TMROUT1] [TMROUT0] Last sentence.	[TMROUT1]-[TMROUT0] are three-stated during bus-hold or reset conditions.		Remove

8. Data Sheet (186CC PID # 21915B) – page 14 and 16 – ARDY and SRDY pin description clarification

Page 13 and 16 for Am186CH Data Sheet (PID # 22024B) and Am186CU Data Sheet (PID # 22025B)

Page	Item	Original Text	Change To	Comment
14	ARDY Last paragraph	If the system does not use ARDY, tie the pin low to yield control to SRDY.	If the system does not use ARDY, tie the pin low to yield control to SRDY. **When ARDY is configured as PIO8, the internal SRDY signal is driven low.**	Clarification
16	SRDY Last paragraph	If the system does not use SRDY, tie the pin Low to yield control to ARDY.	If the system does not use SRDY, tie the pin Low to yield control to ARDY. **When SRDY is configured as PIO35, the internal SRDY signal is driven low.**	Clarification