Introduction

DRAMs may be supplied on modules known as SIMMs, DIMMs, SO DIMMs or IC DRAM cards. These assemblies are designed in a well-defined industry standard format. There are significant advantages to the system designer of using these modules rather than unique assemblies of DRAMs.

1. Most personal computers, workstations and other computer-based systems require low-cost customer upgradeable memory, ease of repair and, or variable-base memory sizes (for different models). Because DRAM modules are designed to a JEDEC standard, they and their associated connectors are widely available from a variety of vendors. The end-user can easily acquire memory upgrades from the original system manufacturer or from a large number of specialized suppliers. These “user friendly” upgrades are easily installed, changed or removed without extensive training.
2. The use of industry standard DRAM Modules enables the system supplier to design systems that will be compatible with higher density DRAM technology as it becomes available.
3. No viable method of socketing TSOP DRAM packaging exists. An external carrier such as a DRAM module is necessary.
4. DRAM modules are configured to support multiple memory subsystem architectures such as Non-parity, Parity, and ECC.
5. DRAM module connectors can consume less system board or adapter card real estate than directly attaching individual chips, thus providing potential density increases.

Module Descriptions

The IBM Microelectronics Division offers a broad range of industry-standard DRAM modules. The IBM DRAM module data books include specifications for current offerings:

72 pin Single-Inline-Memory Modules (SIMMs)

72-pin SIMMs are popular 5V-only, industry standard assemblies with functionally equivalent (redundant) contacts on both sides of the card. Capacity ranges from 1 to 32MB. They have 32, 36 or 40 data bits in 4-byte wide data busses and are constructed with 1 to 16Mb SOJ or TSOP-packaged DRAMs. They are 4.25 inches wide and vary in height (generally 1 inch). Presence Detect pins provide speed and density information.

168 pin Dual-Inline-Memory Modules (DIMMs) Buffered

168-pin DIMMs are designed to an industry standard using functionally unique contacts on both sides of the card. Both 3.3 V and 5.0V versions are currently available. Constructed with 4 to 64Mb DRAMs, their capacity is 8 to 256MB with future DIMMs planned to 512MB when assembled with 256Mb DRAM technology. They are 5.25 inches wide and vary in height from 1 to 2.5 inches. Data busses have 64, 72 or 80 data bits for non-parity, parity or ECC applications. Eight buffered Presence Detect pins provide speed and density information while two additional Identity Detect pins provide bus size and self-refresh information.

168 pin Dual-Inline-Memory Modules (DIMMs) Unbuffered

168-pin Unbuffered DIMMs are designed to a new industry standard using functionally unique contacts on both sides of the card. The Unbuffered DIMMs allow the system to take full advantage of the DRAM speed by eliminating the on-card buffers and are intended for systems with “light” loads (1-4 slots), or systems that redrive the signals on the planar. In addition, the Unbuffered DIMMs have a new key and pinout that is common for both DRAM and SDRAM assemblies (advantageous for systems designed for Unified Memory Architecture) and also have a 2-wire serial ID port (I^2C interface) to read the DIMM attributes.

Although the JEDEC standard encompasses 5V and 3.3V, as well as FPM, EDO and SDRAM, IBM’s planned offerings are all 3.3V - in both EDO and SDRAM versions.. Constructed with 4 to 64Mb

DRAMs, their capacity is 8 to 256MB with future DIMMs planned to 512MB when assembled with 256Mb DRAMM technology. They are 5.25 inches wide and vary in height ranging from 1 to 2.5 inches. Data busses have 64, 72, or 80 data bits for non-parity, parity or ECC applications.

72 pin Small-Outline-Dual-Inline-Memory Modules (SO DIMMs)

Useful in mobile or portable computer applications, 72 pin SO (Small Outline) DIMMs are 2.35 inches wide with a variable height ranging from 1 to 1.5 inches. They are constructed with 4 to 64Mb DRAMs (TSOP packages only) and are also extendable to 256Mb DRAMs. Data bus widths are 32 or 36 data bits with capacities of 2MB to 32MB currently available. Seven presence detect pins provide density, organization, addressing, speed and refresh information.

144 pin Small-Outline-Dual-Inline-Memory Modules (SO DIMMs)

Also used in mobile or portable computer applications, 144 pin SO (Small Outline) DIMMs are 2.66 inches wide with a variable height ranging from 1 to 1.5 inches. They are constructed with 16 to 64Mb DRAMs (TSOP packages only) and are also extendable to 256Mb DRAMs. Data bus widths are 64 or 72 data bits with capacities of 8MB to 64MB currently available. A serial presence detect device is used to provide density, organization, addressing, speed, refresh and other miscellaneous information via a two pin (I^2C) interface.

IC DRAM Cards

Also intended for portable applications, IC DRAM cards are fully enclosed rugged assemblies having dimensions equivalent to the popular PCMCIA cards. Similar in architecture to 72 pin SIMMs, these 88 pin cards are 3.37 by 2.13 by 0.130 inches in size and available in 5 or 3.3V configurations. Constructed with 4 to 16Mb TSOP-packaged DRAMs, 32 and 36 bit capacities of 2 to 32MB are offered. Future cards can be based with up to 256Mb technology. Eight Presence Detect pins provide speed and density information.

DRAM Module Pin Assignment Impact

Within each DRAM module type, pinouts vary due to different densities, memory architecture and DRAM chip technology. The application note specific to the module type provides the pin assignment detail needed for the memory system designer to maximize the benefits of using the module. Also included are recommendations on how to use the presence detect pins in system design to enable the system to sense the installed DRAM module type (additional details are found in the individual datasheets).

Prior to designing or specifying any memory subsystem, the designer should become familiar with the timing characteristics of the DRAM modules to be used. Although some DRAM modules appear to be compatible from an architectural and pinout perspective, they may not have identical timing characteristics. Often differences in DRAM modules can be accommodated by careful design of the memory controller but a thorough timing analysis involving all of the anticipated DRAM modules is essential to ensure a robust, reliable, trouble-free system.

Glossary

The following is a mini-glossary of computer memory terms that have a particular significance when used in connection with DRAM modules:

Byte-write

CPUs can perform memory operations involving less than the full data bus width. For example, a so-called 4-byte processor will fetch or store, one, two, three or all four bytes. This requires the DRAM module architecture to support operations such that some bytes may be masked during store operations so that only particular bytes will be accessed, hence the term “byte-write”. Industry Standard DRAM modules designed for byte-write applications, have individual CAS-addressable data bytes.

Check Bits

Extra data bits provided by a DRAM Module to support ECC function. In the case of 4 data bytes, this can be 7 or 8 bits producing 39 or 40 data bits. For 8 data bytes, 8 additional bits results in a total of 72 bits. (Refer to ECC-optimized)

ECC-on-Simm (EOS)

These SIMMs are designed to be plug compatible

with parity based SIMMs but include on-board ECC logic that corrects single-DRAM errors in each byte of SIMM data. System memory data I/O operations via the SIMM are performed on a parity basis, with the on-board ECC features being transparent. These SIMMs provide a convenient way of upgrading a system to fault-tolerant capability without system alterations.

ECC-Optimized

Some systems employed in particular mission-critical applications require memory fault tolerance via ECC (error correction code) techniques. ECC results in memory operations being carried out across all data bits and check bits simultaneously. Since there is no need for byte-write capability, the module's addressing architecture is unique to ECC operations, hence the term, ECC-optimized.

Extended Data Out (EDO) or Hyper Page Mode

Improved form of Fast Page Mode, wherein accessed data remains valid after CAS goes inactive. This feature allows a new access to begin at the next column address, while strobing in the current column address. EDO page cycles are shorter than Fast Page cycles (25ns vs 40ns for a 60ns DRAM). Systems can be designed to be compatible with either, or both types of DRAM modules.

Fast Page Mode

An addressing technique employing variable column addresses strobed in by CAS during an extended RAS cycle resulting in shorter memory cycles. In Fast Page mode cycles, accessed data goes invalid when CAS goes inactive.

Low Power

A growing percentage of systems require low-power memory for portable and "green" or environmentally conscious computers. Low Power implies the use of DRAM chips with extended memory retention, low standby current and often self-refresh capability on the module.

Parity

Parity is generally applied on a byte-wide basis, e.g., a 4-byte SIMM will have four, 8-bit bytes plus one parity bit per each byte. (refer to Byte-write), By necessity, parity, as opposed to a non-parity DRAM modules, have additional DRAM chips and additional cost. Parity is useful to assist in diagnosis of the sources of system problems. This guards against inaccurate data processing and unexplained system hangs.

Presence Detect and ID Pins

Pins defined to permit the interfacing system to derive information such as speed, density, ECC, parity or functional information about each DRAM module plugged into a socket. The information provided by these pins is in accordance with established, JEDEC standards and can be exploited to allow the system to automatically configure the memory system.

Voltage Keying

Some DRAM modules are equipped with special notches, or keys, to ensure that they can only be plugged into systems with the appropriate power supply. 3.3V DRAMs will not work and are subject to damage if plugged into 5V systems.

For more information contact your IBM Microelectronics sales representative or
visit us on World Wide Web at http://www.chips.ibm.com

IBM Microelectronics manufacturing is ISO 9000 compliant.

FormID