FARADAY
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T-52-33-15

Advance Information

FE5000

Enhanced CPU and Peripheral Control Logic

- 100% Hardware (Register Level) and Software Compatible to the IBM* Personal System/2* Models 50 and 60
- Equivalent Functionality of the following:
  - Two 8259 Interrupt Controllers
  - 8254 Timer
  - Watchdog Timer Logic
  - System Board I/O Decode Logic
  - Peripheral Bus Control Generator
  - NMI Generator
  - Error Control Logic
- Operates at CPU Clock Rates to 20 MHz
- Interfaces Directly to the Channel
- 80287 Math Coprocessor Support
- Programmable Option Select (POS) Logic
- Clock Generation Logic for 80287 Math Coprocessor and 8742 Keyboard Controller
- Support for External CMOS RAM for Storage of Configuration Data
- Extended Setup Facility™ (ESF™)
- Low Power 1.25 Micron CMOS Technology
- 132 Lead JEDEC Plastic Quad Flat Pack

As part of the Faraday® FE5400 Chip Set, the FE5000 CPU and Peripheral Control Logic integrated circuit significantly facilitates the design and implementation of IBM PS/2* Model 50 and 60 compatible system boards. By combining functionality normally implemented in 1 gate array and 29 discrete components, the FE5000 decreases design complexity, saves space, reduces system cost, and increases system reliability.

The Extended Setup Facility (ESF) is a fully compatible enhancement that allows designers to easily configure additional functionality (e.g., Winchester Controller, LAN Adapter, Additional Serial Port) on the system board. This facility can help reduce costs and provide system level product differentiation. Figure 1 shows a typical system diagram using the FE5400 Chip Set.

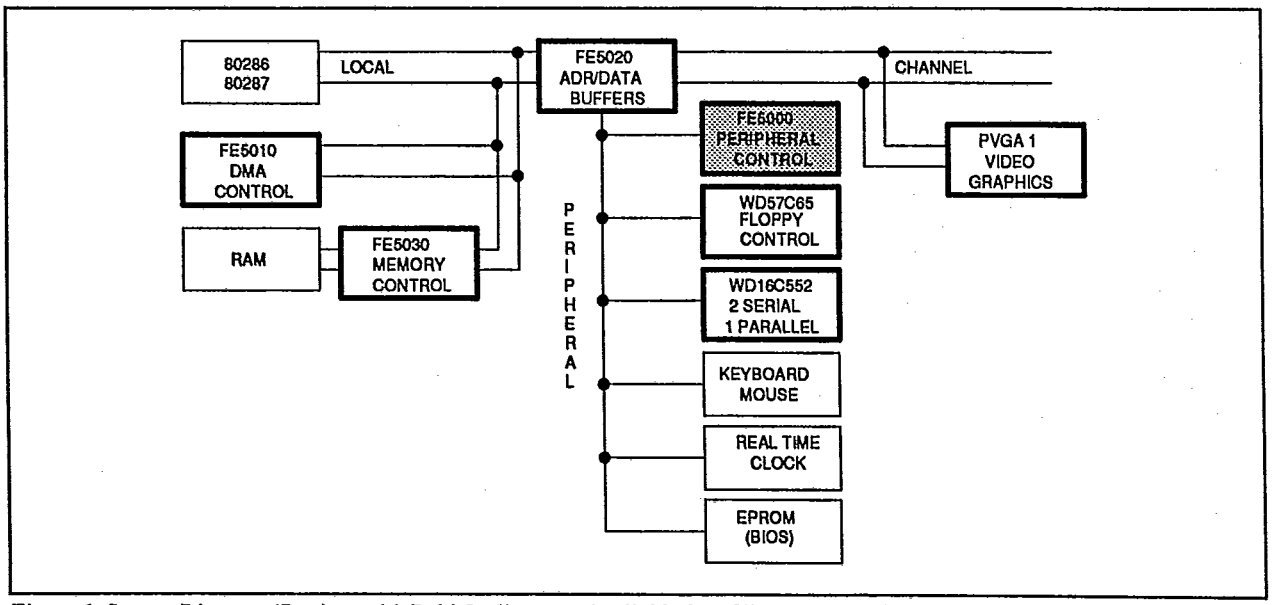

Figure 1. System Diagram (Devices with Bold Outlines are Available from Western Digital Corporation)

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Release 1.0

January 31, 1988

Additional References

IBM PS/2 Model 50/60 Technical Reference Manual
Intel Microprocessor and Peripheral Handbook*

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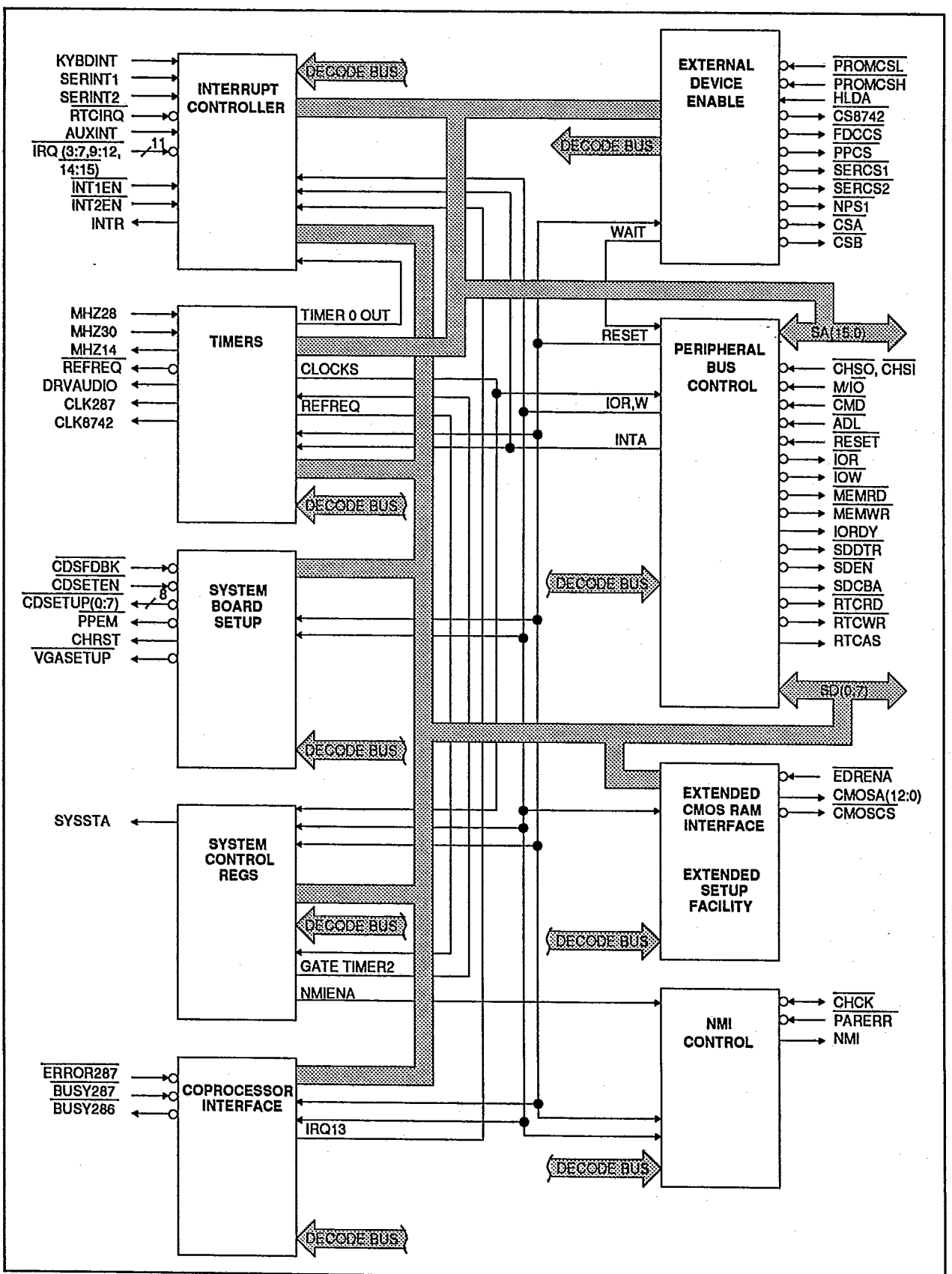


Figure 2. FE5000 Block Diagram

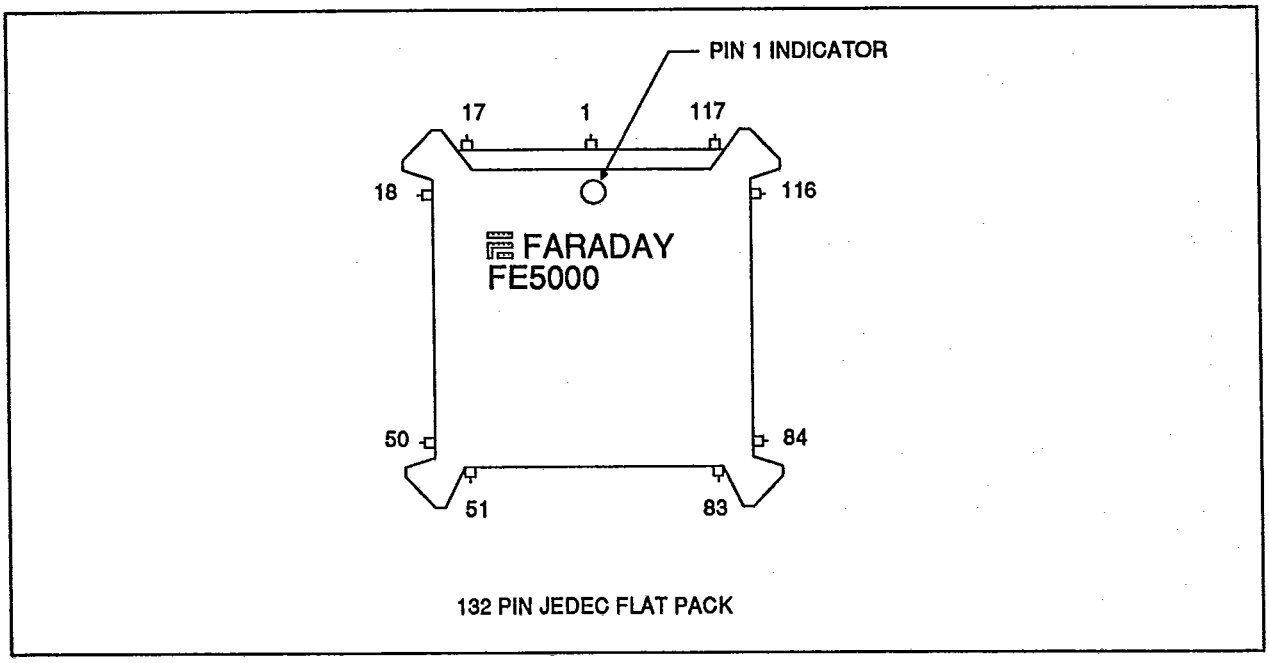


Figure 3. Pin Diagram

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	SD6	34	SA14	67	RESERVED	100	$\overline{\text{RTCWR}}$
2	V_{DD}	35	V_{DD}	68	V_{DD}	101	V_{SS}
3	SD5	36	SA13	69	CMOSA10	102	$\overline{\text{RTCRD}}$
4	RESERVED	37	SA12	70	CMOSA9	103	RTCAS
5	SD4	38	SA11	71	CMOSA8	104	$\overline{\text{IOW}}$
6	SD3	39	SA10	72	CMOSA7	105	$\overline{\text{IOR}}$
7	SD2	40	SA9	73	CMOSA6	106	$\overline{\text{MEMWR}}$
8	RESERVED	41	SA8	74	CMOSA5	107	$\overline{\text{MEMRD}}$
9	SD1	42	SA7	75	CMOSA4	108	CLK287
10	SD0	43	SA6	76	V_{SS}	109	CLK8742
11	V_{SS}	44	SA5	77	CMOSA3	110	SDCBA
12	$\overline{\text{CHCK}}$	45	SA4	78	CMOSA2	111	$\overline{\text{SDEN}}$
13	V_{SS}	46	SA3	79	CMOSA1	112	$\overline{\text{SDDTR}}$
14	$\overline{\text{BUSY287}}$	47	SA2	80	CMOSA0	113	RESERVED
15	$\overline{\text{ERROR287}}$	48	SA1	81	MHZ14	114	CMOSA12
16	$\overline{\text{RESET}}$	49	SA0	82	NMI	115	V_{SS}
17	MHZ28	50	V_{SS}	83	DRVAUDIO	116	CMOSA11
18	$\overline{\text{PARERR}}$	51	$\overline{\text{IRQ11}}$	84	$\overline{\text{SYSSTA}}$	117	$\overline{\text{BUSY286}}$
19	$\overline{\text{CDSETEN}}$	52	$\overline{\text{IRQ10}}$	85	$\overline{\text{CMOSCS}}$	118	$\overline{\text{CSA}}$
20	MHZ30	53	$\overline{\text{IRQ9}}$	86	V_{DD}	119	$\overline{\text{CSB}}$
21	SERINT2	54	$\overline{\text{RTCIRQ}}$	87	INTR	120	$\overline{\text{CMDBUF}}$
22	SERINT1	55	$\overline{\text{IRQ7}}$	88	V_{SS}	121	$\overline{\text{CDSETUP0}}$
23	$\overline{\text{INT2EN}}$	56	$\overline{\text{IRQ6}}$	89	$\overline{\text{NPS1}}$	122	$\overline{\text{CDSETUP1}}$
24	$\overline{\text{INT1EN}}$	57	$\overline{\text{IRQ5}}$	90	$\overline{\text{PPCS}}$	123	V_{DD}
25	AUXINT	58	$\overline{\text{IRQ4}}$	91	$\overline{\text{SERCS2}}$	124	$\overline{\text{CDSETUP2}}$
26	$\overline{\text{DACK}}$	59	$\overline{\text{IRQ3}}$	92	$\overline{\text{SERCS1}}$	125	V_{SS}
27	$\overline{\text{PROMCS}}$	60	KYBDINT	93	$\overline{\text{FDCCS}}$	126	$\overline{\text{CDSETUP3}}$
28	HLDA	61	M/$\overline{\text{IO}}$	94	$\overline{\text{CS8742}}$	127	$\overline{\text{CDSETUP4}}$
29	$\overline{\text{IRQ15}}$	62	$\overline{\text{CMD}}$	95	$\overline{\text{PPEM}}$	128	$\overline{\text{CDSETUP5}}$
30	$\overline{\text{IRQ14}}$	63	$\overline{\text{ADL}}$	96	$\overline{\text{VGASETUP}}$	129	$\overline{\text{CDSETUP6}}$
31	$\overline{\text{EDRENA}}$	64	$\overline{\text{CHS1}}$	97	IORDY	130	$\overline{\text{CDSETUP7}}$
32	$\overline{\text{IRQ12}}$	65	$\overline{\text{CHS0}}$	98	$\overline{\text{REFREQ}}$	131	CHRST
33	SA15	66	$\overline{\text{CDSFDBK}}$	99	V_{DD}	132	SD7

1.0 PIN DESCRIPTION

PIN NO.	NAME	TYPE	FUNCTION
			INTERRUPT CONTROLLER
60	KYBDINT	I	KEYBOARD INTERRUPT—Driven by the system keyboard controller (8742).
22	SERINT1	I	SERIAL INTERRUPT 1—Internally switched with SERINT2 to share IRQ3 and IRQ4 under software control. The program control register (PCR) and setup register 0102H are used to assign the serial interrupt signals.
21	SERINT2	I	SERIAL INTERRUPT 2—Internally switched with SERINT1 to share IRQ3 and IRQ4 under software control. The program control register (PCR) and setup register 0102H are used to assign the serial interrupt signals.
54	$\overline{\text{RTCIRQ}}$	I	$\overline{\text{REAL TIME CLOCK INTERRUPT}}$—Generated by the system Real Time Clock module.
25	AUXINT	I	AUXILIARY INTERRUPT—Driven by the system keyboard controller (8742).
59 58 57 56 55 53 52 51 32 30 29	$\overline{\text{IRQ3}}$ $\overline{\text{IRQ4}}$ $\overline{\text{IRQ5}}$ $\overline{\text{IRQ6}}$ $\overline{\text{IRQ7}}$ $\overline{\text{IRQ9}}$ $\overline{\text{IRQ10}}$ $\overline{\text{IRQ11}}$ $\overline{\text{IRQ12}}$ $\overline{\text{IRQ14}}$ $\overline{\text{IRQ15}}$	I	$\overline{\text{INTERRUPT REQUESTS}}$—Asynchronous inputs that may be shared by other interrupting devices.
24	$\overline{\text{INT1EN}}$	I	$\overline{\text{SERIAL INTERRUPT 1 ENABLE}}$—System generated programmable output that gates interrupt signal SERINT1 from the associated serial device. This line may be left open to enable the interrupt.
23	$\overline{\text{INT2EN}}$	I	$\overline{\text{SERIAL INTERRUPT 2 ENABLE}}$—System generated programmable output that gates interrupt signal SERINT2 from the associated serial device. This line may be left open to enable the interrupt.
87	INTR	O	INTERRUPT—Drives the system CPU interrupt pin.
			TIMERS
17	MHZ28	I	28.636 MHz—Basic clock used for all FE5000 internal functions (timers, wait generator, bus interface logic).
20	MHZ30 (optional)	I	30.0 MHz—This input drives the coprocessor and keyboard clock outputs appropriately. See below.
81	MHZ14	O	14.318 MHz—This clock output drives the Channel OSC line.
98	$\overline{\text{REFREQ}}$	O	$\overline{\text{REFRESH REQUEST}}$—This timer output is used to request a refresh cycle by the CACP and DMA controller.
83	DRVAUDIO	O	DRIVE AUDIO—This output drives the audio summing network shared by the Channel audio line. This output is Timer 2 OUT gated by Control Port B (0061H) bit 0.
108	CLK287	O	287 CLOCK—This is a 33% duty cycle clock derived from the MHZ30 clock input divided by 3. Its specification is suitable for the 80287 math coprocessor.
109	CLK8742	O	8742 CLOCK—This clock drives the 8742. It is derived from the 30 MHz clock input divided by 3.

O = Output, I = Input, IO = Bidirectional

PIN NO.	NAME	TYPE	FUNCTION
			SYSTEM BOARD SETUP
66	$\overline{\text{CDSFDBK}}$	I	$\overline{\text{CARD SELECTED FEEDBACK}}$—This Channel signal indicates that the addressed slave is present.
19	$\overline{\text{CDSETEN}}$	I	$\overline{\text{CARD SETUP ENABLE}}$—This signal is the timing decode for 0100H-0107H from the FE5010.
121 122 124 126 127 128 129 130	$\overline{\text{CDSETUP0}}$ $\overline{\text{CDSETUP1}}$ $\overline{\text{CDSETUP2}}$ $\overline{\text{CDSETUP3}}$ $\overline{\text{CDSETUP4}}$ $\overline{\text{CDSETUP5}}$ $\overline{\text{CDSETUP6}}$ $\overline{\text{CDSETUP7}}$	O	$\overline{\text{CARD SETUP}}$—Each signal drives a Channel slot.
95	$\overline{\text{PPEM}}$	O	$\overline{\text{PARALLEL PORT EXTENDED MODE}}$—When asserted, this signal puts the parallel port into Extended (bidirectional) Mode.
131	CHRST	O	CHANNEL RESET—This software generated signal resets all Channel resident adapters and system board IO devices only. It is located in register 0096H bit 7.
96	$\overline{\text{VGASETUP}}$	O	$\overline{\text{VGA SETUP}}$—Tells the PVGA device to enter Setup Mode.
			SYSTEM CONTROL REGISTERS
84	$\overline{\text{SYSSTA}}$	O	$\overline{\text{SYSTEM STATUS}}$—This signal is used to drive a system status LED.
			COPROCESSOR INTERFACE
15	$\overline{\text{ERROR287}}$	I	$\overline{\text{ERROR 287}}$—Driven by the coprocessor, this signal indicates that the coprocessor has encountered an error condition. This condition causes an interrupt (13H) to be issued and holds the BUSY 286 signal in the busy state. The busy and interrupt are cleared by issuing an 8 bit IO write command to location 00F0H with data equal to 00H.
14	$\overline{\text{BUSY287}}$	I	$\overline{\text{BUSY 287}}$—Driven by the coprocessor, this signal indicates the coprocessor is currently executing a command.
117	$\overline{\text{BUSY286}}$	O	$\overline{\text{BUSY 286}}$—Indicates the coprocessor is currently executing a command.
			EXTERNAL DEVICE ENABLE
28	HLDA	I	HOLD ACKNOWLEDGE—This line indicates when the CPU has given the system MPU local bus to another master (Channel bus master or DMA controller). It is used to prevent non-system CPU access to locations 0000–00FFH in the FE5000.
27	$\overline{\text{PROMCSL}}$	I	$\overline{\text{PROMPT CHIP SELECT}}$—Is located in addresses E0000H to FFFFFH. The line is used by the Wait/Ready logic to control the bus cycle length for PROM accesses. It is tied high (using 10K ohms), and the system EPROM is connected to the FE5030.
26	$\overline{\text{DACK}}$		$\overline{\text{DMA ACKNOWLEDGE}}$—This signal starts the Wait/Ready logic when the DMA accesses the floppy controller.
94	$\overline{\text{CS8742}}$	O	$\overline{\text{CHIP SELECT 8742}}$—This signal is the chip select to the keyboard/auxiliary device controller.
93	$\overline{\text{FDCCS}}$	O	$\overline{\text{FLOPPY DISK CONTROLLER CHIP SELECT}}$—This signal is the chip select to the floppy disk controller.
90	$\overline{\text{PPCS}}$	O	$\overline{\text{PARALLEL PORT CHIP SELECT}}$—This signal is the chip select to the parallel port controller.

O = Output, I = Input, IO = Bidirectional

PIN NO.	NAME	TYPE	FUNCTION
92	$\overline{\text{SERCS1}}$	O	$\overline{\text{SERIAL CHIP SELECT 1}}$—This signal is the chip select for the first serial port controller.
91	$\overline{\text{SERCS2}}$	O	$\overline{\text{SERIAL CHIP SELECT 2}}$—This signal is the chip select to second serial port controller.
89	$\overline{\text{NPS1}}$	O	$\overline{\text{NUMERIC PROCESSOR SELECT}}$—This signal is the chip select to the math coprocessor.
118	$\overline{\text{CSA}}$	O	$\overline{\text{CHIP SELECT A}}$—This signal is a software programmable chip select.
119	$\overline{\text{CSB}}$	O	$\overline{\text{CHIP SELECT B}}$—This signal is a software programmable chip select.
			PERIPHERAL BUS CYCLE
10 9 7 6 5 3 1 132	SD0 SD1 SD2 SD3 SD4 SD5 SD6 SD7	IO	SYSTEM DATA—These bidirectional lines are the low byte of data from the Channel data bus (buffered).
49 48 47 46 45 44 43 42 41 40 39 38 37 36 34 33	SA0 SA1 SA2 SA3 SA4 SA5 SA6 SA7 SA8 SA9 SA10 SA11 SA12 SA13 SA14 SA15	I	SYSTEM ADDRESS—These 16 address lines are used to decode the appropriate locations of the system CPU 64K IO space.
65 64 61	$\overline{\text{CHS0}}$ $\overline{\text{CHS1}}$ M/$\overline{\text{IO}}$	I	$\overline{\text{CHANNEL STATUS}}$ and MEMORY $\overline{\text{I/O}}$—These three lines encode the Channel bus cycle type information.
62	$\overline{\text{CMD}}$	I	$\overline{\text{COMMAND}}$—This signal defines when data to or from the Channel is valid.
120	$\overline{\text{CMDBUF}}$	O	$\overline{\text{COMMAND BUFFERED}}$—This signal is a buffered $\overline{\text{COMMAND}}$ output provided to latch the peripheral address bus externally.
63	$\overline{\text{ADL}}$	I	$\overline{\text{ADDRESS DECODE LATCH}}$—This line is used to set the direction control lines for the IO data bus.
16	$\overline{\text{RESET}}$	I	$\overline{\text{RESET}}$—This signal initializes all the internal logic to a power on state.
105 104 107 106	$\overline{\text{IOR}}$ $\overline{\text{IOW}}$ $\overline{\text{MEMRD}}$ $\overline{\text{MEMWR}}$	O	$\overline{\text{I/O READ}}$, $\overline{\text{I/O WRITE}}$, $\overline{\text{MEMORY READ}}$, and $\overline{\text{MEMORY WRITE}}$—These signals comprise the command information for peripheral bus cycles and track the Channel cycle.

O = Output, I = Input, IO = Bidirectional

PIN NO.	NAME	TYPE	FUNCTION
97	IORDY	O	I/O READY—This signal indicates the FE5000 is finished with the current bus cycle. It is deactivated to extend the current system MPU bus cycle.
112 111 110	$\overline{\text{SDDTR}}$ $\overline{\text{SDEN}}$ SDCBA	O O O	$\overline{\text{SD BUS DATA TRANSMIT/READ}}$, $\overline{\text{SD BUS ENABLE}}$, SD BUS CLOCK (latches when clock is low)—These three lines control the address and data buffer latches for the peripheral bus. When $\overline{\text{SDDTR}}$ is asserted the bus cycle is a read.
103	RTCAS	O	REAL TIME CLOCK ADDRESS SELECT—This signal latches the address into the Real Time Clock module.
102 100	$\overline{\text{RTCRD}}$ $\overline{\text{RTCWR}}$	O	$\overline{\text{REAL TIME CLOCK READ/WRITE}}$—These two lines are the command lines to the Real Time Clock Module.
			EXTENDED CMOS RAM INTERFACE
80 79 78 77 75 74 73 72 71 70 69 116 114	CMOSA0 CMOSA1 CMOSA2 CMOSA3 CMOSA4 CMOSA5 CMOSA6 CMOSA7 CMOSA8 CMOSA9 CMOSA10 CMOSA11 CMOSA12	O	CMOS ADDRESS—These 13 lines are used to address the Extended CMOS RAM.
85	$\overline{\text{CMOSCS}}$	O	$\overline{\text{CMOS CHIP SELECT}}$—This line is used to select the Extended CMOS RAM.
31	$\overline{\text{EDRENA}}$	I	$\overline{\text{ESF DATA REGISTER PORT ENABLE}}$—This signal from the FE5010 indicates that the ESF Data Register is being read or written.
			NMI CONTROL
12	$\overline{\text{CHCK}}$	IO	$\overline{\text{CHANNEL CHECK}}$—This signal is the Channel error indication. It is driven by bus resident adapters. During a bus master DRAM cycle the system board drives this line if a parity error occurs.
18	$\overline{\text{PARERR}}$	I	$\overline{\text{PARITY ERROR}}$—This signal is the output of the DRAM controller parity generator.
82	NMI	O	NON-MASKABLE INTERRUPT—This signal is "wire OR" with the FE5010 NMI signal to drive the system CPU NMI line.
			MISCELLANEOUS
2,35,68, 86,99,123	V_{DD}	I	+5 V Power Supply
11,13,50, 76,88,101, 115, 125	V_{SS}	I	0V Ground
4,8, 67,113	RESERVED	—	NO CONNECT—These pins must be left open.

O = Output, I = Input, IO = Bidirectional

The FE5400 IO map is shown in Table 1.

ADDRESS RANGE	LOCATION	FUNCTION
0000 to 000FH	FE5010	DMA Controller chan 0-3 [1]
0018H	FE5010	Extended Function Register [1]
001AH	FE5010	Extended Function Execute [1]
0020 to 0021H	FE5000	Interrupt Controller 1
0040,0042-0044,0047H	FE5000	System Timers
0060H	FE5000	Keyboard Data Port
0061H	FE5000	System Control Port B
0064H	FE5000	RD=Kybd status, WR=Kybd command
0070H	FE5000	RTC/CMOS address register, NMI Mask
0071H	FE5000	RTC/CMOS data port
0074H	FE5000	EAR0 Extended CMOS RAM; ESF
0075H	FE5000	EAR1 Extended CMOS RAM
0076H	FE5000	Extended CMOS RAM data port
0081 to 0083, 0087H	FE5010	DMA Page Registers (0-3) [1]
0089 to 008B, 008FH	FE5010	DMA Page Registers (4-7) [1]
0090H	FE5010	AC [1]
0091H	FE5000	Card Selected Feedback
0092H	FE5000	System Control Port A
0094H	FE5000	System Board Setup
0096,0097H	FE5000	POS, Channel Connector Select
00A0 to 00A1H	FE5000	Interrupt Controller 2
00C0 to 00DFH	FE5000	DMA Controller (even only) [1]
00F0H	FE5000	Coprocessor clear busy
00F1H	FE5000	Coprocessor reset
00F8 to 00FFH	FE5000	Coprocessor
0100, 0101H	FE5000	System ID
0102 to 0107H	FE5000	System Board Configuration (POS)
0278 to 027BH	FE5000	Parallel Port 3
02F8 to 02FFH	FE5000	Alternate Serial Port
0378 to 037BH	FE5000	Parallel Port 2
03BC to 03BFH	FE5000	Parallel Port 1
03B4,03B5,03BA,03C0-03C5H	PVGA1	Video Subsystem [2]
03CE,03CF,03D4,03D5,03DAH	PVGA1	Video Subsystem [2]
03C6 to 03C9H	PVGA1	Video DAC [2]
03F0 to 03F7H	FE5000	Diskette Drive Controller
03F8 to 03FFH	FE5000	Primary Serial Port
0700H	FE5010	ESF Data Register (Default)
[1] No Channel cycle is generated on these IO addresses.		[2] IO location 03C3H (PVGA Enable Register) is in FE5010.

Table 1. System Level I/O Map

2.0 INTERRUPT CONTROLLER

The Interrupt Controller is functionally compatible with two Intel 8259 controllers cascaded together. It operates in level-sensitive mode and controls 16 levels of interrupts; 5 internal and 11 system interrupts. ***The edge trigger mode is not available.*** Any or all of the interrupts may be masked. The non-maskable interrupt may be masked by setting register 0070H bit 7.

Interrupt controller #1 is the master controller and is located at I/O space 0020H and 0021H. Interrupt controller #2 is the slave and is located at I/O space 00A0H and 00A1H. Interrupt request 2 (IRQ2) of interrupt controller #1 is used to cascade the two controllers (see Fig. 4).

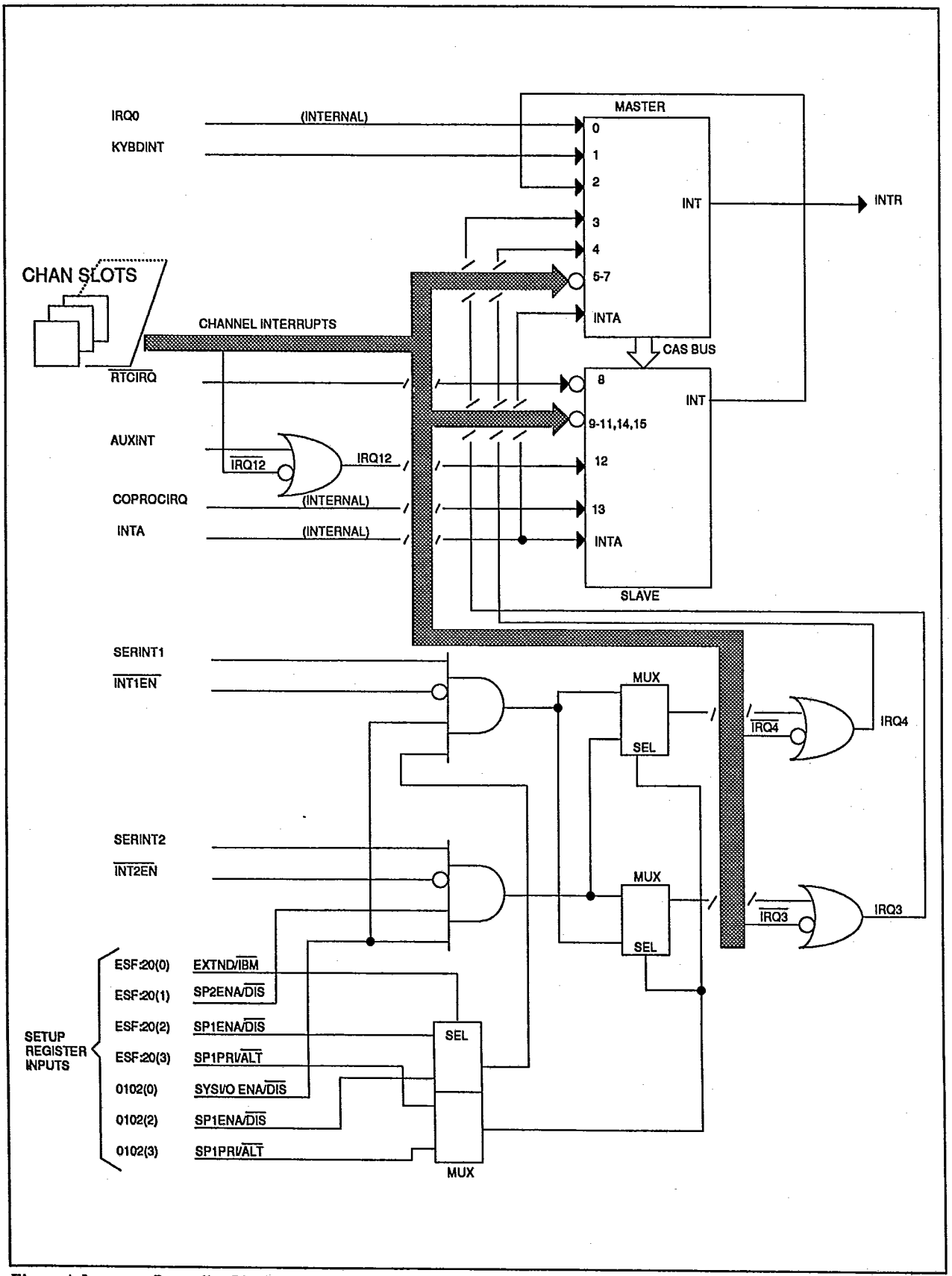


Figure 4. Interrupt Controller Block Diagram

SYSTEM SOURCE	CHANNEL	LEVEL
Timer	—	0 [1]
Keyboard Port	—	1
Cascade	—	2 [1]
Alt. Serial Port	IRQ3	3
Pri. Serial Port	IRQ4	4
—	IRQ5	5
Floppy Disk	IRQ6	6
Parallel Port	IRQ7	7
RTC	—	8
PVGA	IRQ9	9
—	IRQ10	10
—	IRQ11	11
Mouse Port (AUXINT)	IRQ12	12
Coprocessor	—	13 [1]
—	IRQ14	14
—	IRQ15	15
[1] This interrupt is internally generated in the FE5000.		

Table 2. Interrupt Sharing

Interrupts may be shared by more than one hardware interrupt requester. Table 2 shows the interrupt assignments in a system environment.

AUXINT is an active high input that is ORed with IRQ12 from the Channel. It is treated exactly like an IRQ12 interrupt.

SERINT1 is an active high interrupt from Serial Port 1 (SP1). SERINT1 is masked by $\overline{\text{INT1EN}}$ which must be low for SERINT1 to be detected. SERINT1 is ORed with IRQ3 or IRQ4 depending on how it is programmed. If SP1 is enabled (see SYSTEM BOARD SETUP, Section 4.0), SERINT1 is treated as IRQ3 when SP1 is programmed to alternate addresses 02F8–02FFH, or IRQ4 when SP1 is programmed to primary addresses 03F8–03FFH.

SERINT2 is an active high interrupt from Serial Port 2 (SP2). SERINT2 is masked by $\overline{\text{INT2EN}}$ which must be low for SERINT2 to be detected. SERINT2 is ORed with IRQ3 or IRQ4 depending on how it is programmed. If SP2 is enabled (see Peripheral Configuration Register, Section 9.2.3), SERINT2 is treated as IRQ3 when SP2 is programmed to primary addresses 03F8–03FFH, or IRQ4 when SP2 is programmed to alternate addresses 02F8–02FFH.

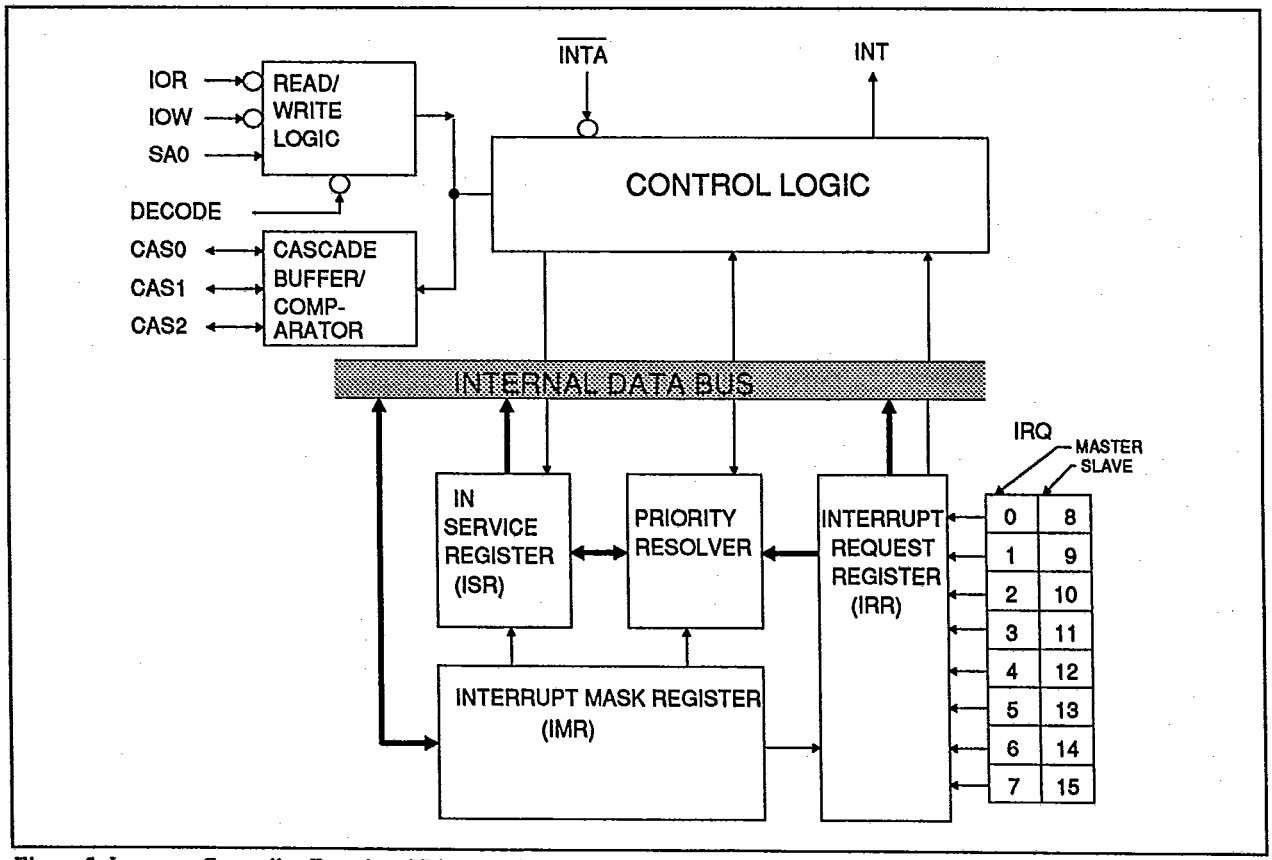


Figure 5. Interrupt Controller Functional Diagram (Typical Master or Slave)

2.1 INTERRUPT CONTROLLER OPERATION

Figure 5 is a functional diagram for each interrupt controller in the FE5000. It provides an operational representation of how each controller works.

2.1.1 Interrupt Request Register (IRR) and In-Service Register (ISR)

Interrupts are handled by the IRR and the ISR. The IRR stores all the interrupt levels that request service and the ISR stores all the interrupt levels that are being serviced.

2.1.2 Priority Resolver

This function decodes the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during the INTA cycle.

2.1.3 Interrupt Mask Register (IMR)

The IMR stores the bits that mask selected interrupt lines. Masking a higher priority input does not affect lower priority interrupt request lines.

2.1.4 Read/Write Control Logic

This function accepts commands from the CPU and allows Interrupt Controller status to be read on the Data Bus. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers that store the various control formats for device operation.

2.1.5 Cascade Buffer/Comparator

This function stores and compares the ID of the slave controller. In the FE5000 Interrupt Controller configuration, the CAS bus is an output from the master and an input to the slave. When a slave request line is activated and acknowledged, the master sends the ID (fixed at 2) of the slave onto the CAS bus. This enables the slave to send its preprogrammed subroutine address onto the Data Bus during the second INTA cycle. All handshaking is handled internally.

2.2 INTERRUPT SEQUENCE

The events of an interrupt in a system environment are as follows:

1. One or more interrupts arrive from a peripheral device which sets the corresponding bit(s) in the IRR.

2. The request is evaluated and if the interrupt has not been masked, it is passed to the priority circuit and the Interrupt Controller sends an interrupt (INTR) to the CPU.

3. The CPU responds to the interrupt with an INTA cycle.

4. When the INTA is received, the priority is frozen and the highest priority ISR bit is set. The Interrupt Controller does not drive the Data Bus during this cycle.

5. The CPU initiates another INTA cycle that causes the Interrupt Controller to send an 8-bit vector to the CPU (see Figure 12). The master or slave may be programmed to send the byte of data. As long as the ISR bit is set, all interrupts at the same level or lower are inhibited (in Special Mask Mode (SMM), only interrupts at the same level are inhibited). If a higher priority interrupt occurs during an interrupt service routine, it is only acknowledged if the CPU internal interrupt enable has been re-enabled.

When the slave issues an interrupt, other interrupts from the slave are locked out. If it is desired to preserve priority in the slave (i.e. allow higher interrupts to occur when a lower interrupt is being serviced), Special Fully Nested Mode (SFNM) should be programmed in the master (see ICW4).

6. At the end of the second INTA cycle, one or two end of interrupt (EOI) commands must be issued to complete the interrupt; one for the master and the other for the slave. This clears the appropriate bit in the ISR.

If SFNM is programmed, send a Non-Specific EOI to the slave and check the ISR to see if any other interrupts are active. If there are none, a Non-Specific EOI should be sent to the master.

2.3 END OF INTERRUPT (EOI)

There are three EOI commands: Specific, Non-Specific, and Automatic. When the Interrupt Controller is programmed to operate in modes that preserve fully nested interrupts, the CPU can determine which ISR bit to reset on EOI since the current highest priority ISR bit is necessarily the last level acknowledged and serviced. In this case a Non-Specific EOI can be issued. In Special Mask Mode, an ISR bit that is masked in the IMR is not cleared by a Non-Specific EOI.

When the fully nested structure is not preserved, a Specific EOI must be issued at the end of the interrupt service routine which includes the ISR bit to reset. Specific and Non-Specific EOI are issued with OCW2.

Automatic EOI (AEOI) automatically occurs on the trailing edge of the second INTA cycle. AEOI can only be used for the master; not the slave. AEOI is set with ICW4.

2.4 POLLED MODE

The Interrupt Controller may also be operated in a polled mode. In this mode interrupts should be masked by the CPU. An interrupt is detected when software issues a poll command. The poll command is issued by setting P = 1 in OCW3. This results in an equivalent INTA cycle during the next read operation to the Interrupt Controller (i.e., IOR = 0, DECODE = 0) which sets the IS bit, if a request was made, and allows the priority level to be read (see Figure 6). The IRR remains frozen until the read cycle is complete. At the end of the process, Polled Mode is reset to 0.

D7	D6	D5	D4	D3	D2	D1	D0
I	—	—	—	—	W2	W1	W0

W0–W2: Binary code of the highest priority level requesting service.
I: Equal to "1" if there is an interrupt.

Figure 6. Interrupt Priority Level Using the Poll Command.

2.5 INTERRUPT PRIORITY

There are three types of interrupt priority: Fixed, Automatic Rotation, and Specific Rotation. Fixed priority is the default condition unless Automatic or Specific Rotation is programmed with OCW2 or Polled Mode is programmed with OCW3. In Fixed Mode, interrupts are fully nested with IRQ0 having the highest priority and IRQ7 the lowest.

2.5.1 Automatic Rotation

Automatic Rotation is useful in applications where a number of interrupting devices have equal priority. In this mode, the last interrupt serviced has the lowest priority. For example, Figure 7 shows the status of the ISR and the corresponding priority status. Once the highest priority interrupt (IRQ4 in Figure 7) is serviced, the priority status changes as shown in Figure 8.

2.5.2 Specific Rotation

Specific Rotation is used to change the lowest priority thus fixing all other priorities. For example, if IRQ4 is programmed to be the lowest priority, then the new priority becomes 5, 6, 7, 0, 1, 2, 3, and 4 with IRQ5 the highest priority and IRQ4 the lowest.

Specific Rotation is programmed with OCW2 in two ways: Rotate on Specific EOI and Set Priority. Note that priority changes can only be made during an EOI command by using the Rotate on Specific EOI.

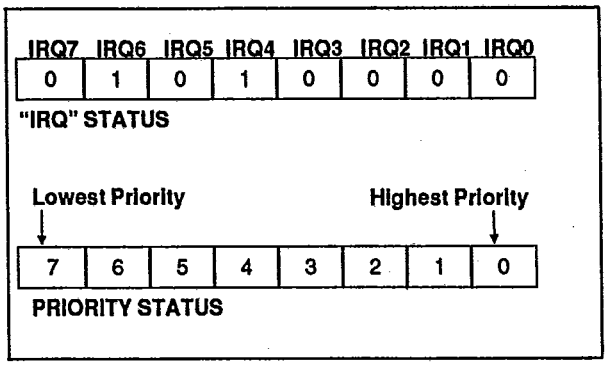


Figure 7. Interrupt Priority Before Automatic Rotation

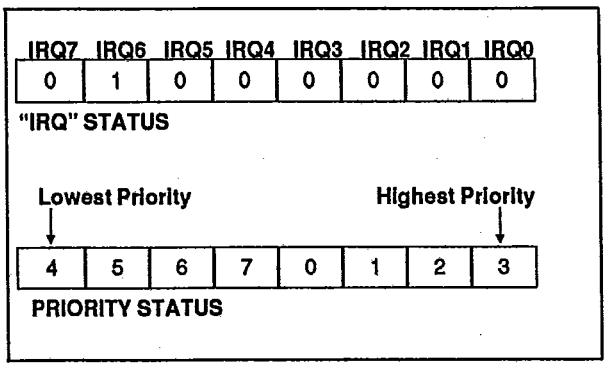


Figure 8. Interrupt Priority After Automatic Rotation

2.6 SPECIAL MASK MODE

Special Mask Mode (SMM) allows the priority structure to be dynamically changed. In SMM, when a bit is masked in OCW1, interrupts are inhibited at that level; all other levels (lower and higher) that are not masked are enabled. Thus selective enabling of interrupts can be accomplished in SMM by changing the IMR. SMM is programmed with OCW3.

2.7 READING REGISTER STATUS

The status of the IRR, and ISR can be read at address 020H (master) and 0A0H (slave). Prior to the read status operation, indicate the register to be read with OCW3. The contents of the selected register can be read again (i.e., no need to write another OCW3 to read the same register) unless Polled Mode is selected.

IMR can be read at address 021H and 0A1H.

2.8 INTERRUPT TRIGGERING

An interrupt request is recognized by a high level on the IRQ input. The interrupt request must be removed before the EOI is issued or before the CPU internal interrupt enable has been re-enabled. Otherwise a "second" interrupt is detected.

The IRQ inputs must remain high until after the falling edge of the first INTA (see Figure 9). If the IRQ goes low before this time, the Interrupt Controller issues an interrupt level 7 vector during the second INTA cycle; thus ignoring the false interrupt. This allows detection of false interrupts caused by spurious noise glitches on the interrupt inputs.

If IRQ7 is needed for other purposes, a false IRQ7 can still be detected by reading the ISR. A normal IRQ7 sets the corresponding ISR bit, a false IRQ7 does not; except when a false IRQ7 occurs during a normal IRQ7. In this case it is necessary to keep track of IRQ7 occurrences to determine default occurrences that may follow.

2.9 PROGRAMMING

The Interrupt Controller is initialized by writing a series of Initialization Command Words to each controller (master and slave) (see Figure 10). Following initialization the controllers are ready to accept interrupt requests. Operation Control Words can then be used to change operating modes and command the controllers for various functions. The master and slave can be programmed to work in different modes.

Table 3 indicates each read/write function and its corresponding address for interrupt controller #1 (master) and interrupt controller #2 (slave).

2.9.1 Initialization Command Word 1 (ICW1)

The initialization sequence is started by writing ICW1 to address 020H or 0A0H. ICW1 has a fixed format as shown in Figure 11. Initialization accomplishes the following:

1. The Interrupt Mask Register is cleared.
2. Fixed Priority Mode is selected.
3. The Slave Mode address is set to 7.
4. Special Mask Mode is cleared.
5. IRR is set for Status Read.

The next three commands to address 021H or 0A1H loads ICW2 through ICW4.

2.9.2 Initialization Command Word 2 (ICW2)

Bits 3–7 are the five most significant bits of the interrupt vector (T3–T7); they are programmable by the CPU. Bits 0–2 are generated by the Priority Resolver during the INTA cycle according to the interrupt level (see Table 2). Figure 12 shows the format for ICW2.

INTERRUPT CONTROLLER	ADDRESS	FUNCTION	READ/WRITE
1	020	ICW1	Write
1	021	ICW2	Write
1	021	ICW3	Write
1	021	ICW4	Write
1	021	OCW1	Write
1	020	OCW2	Write
1	020	OCW3	Write
1	020	IRR	Read
1	020	ISR	Read
1	021	IMR	Read
2	0A0	ICW1	Write
2	0A1	ICW2	Write
2	0A1	ICW3	Write
2	0A1	ICW4	Write
2	0A1	OCW1	Write
2	0A0	OCW2	Write
2	0A0	OCW3	Write
2	0A0	IRR	Read
2	0A0	ISR	Read
2	0A1	IMR	Read

Table 3. Interrupt Controller Function Map

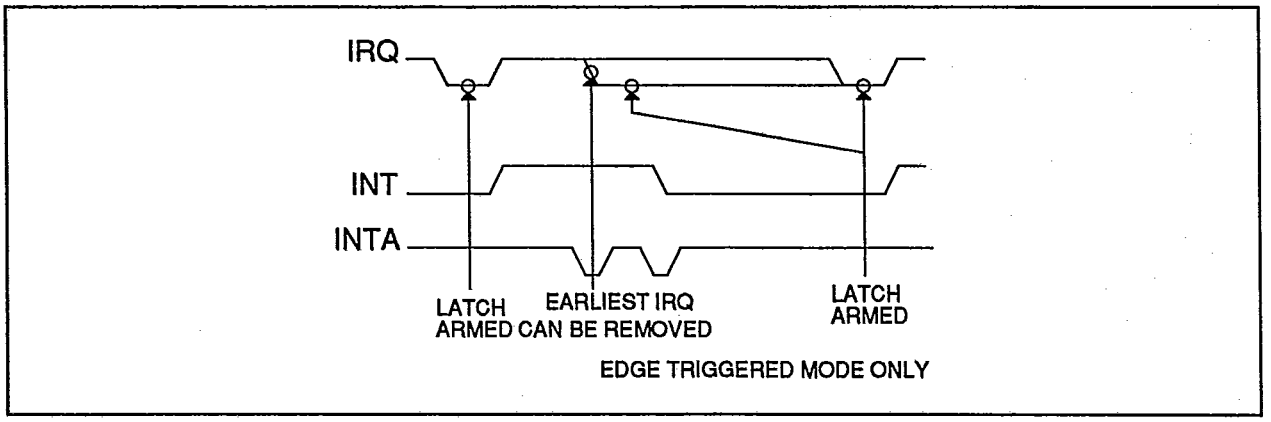


Figure 9. IRQ Triggering Timing Requirements (Note: I/O Address 20/21H applies to Master, A0/A1H applies to Slave.)

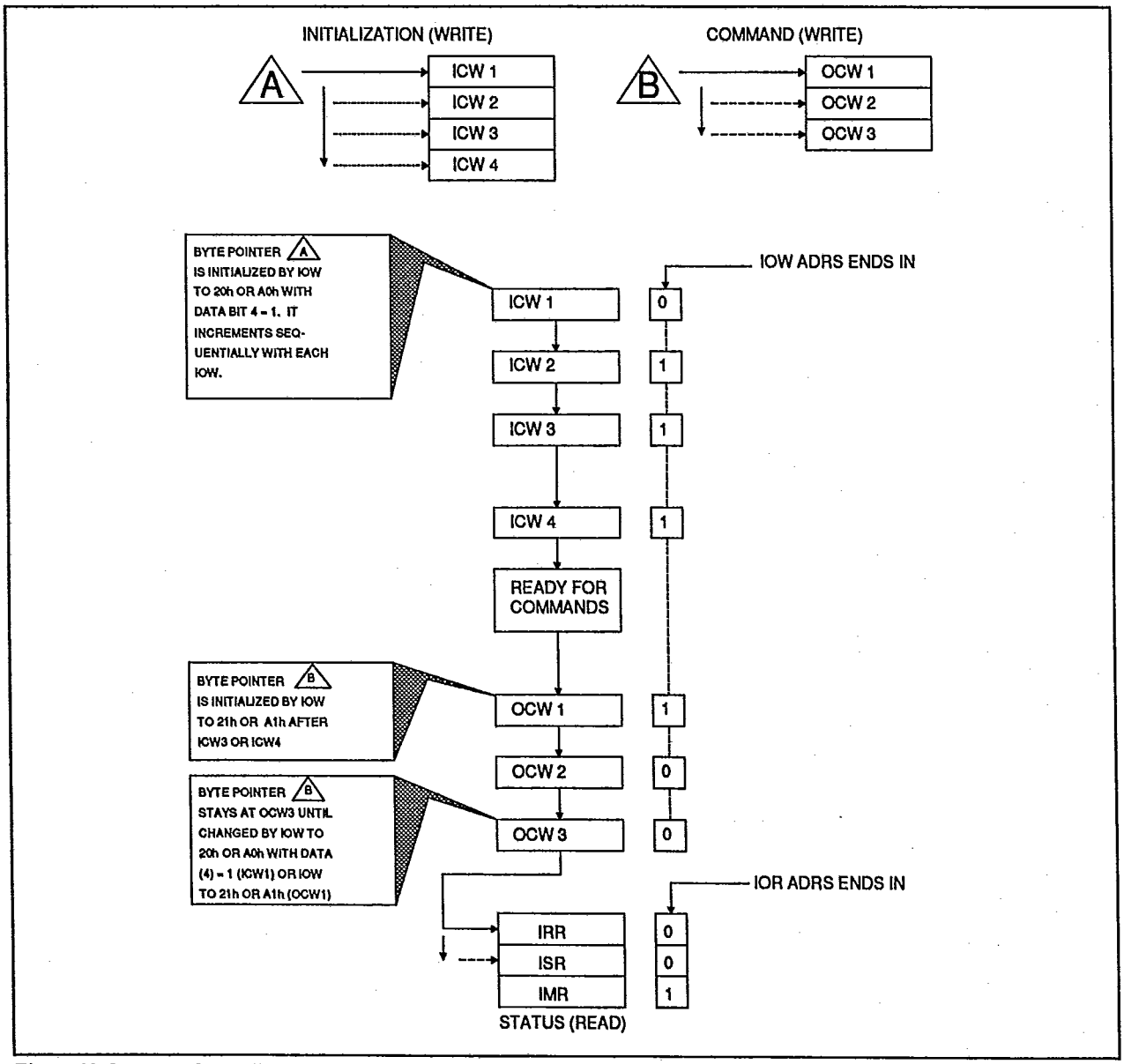


Figure 10. Interrupt Controller Programming Model (Note: I/O Address 20/21H applies to Master, A0/A1H applies to Slave.)

2.9.3 Initialization Command Word 3 (ICW3)

ICW3 initializes the master and slave. For the master, ICW3 sets a 1 for each IRQ input used to cascade a slave. For the slave, bits 0–2 of ICW3 provides the Slave Mode address. Figure 13 shows the format for ICW3 for master and slave. The formats are fixed and must be written as shown in order to function.

2.9.4 Initialization Command Word 4 (ICW4)

ICW4 is used to program Special Fully Nested Mode (SFNM) and Automatic End Of Interrupt (AEOI) (see Figure 14).

7	6	5	4	3	2	1	0
1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0
—	—	—	—	LEVEL TRIG MODE	—	CASCADE MODE	ICW4 NEEDED
0	0	0	1	1	0	0	1

Figure 11. ICW1

= Nonprogrammable

INTERRUPT VECTOR TABLE START ADDRESS POINTER					—	—	—
T7	T6	T5	T4	T3	D2	D1	D0

D2	D1	D0	LEVEL MASTER	LEVEL SLAVE
0	0	0	0	8
0	0	1	1	9
0	1	0	2	10
0	1	1	3	11
1	0	0	4	12
1	0	1	5	13
1	1	0	6	14
1	1	1	7	15

Figure 12. ICW2

INTERRUPT LEVEL HAS SLAVE															
YES	NO	YES	NO	YES	NO	YES	NO	YES	NO	YES	NO	YES	NO	YES	NO
0		0		0		0		0		1		0		0	

(Master Device)

—	—	—	—	—	SLAVE ID		
0	0	0	0	0	0	1	0

(Slave Device)

D2	D1	D0	SLAVE ID = 2
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Figure 13. ICW3 Formats

= Nonprogrammable

2.9.5 Operation Control Word 1 (OCW1)

OCW1 sets and clears the mask bits in the IMR (see Figure 15). M0–M7 represent the eight mask bits, where M0 controls IRQ0, etc. Programming a 1 indicates the interrupt is masked.

2.9.6 Operation Control Word 2 (OCW2)

Bits 5–7 (EOI, SL and R) of OCW2 control the EOI and Rotate modes and combinations of the two (see Figure 16). Bit 0–2 (L0–L2) of OCW2 determines which interrupt is affected when bit 6 is active.

2.9.7 Operation Control Word 3 (OCW3)

Bit 5 and 6 program Special Mask Mode (SMM). Set bit 5 (SMM) and 6 (ESMM) to 1 to program SMM (see Figure 17); SMM = 0 resets the controller to normal mask mode. Polled Mode is enabled when bit 2 is set to 1. Set bit 1 (RR) and bit 0 (RIS) to 0 to read the status of the ISR on SD0–SD7 at address 020H or 0A0H. Set bit 1 to 1 and bit 0 to 0 to read the status of the IRR on SD0–SD7 at address 020H or 0A0H.

3.0 TIMERS AND CLOCK GENERATION

FE5000 contains four counter/timers designated Timer 0–3 (see Figure 18). Timer 1 generates Refresh requests and is not programmable. The time generated is based on the 1.19 MHz clock and is divided by 18.

Timer 1 also generates the clocks to the 80287 and 8742 devices. If a MHZ30 clock input is connected to a 30.0 MHz clock, the output clock is 10 MHz, otherwise, this pin may be connected to the MHZ28 pin and the output will be 9.54 MHz. In either case, the clock output is a 33% duty cycle clock to meet the specifications of the 80287.

The MHZ30 clock input is optional to allow for lower cost implementations. If it is not used this input should be connected to the MHZ28 input.

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

—		—		—		SPEC FULLY NEST MODE		—		—		AUTO EOI		—	
0		0		0		YES	NO	0		0		AUTO	NORM	1	

Figure 14. ICW4

= Nonprogrammable

M7/S15		M6/S14		M5/S13		M4/S12		M3/S11		M2/S10		M1/S9		M0/S8	
YES	NO	YES	NO	YES	NO	YES	NO	YES	NO	YES	NO	YES	NO	YES	NO

Figure 15. OCW1 (Mask Reg)

Mn = Master Mask Bit
Sn = Slave Mask Bit

R	SL	EOI	—	—	IRQ LEVEL		
—	—	—	0	0	L2	L1	L0

R	SL	EOI	FUNCTION
0	0	1	Non-specific EOI Command
0	1	1	Specific EOI Command
1	0	1	Rotate On Non-specific EOI Command
1	0	0	Rotate In Automatic EOI Mode (set)
0	0	0	Rotate In Automatic EOI Mode (clear)
1	1	1	*Rotate On Specific EOI Command
1	1	0	*Set Priority Command
0	1	0	No Operation

*L0–L2 ARE USED

L2	L1	L0	IRQ LEVEL MASTER	IRQ LEVEL SLAVE
0	0	0	0	8
0	0	1	1	9
0	1	0	2	10
0	1	1	3	11
1	0	0	4	12
1	0	1	5	13
1	1	0	6	14
1	1	1	7	15

Figure 16. OCW2

= Nonprogrammable

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

—	SPECIAL MASK MODE		—	—	POLL CMD		READ REG COMMAND	
0	ESMM	SMM	0	1	YES	NO	RR	RIS

ESMM	SMM	SPECIAL MASK MODE
0	0	No Action
0	1	No Action
1	0	Reset Special Mask
1	1	Set Special Mask

RR	RIS	READ REG COMMAND
0	0	No Action
0	1	No Action
1	0	IR Reg On Next $\overline{Rd}$ Pulse
1	1	IS Reg On Next $\overline{Rd}$ Pulse

Figure 17. OCW3

= Nonprogrammable

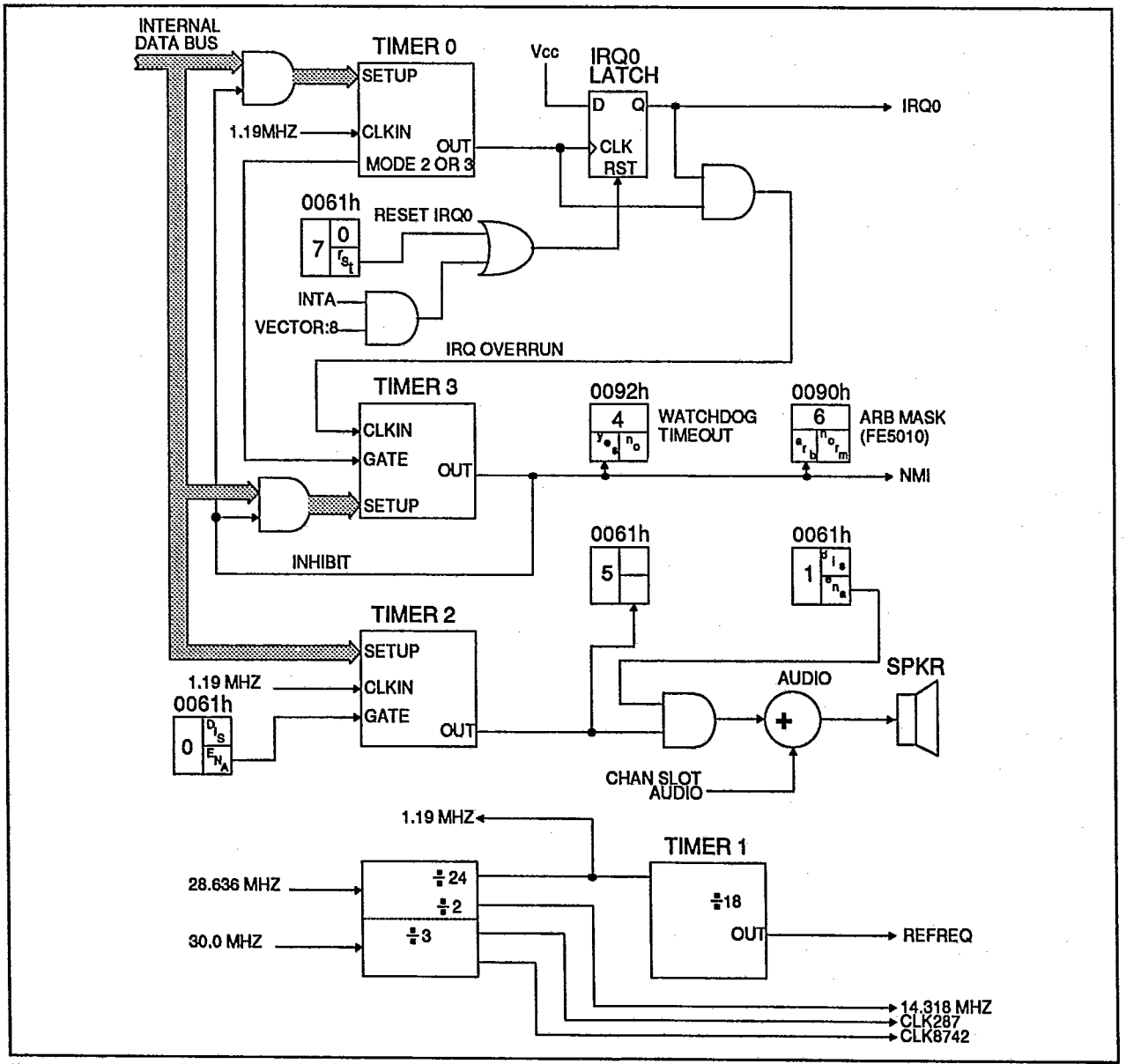


Figure 18. System Timer Functional Block Diagram

3.1 TIMERS 0, 2 AND 3

Timers 0 and 2 are 16 bit programmable binary or BCD down counters. Timer 3 is an 8 bit presettable binary down counter. These counter/timers are fully independent and can be programmed, except as noted, to operate in the modes shown in Table 5. Address 0040H, 0042H, and 0044H are the data ports for Timer 0, 2, and 3 respectively.

MODE	DESCRIPTION
0	Interrupt on Terminal Count
1	Hardware Retriggerable One Shot (Timer 2 only)
2	Rate Generator
3	Square Wave
4	Software Retriggerable Strobe
5	Hardware Retriggerable Strobe (Timer 2 only)

Table 4. Counter Operating Modes

Each counter/timer contains a Control Word Register, a Status Register, a 16-bit Counting Element (CE), a pair of 8-bit input latches called Count Registers (CR_M and CR_L), and a pair of output latches (OL_M and OL_L) (see Figure 19). Each counter also has a clock input (CLK) for loading and decrementing the CE, a GATE input for controlling the counter, and an OUT signal. Only GATE2, OUT2, and OUT3 are externally accessible to the timers.

The contents of the Control Word Register determines how the counter operates. The Control Word Register for Timers 0 and 2 are at address 0043H. The Control Word Register for Timer 3 is at address 0047H. Table 6 summarizes the counter/timer address map. The Status Register, when latched, contains the current contents of the Control Word Register, and status of the counter. The CE is a 16-bit presettable synchronous down counter.

ADDRESS	FUNCTION
040H	Timer 0 Read/Write
042H	Timer 2 Read/Write
044H	Timer 3 Read/Write
043H	Control Word Reg. (Timer 0 & 2) Write Only
047H	Control Word Reg. (Timer 3) Write Only

Table 5. Counter/Timer Address Map

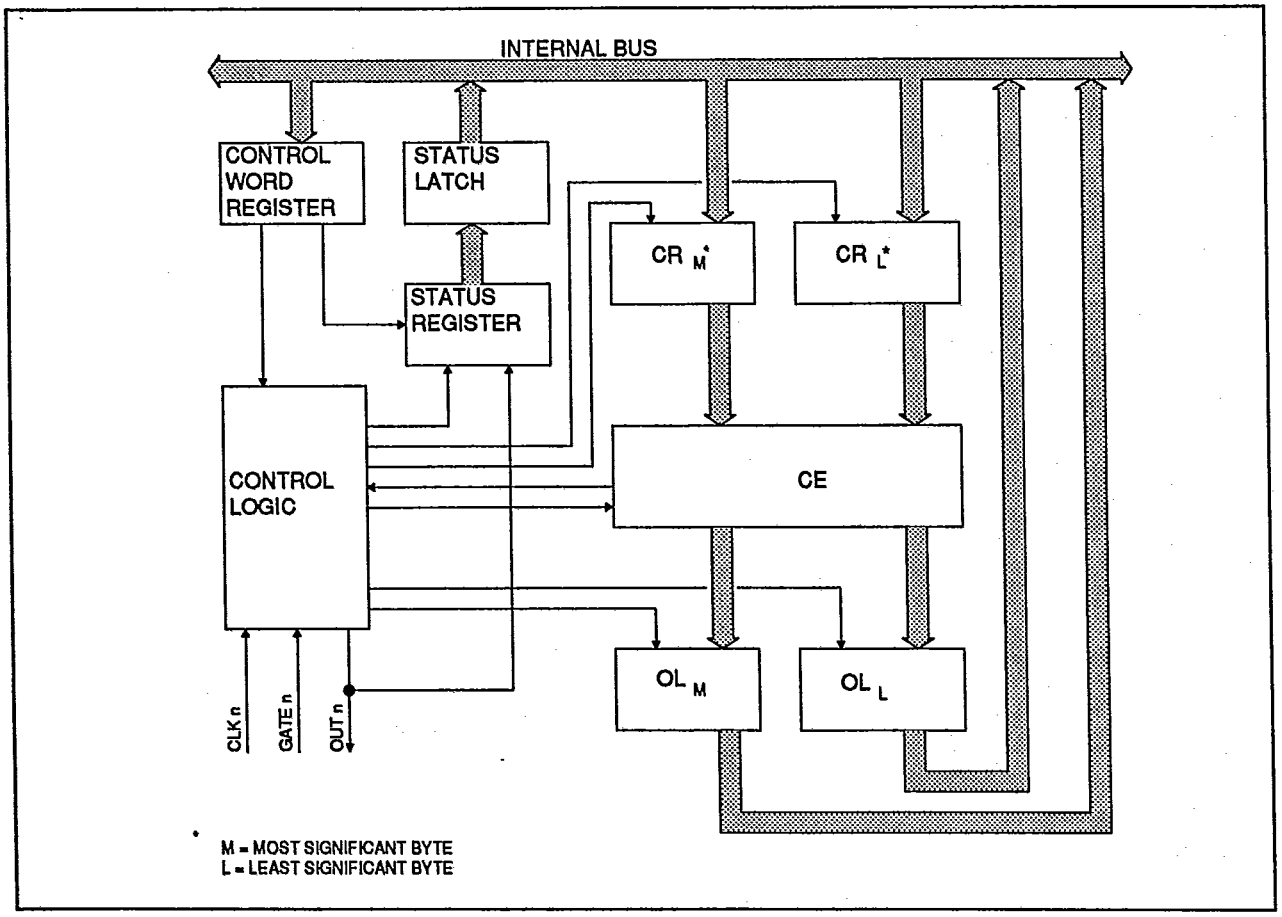


Figure 19. Internal Block Diagram of a Counter

When a new count is written to the counter, the count is stored in the CRs and later transferred to the CE. The CRs are loaded from the internal bus one at a time by the Control Logic. Both bytes are transferred to the CE simultaneously. The CE is loaded or decremented on the falling edge of the timer clock (CLK). The OLs are enabled one at a time by the Control Logic to drive the internal bus.

3.2 PROGRAMMING

At power-up the counter mode, count value, and output of all counters and registers is undefined. Each counter must be programmed before it can be used.

Counters are programmed by writing a Control Word to the Control Word Register followed by an initial count. The Control Word indicates the counter being programmed and the format of the initial count (e.g., most significant only). Figure 20 shows the format for the Control Word for Timers 0 and 2 at address 0043H, and Timer 3 at address 0047H.

3.2.1 Write Operations

When writing to each counter, the Control Word must be written before the initial count is written and the initial count must follow the format specified in the Control Word. As long as the conventions in the Control Word formats are followed, no particular programming sequence is required.

A new initial count may be written to a counter at any time without affecting the programmed Mode of the counter provided the programmed format is followed. Counting is affected as described in the Mode definitions.

Caution

When programmed to write two-byte counts, do not transfer control to another routine that writes into the same counter between writing the first and second byte. Otherwise the counter is loaded with an incorrect count.

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

SELECT COUNTER		READ/WRITE MODE		PROGRAM MODE			COUNT MODE	
SC1	SC0	RW1	RW0	M2	M1	M0	BCD	BNRY

SC1	SC0	SELECT COUNTER	RW1	RW0	READ/WRITE MODE	M2	M1	M0	PROGRAM MODE
0	0	Select Counter 0	0	0	Counter Latch Command	0	0	0	0
0	1	Reserved			(see Read Operations)	0	0	1	1
1	0	Select Counter 2	0	1	Read/Write	X	1	0	2
1	1	Read-back Command			least significant byte only	X	1	1	3
		(see Read Operations)	1	0	Read/Write	1	0	0	4
					most significant byte only	1	0	1	5
			1	1	Read/Write least significant byte first, then most significant byte				

(Register 0043H W/O)

SELECT COUNTER		SETUP MODE		RESERVED
SC1	SC0	RW1	RW0	0

SC1	SC0	SELECT COUNTER
0	0	Select Counter 3
0	1	Reserved
1	0	Reserved
1	1	Reserved

RW1	RW0	SETUP MODE
0	0	Counter 0 Latch Command
0	1	Read/Write least significant byte only
1	0	Reserved
1	1	Reserved

(Register 0047H W/O)

Figure 20. Control Word Formats

▒ = Nonprogrammable

3.2.2 Read Operations

The counters can be read in three ways: a read operation, the Counter Latch Command, and the Read-Back Command. A simple read operation to a counter requires that the CLK input of the selected counter be inhibited by using the GATE input. Otherwise a false reading can result since the counter may be changing during the read.

Caution

When programmed to read two-byte counts, do not transfer control to another routine that reads from the same counter between reading the first and second byte. Otherwise an incorrect count is read.

Counter Latch Command—When a Counter Latch Command is issued in a Control Word (see Figure 20), the output latches (OLs) of the selected counter latch the current count of the CE. The count remains latched until read by the CPU (or until the counter is reprogrammed). A subsequent Counter Latch Command for the same counter is ignored if issued before the latches are read. A Counter Latch Command may be issued to more than one counter and they do not affect the programmed Mode of the counter.

Read-Back Command—When a Read-Back Command is issued in a Control Word (see Figure 21), the count, programmed Mode, and current states of the OUT pin and Null Count flag of the selected counter(s) can be checked. The Read-Back Command can be used to latch multiple counter output latches (OLs) by setting D5 = 0 and selecting the desired counter(s). This command is equivalent to several Counter Latch Commands; one for each counter latched. Similar to the Counter Latch Command, counts are held until read by the CPU or the counter is reprogrammed.

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

—	—	STATUS/COUNTER SELECT				COUNTER SELECTED			—
1	1	—	CNT	—	STS	COUNTER 2	COUNTER 1	COUNTER 0	0

Figure 21. Read-Back Command

OUTPUT	COUNT		READ/WRITE MODE		PROGRAM MODE			COUNT MODE	
STATE	NULL	AVAIL	RW1	RW0	M2	M1	M0	BCD	BNRY

Counter 0, 2 Status Byte

RW1	RW0	READ/WRITE MODE	M2	M1	M0	PROGRAM MODE
0	0	Counter Latch Command	0	0	0	0
		(see Read Operations)	0	0	1	1
0	1	Read/Write least significant byte only	X	1	0	2
1	0	Read/Write most significant byte only	X	1	1	3
1	1	Read/Write least significant byte first, then most significant byte	1	0	0	4
			1	0	1	5

OUTPUT	COUNT		READ/WRITE MODE		RESERVED
STATE	NULL	AVAIL	RW1	RW0	0

Counter 3 Status Byte

RW1	RW0	READ/WRITE MODE
0	0	Counter 0 Latch Command
0	1	Read/Write least significant byte only
1	0	Reserved
1	1	Reserved

Figure 22. Counter Status Bytes

= Nonprogrammable

COMMAND D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION	RESULT
1	1	0	0	0	0	1	0	Read back count and status of Counter 0	Count and status latched for Counter 0
1	1	1	0	0	1	0	0	Read back status—Counter 1	Status latched for Counter 1
1	1	1	0	1	1	0	0	Read back status of Counters 2, 1	Status latched for Counter 2, but not Counter 1
1	1	0	1	1	0	0	0	Read back count—Counter 2	Count latched for Counter 2
1	1	0	0	0	1	0	0	Read back count and status of Counter 1	Count latched for Counter 1, but not status
1	1	1	0	0	0	1	0	Read back status of Counter 1	Command ignored, status already latched for Counter 1

Figure 23. Read-Back Command Examples

Status information of the selected counter(s) can be latched by the Read-Back Command by setting status bit D4 = 0. The status is latched until read by the CPU with a read operation to the counter (or the counter is reprogrammed). Figure 22 shows the format for the counter status. Bits 0–5 indicate the programmed status of the counter as written into the Control Word Register.

D7 (Figure 22) allows monitoring of the counter output. The Null Count (NC) flag indicates the condition of the CE. NC = 1 during a write operation to the Control Word Register or the counter. NC = 0 when a new count is loaded from the CRs to the CE. If the counter is programmed for two-byte counts, NC = 1 when the second byte is written.

Both count and status of the selected counter(s) may be latched simultaneously by setting D4 and D5 = 0. This command equivalent to two Read-Back Commands. If both count and status are latched with a Read-Back Command, the first read operation to the selected counter(s) returns the status. The next read (or two reads if the counter is programmed for two-byte counts) returns the latched count. Subsequent reads return unlatched counts.

3.3 COUNTER OPERATION

Each counter may be set in one of 5 modes by writing a Control Word. When a Control Word is written to a counter, all Control Logic is immediately reset and OUT goes to a known initial state; no CLK pulse is required.

New counts are loaded and counters are decremented on the falling edge of CLK. The maximum possible initial count is 0-equivalent to 65536 in binary operation or 10000 in BCD. The counter does not stop when it reaches 0. In Modes 0, 1, 4, and 5 it wraps around to the highest count (FFFF in binary operation or 9999 in BCD). In Modes 2 and 3, the counter is reloaded with the initial count and continues counting. Figure 24 shows minimum and Maximum initial counts for each mode.

The GATE input is level sensitive in Modes 0, 2, 3, and 4 and is sampled on the rising edge of CLK. In Modes 1, 2, 3, and 5 the GATE input is rising-edge sensitive-arising edge (trigger) sets an internal flip-flop whose output is sampled on the next rising edge of CLK. The flip-flop resets immediately after it is sampled. Note that in Modes 2 and 3, the GATE input is both edge and level-sensitive.

MODE	MIN COUNT	MAX COUNT
0	1	0
1	1	0
2	2	0
3	2	0
4	1	0
5	1	0
Note: 0 is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.		

Figure 24. Minimum and Maximum Initial Counts

3.3.1 Mode 0—Interrupt on Terminal Count

Mode 0 is typically used for event counting. Writing the Control Word causes OUT to go low and remain low until the counter reaches 0. At this time OUT goes high and remains high. The counter continues to run until a new count or Control Word is written. Counting is enabled when GATE = 1. Disabling the count (GATE = 0) has no effect on OUT.

The initial count is loaded into the CE on the next CLK pulse after the Control Word and initial count are written. For an initial count of N, OUT goes high N+1 CLK pulses later. Writing a new count reloads the counter (CE) on the next CLK pulse and counting continues from the new count.

When writing a two-byte count, the first byte disables counting and OUT is set low. After writing the second byte, the new count is loaded on the next CLK pulse. This allows the counting sequence to be synchronized by software.

If an initial count is written when GATE = 0, it is still loaded on the next CLK pulse. When GATE = 1, counting begins and OUT goes high N CLK pulses later. Figure 25 shows examples of Mode 0 operation.

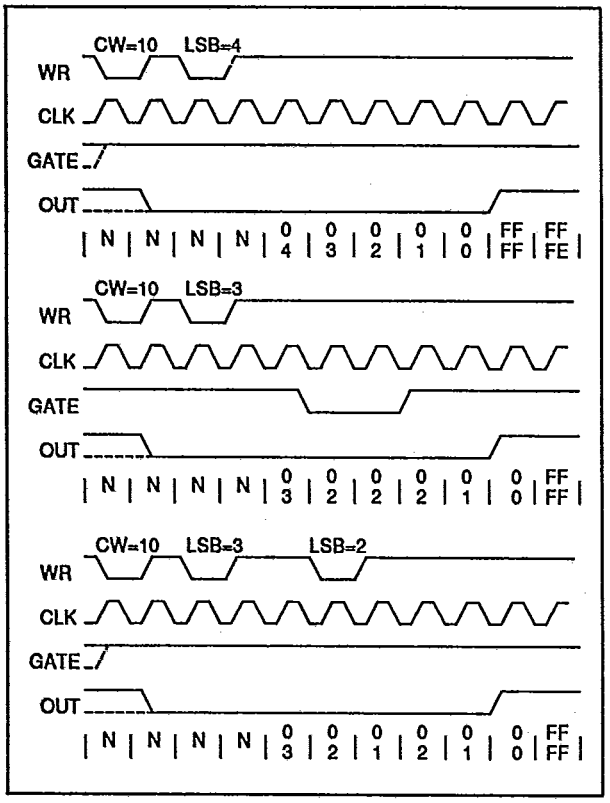


Figure 25. Mode 0 Examples

3.3.2 Mode 1—Hardware Retriggerable One-Shot

Writing the Control Word causes OUT to go high. A trigger (i.e., GATE = 1) causes OUT to go low on the next CLK pulse and remain low until the counter reaches 0; this creates the one-shot pulse. At this time OUT goes high and remains high until the next trigger. An initial count of N results in a one-shot pulse N CLK cycles long.

Since the one-shot is retriggerable, if another trigger occurs during a one-shot pulse, OUT remains low to extend the pulse for N CLK cycles. Writing a new count during a one-shot pulse has no effect unless the counter is retriggered in which case the pulse extends from the new count. GATE has no effect on OUT. Figure 26 shows examples of Mode 1 operation. Mode 1 is valid for counter 2 only.

3.3.3 Mode 2—Rate Generator

Mode 2 functions as a divide-by-N counter. It is typically used to generate a real-time clock interrupt. Writing the Control Word causes OUT to go high. When the initial count reaches 1, OUT goes low for one CLK

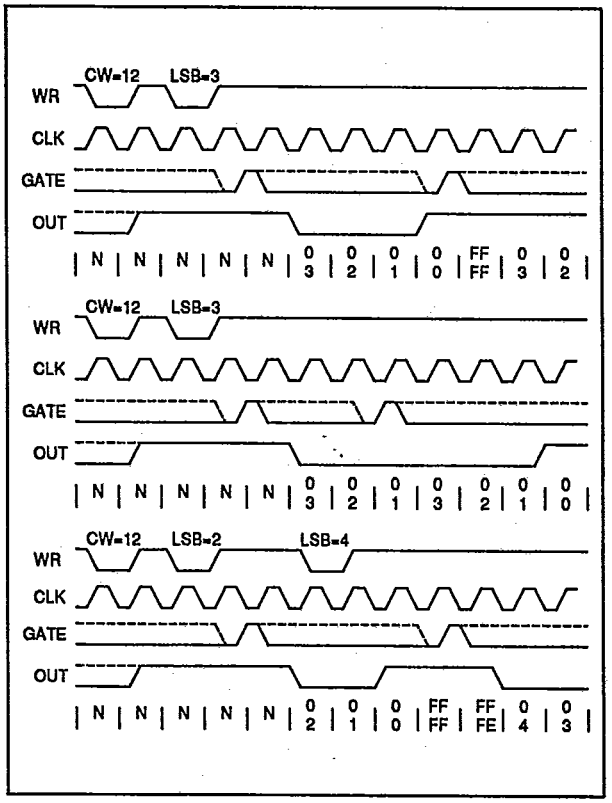


Figure 26. Mode 1 Examples

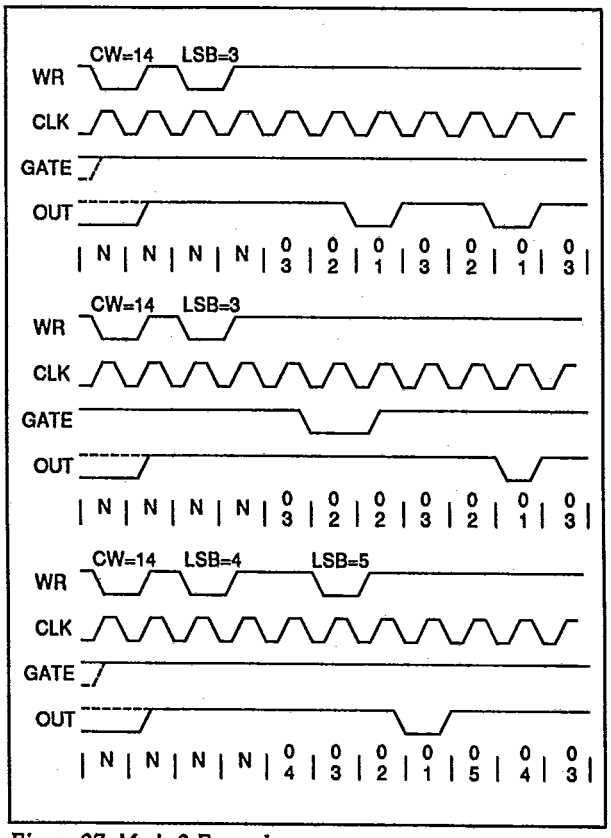


Figure 27. Mode 2 Examples

pulse. When OUT goes high, the counter reloads the initial count and the process is repeated. For an initial count of N, the sequence repeats every N CLK cycles. Note that a count of 1 is illegal in Mode 2.

Counting is enabled when GATE = 1. GATE = 0 disables counting and forces OUT high. A trigger reloads the counter with the initial count on the next CLK pulse. Using the GATE input allows synchronization with external events.

Writing a new count during a counting sequence has no effect unless the counter is triggered. If triggered, the count is extended by the new count on the next CLK pulse. Otherwise, the new count is loaded at the end of the current counting cycle. Figure 27 shows examples of Mode 2 operation.

3.3.4 Mode 3—Square Wave Generator

Mode 3 is typically used for Baud rate generation. This mode is identical to Mode 2 except for the duty cycle of OUT. Writing the Control Word causes OUT to go high and remain high for the first half of the count. Then OUT goes low and remains low for the remainder of the count. The cycle is repeated thus creating a square wave with a period of N CLK cycles when the initial count is N.

If the counter is loaded with an even count, the duty cycle of OUT is 50% (i.e., high = low = N/2). For odd count values, OUT is high for one CLK cycle longer than it is low (i.e., high = (N+1)/2 and low = (N-1)/2). Figure 28 shows examples of Mode 3 operation.

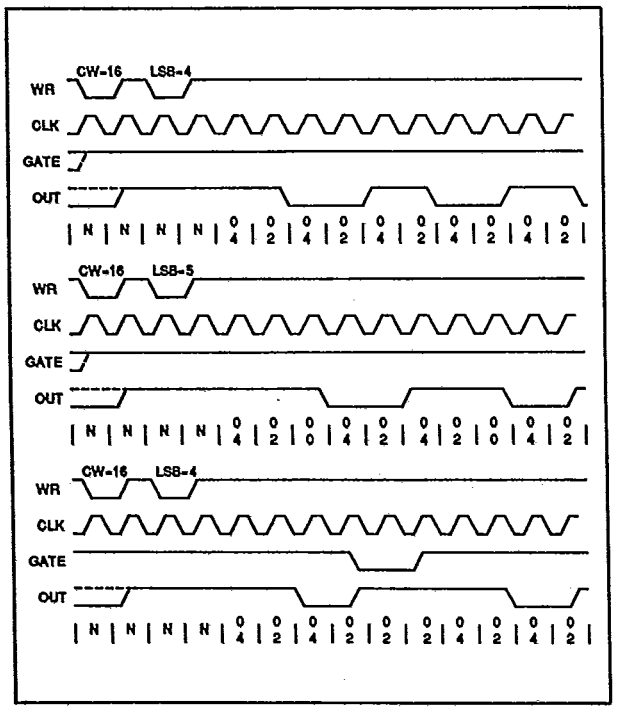


Figure 28. Mode 3 Examples

3.3.5 Mode 4—Software Triggered Strobe

Writing the Control Word causes OUT to go high. When the initial count expires, OUT goes low for one CLK cycle. The sequence is started by writing the initial count. Counting is enabled when GATE = 1. Disabling the count (GATE = 0) has no effect on OUT.

The initial count is loaded on the next CLK pulse after the Control Word and initial count are written. For an initial count of N, OUT goes low for one CLK cycle N+1 CLK cycles later.

If a new count is written during a counting sequence, it is loaded into the CE on the next CLK pulse and counting continues from the new count. When writing a two-byte count, the first byte has no effect on counting. After writing the second byte, the new count is loaded on the next CLK pulse. This allows the counting sequence to be retriggered by software. Figure 29 shows examples of Mode 4 operation.

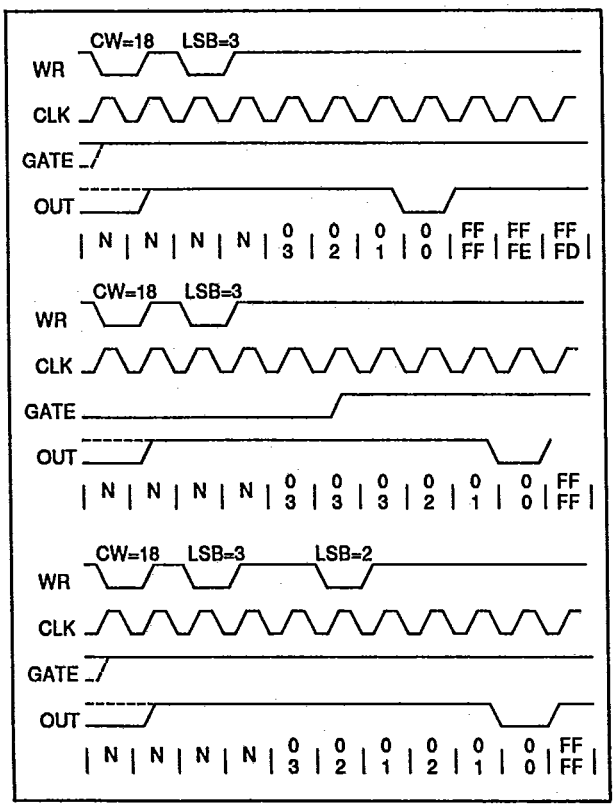


Figure 29. Mode 4 Examples

3.3.6 Mode 5—Hardware Triggered Strobe

Writing the Control Word causes OUT to go high. Counting is started by a trigger (i.e., rising edge of GATE) which loads the CE on the next CLK pulse. When the initial count N expires, N CLK cycles later, OUT goes low for one CLK cycle. GATE = 0 disables the counting.

Writing a new count during a counting sequence has no effect unless the counter is triggered. If triggered, the count is extended by the new count on the next CLK pulse. Otherwise, the new count is loaded at the end of the current counting cycle. Figure 30 shows examples of Mode 5 operation. Mode 5 is valid only for counter 2.

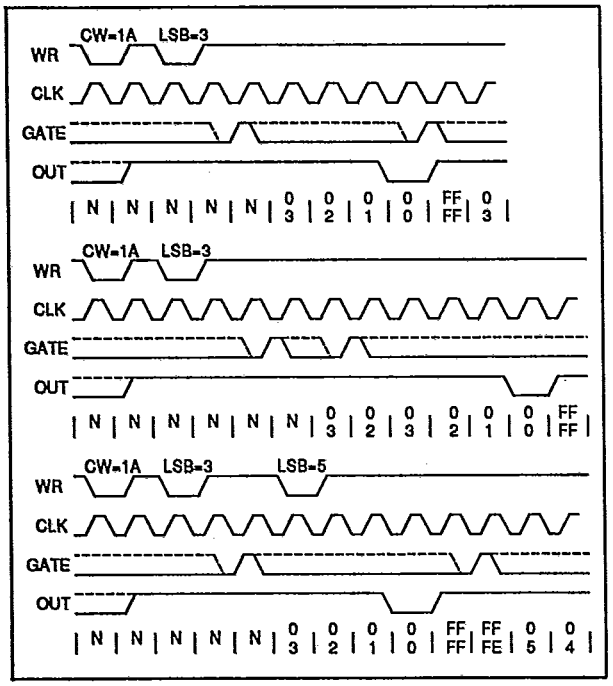


Figure 30. Mode 5 Examples

3.4 WATCHDOG TIMER OPERATION

The watchdog timer is setup by writing the Control Word for Timer 3 to location 0047H and the count value to location 0044H. Timer 3 is enabled to count on the first CLK pulse after the count is loaded to the CE. The CLK pulse for the watchdog timer is the output of Timer 0 which occurs every 55.05 ms.

The watchdog timer (Timer 3) can be enabled to monitor the IRQ0 service routine. When Timer 3 is loaded with a count of 1 and IRQ0 (latched) is pending for more than one CLK cycle, Timer 3 decrements to 0 generating a watchdog timeout and NMI. Write access to Timer 0 and 3 is disallowed when a watchdog timeout occurs. The watchdog timer implementation assumes that the NMI vector in low memory has not been corrupted. System recovery may be invoked by the NMI service routine.

The IRQ0 Latch is reset by:

1. System Reset or

2. IOW to 0061H D7 = 1 or

3. INTA (Interrupt Ack) with vector (D7:0) = 8

Timer 3 is disabled by resetting the IRQ0 Latch and then performing the steps described for watchdog setup above.

4.0 SYSTEM BOARD SETUP

The Programmable Option Select (POS) is implemented by IO registers 0091H, 0094H, 0096H, 0100H, 0101H, 0102H, and 0103H (see Figure 31). POS eliminates switches from the system board and Channel adapters by incorporating programmable registers. The programmed configuration data and adapter ID numbers are then stored in battery-backed CMOS RAM. This permits the Power-On Self-Test (POST) to automatically reconfigure the system whenever the system is powered on. POS registers 0100H and 0101H contain the system ID code. These registers are read-only but can be written one time to store the appropriate ID. The ID codes for the the model 50 and 60 are shown in Table 6.

MODEL	0101H	0100H
50	FB	FF
60	F7	FF

Table 6. System ID Codes

Figure 32 indicates the bit definitions for POS registers 0102H and 0103H. Bit 0 of register 0102H allows bits 1, 2, and 4 to enable and disable their respective devices. In Compatible Mode (bit 7 = 1), the parallel port is compatible with the PC/AT* printer port. In Extended Mode, it operates in bidirectional mode compatible with the Models 50 and 60. This port is configured by POS register 0102H, bits 4–7.

The configuration of on-board serial ports is controlled by either the POS register 0102H or the Peripheral Control Register (PCR). The PCR is part of the Extended Setup Facility (ESF). The physical ports are identified as SP1 and SP2. There are two logical ports identified as the primary serial port at locations 03F8–03FFH (IRQ4) and the alternate serial port at locations 02F8–02FFH (IRQ3). SP1 is configured by POS register 0102H, bits 2 and 3. Note that bits 2 and 3 are overridden in Extended Mode (see EXTENDED SETUP FACILITY, Section 9.0).

Figure 33 indicates the bit definitions for POS registers 0091H, 0094H, and 0096H. POS register 0091H (read only) is used to determine if the PVGA, the system board, or a Channel adapter is present in the systems board peripherals. The Card Selected Feedback ($\overline{\text{CDSFDBK}}$) signal is set to 0 when the address space of the adapter is accessed. Bit 0 of 0091H is set to 1 whenever $\overline{\text{CDSFDBK}}$ is asserted or when the system board IO functions are accessed by an IO cycle.

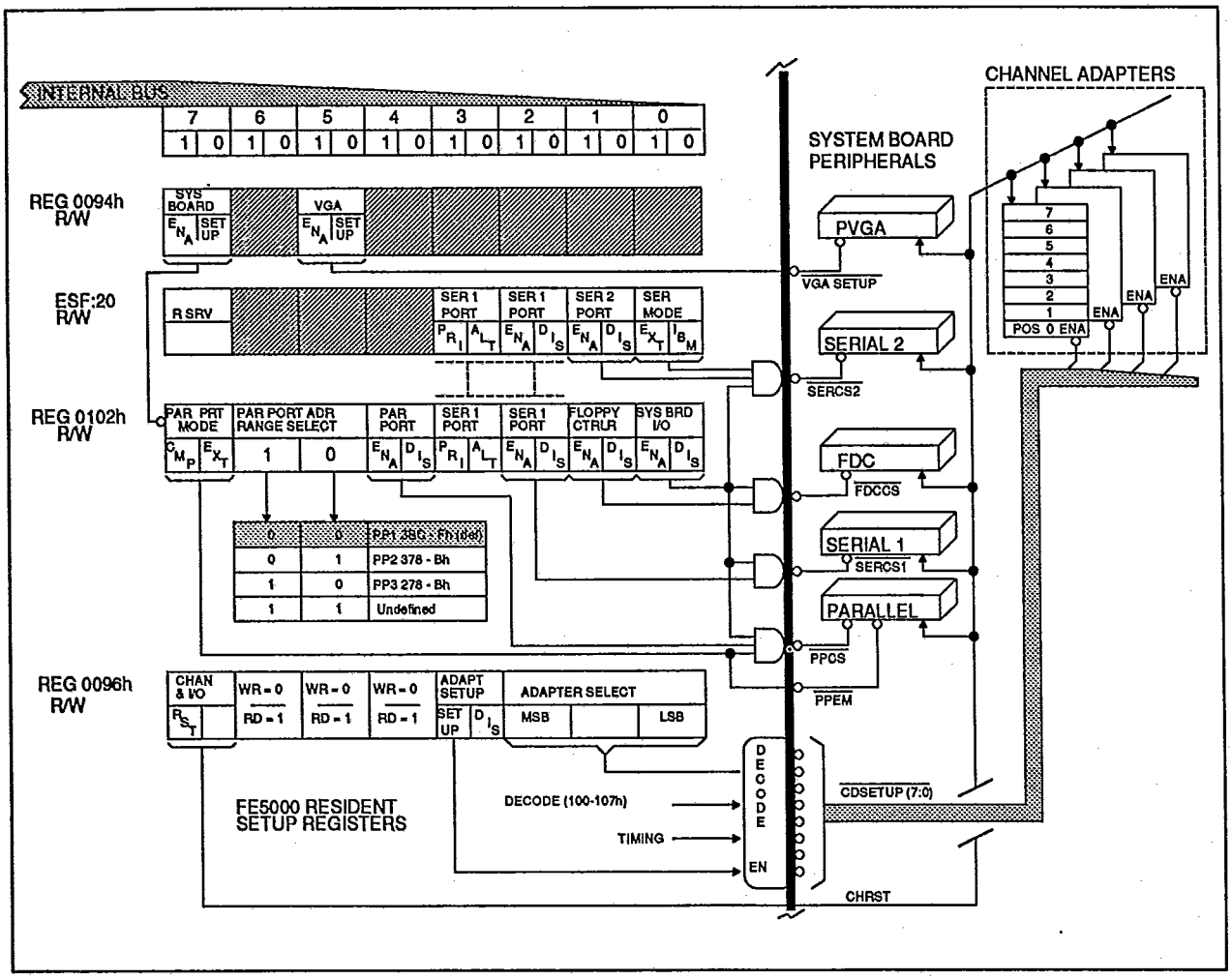


Figure 31. System Board Setup Functional Block Diagram

7	6	5	4	3	2	1	0
1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0

0102H

PARALLEL PORT MODE		PARALLEL PORT SETUP		PARALLEL PORT		SERIAL PORT SEL		SERIAL PORT (SP1)		FLOPPY CONTROL		SYSTEM BOARD IO	
PC/AT COMP	EXT	—	—	ENA	DIS	SP1 = PRIM	SP1 = ALT	ENA	DIS	ENA	DIS	ENA	DIS

6	5	Parallel Port Setup
0	0	PP1 3BC–Fh
0	1	PP2 378–Bh
1	0	PP3 278–Bh
1	1	undefined

0103H

RESERVED	DET 2	DET 1	RESERVED	SYS BD MEM	
1	0	1	1	ENA	DIS

Figure 32. POS Register Formats (0102H and 0103H)

= Nonprogrammable or Default

The Paradise® Video Graphics Array (PVGA1), system board peripherals and Channel adapters are configured or enabled by specific bit settings in registers 0094H and 0096H. Bits 5 and 7 of register 0094H configures PVGA Setup Mode and System Board Setup Mode, respectively. Bit 3 of register 0096H enables Adapter Setup Mode.

Caution

Only one category of device can be in Setup Mode at a time. If more than one is in Setup Mode, bus conflicts occur.

5.0 SYSTEM CONTROL REGISTERS

The FE5000 has two Model 50/60 compatible System Control Registers at 0061H (Control Port B) and 0092H (Control Port A). These ports are defined in Figures 34 and 35.

See EXTENDED SETUP FACILITY, Section 9.0, for other control registers.

6.0 COPROCESSOR INTERFACE

The Coprocessor support function provides error and control signals between the CPU and coprocessor, if any.

An error signal from the coprocessor (ERROR287) generates an interrupt (IRQ13) in the FE5000 that causes the busy signal to the coprocessor (BUSY286) to be held in the busy state. The interrupt and busy are cleared by writing 00H to the Coprocessor Clear Busy register (00F0H).

A power-on reset, system reset, or an IO write operation to register 00F1H with data = 00H sets the coprocessor in Real-Address Mode. The coprocessor is placed in the Protected Mode by executing the SETPM ESC instruction.

7.0 EXTERNAL DEVICE ENABLE

The FE5000 enables the following external devices:

- Keyboard/Auxiliary Controller (8742)
- Floppy Disk Controller
- Parallel Port
- Serial Ports
- PVGA
- Real Time Clock/CMOS RAM
- Coprocessor
- Port A/B decodes (programmable decodes)

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

RESERVED														CARD SEL FEEDBACK	
—														YES	NO

0091h Read Only

SYS BOARD		RESERVED		VGA ENABLE		RESERVED									
ENA (NML)	SETUP MODE	—	—	ENA (NML)	SETUP MODE	—	—	—	—	—	—	—	—	—	—

0094H Read/Write

RESET CHANNEL		RESERVED						ADAPTER SETUP		CARD SELECT		
RSET	—	READ AS 1	WRITE AS 0	READ AS 1	WRITE AS 0	READ AS 1	WRITE AS 0	ENA	DIS	—	—	—

0096H Read/Write

2	1	0	Card Select Slot
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Figure 33. POS Register Formats (0091H,0094H, and 0096H)

= Default

In general, IOR or IOW to the address ranges shown in the I/O map (see Table 1, System Level IO Map) activates the various chip select lines. The FE5000 control interface is shared by the Channel. The System Board Setup Functional Block Diagram (Figure 31) indicates the selection of the floppy disk controller ($\overline{FDCCS}$), the parallel port controller ($\overline{PPCS}$), and serial ports 1 ($\overline{SERCS1}$) and 2 ($\overline{SERCS2}$) by enabling the appropriate POS registers.

The keyboard/auxiliary controller is selected ($\overline{CS8742}$) when the keyboard data port is accessed at location 0060H, or when a read or write to the keyboard command/status port is executed at location 0064H. The coprocessor is selected ($\overline{NPS1}$) when the coprocessor ports are addressed at locations 00F8–00FFH. $\overline{CSA}$ and $\overline{CSB}$ are configurable select lines controlled by Ports A and B (see EXTENDED SETUP FACILITY, Section 9.0, for a description of other control registers).

8.0 PERIPHERAL BUS CONTROL

The Peripheral Bus Control generates control signals that interface the peripheral devices, that are enabled by the External Device Enable function, to the CPU complex. $\overline{CHS0}$, $\overline{CHS1}$ and M/$\overline{IO}$ encode the Microchannel bus cycle type information as shown in Table 7.

M/$\overline{IO}$	$\overline{S1}$	$\overline{S0}$	BUS CYCLE TYPE
0	0	0	Interrupt Acknowledge
0	0	1	IO Read
0	1	0	IO Write
0	1	1	No Cycle
1	0	0	System CPU Halt or Shutdown
1	0	1	Memory Read
1	1	0	Memory Write
1	1	1	No Cycle

Table 7. Channel Command Encoding

9.0 EXTENDED CMOS RAM INTERFACE AND EXTENDED SETUP FACILITY

Externally available signals related to the Extended CMOS RAM (ECR) and the Extended Setup Facility (ESF) are provided by the FE5000. However, implemen-

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

PARITY CHECK		CHAN CHECK		TIMER 2 STATE	REFRESH TOGGLE	CHAN CHECK		PARITY CHECK		SPKR DATA		TIMER 2 GATE	
ERR	OK	ERR	OK	—	—	DIS	ENA	DIS	ENA	DIS	ENA	DIS	ENA

Read

RESET IRQ 0		RESERVED	CHAN CHECK		PARITY CHECK		SPKR DATA		TIMER 2 GATE	
RSET	ENA	—	DIS	ENA	DIS	ENA	ENA	DIS	ENA	DIS

Write

Figure 34. System Control Register Formats (0061H)

= Default

SYSTEM STATUS ($\overline{SYSSTA}$)	RESERVED	WATCHDOG TIMEOUT		PASSWORD SEC LOCK		RESERVED	ALTERNATE A20		ALTERNATE HOT RST	
—	—	YES	NO	YES	NO	—	YES	NO	RST	NO

7	6	System Status
0	0	Off
0	1	On
1	0	On
1	1	On

GATE A20 / A20 = 0

Note: Read/Write in FE5000. Function implemented in FE5010.

Figure 35. System Control Register Formats (0092H Read/Write)

= Default

tation of the ECR and ESF is shared between the FE5000 and the FE5010. Figure 36 is a block diagram of ECR and ESF indicating how functions are divided between the FE5000 and the FE5010.

9.1 EXTENDED CMOS RAM (ECR) INTERFACE

The ECR supports Real Time Clock (RTC) access, and additional storage for POS and the Extended Setup Facility (ESF) parameters needed for large systems. The RTC function is accessed through IO ports 0070H and 0071H. Port 0070H is used to point to the internal register or RAM location (see Figure 37). Port 0071H is the read/write data port. See the IBM Technical Reference for the CMOS RAM byte definition.

The ECR interface allows an additional 8K bytes for storage of POS and/or additional system parameters. This function is accessed through ports 0074H, 0075H,

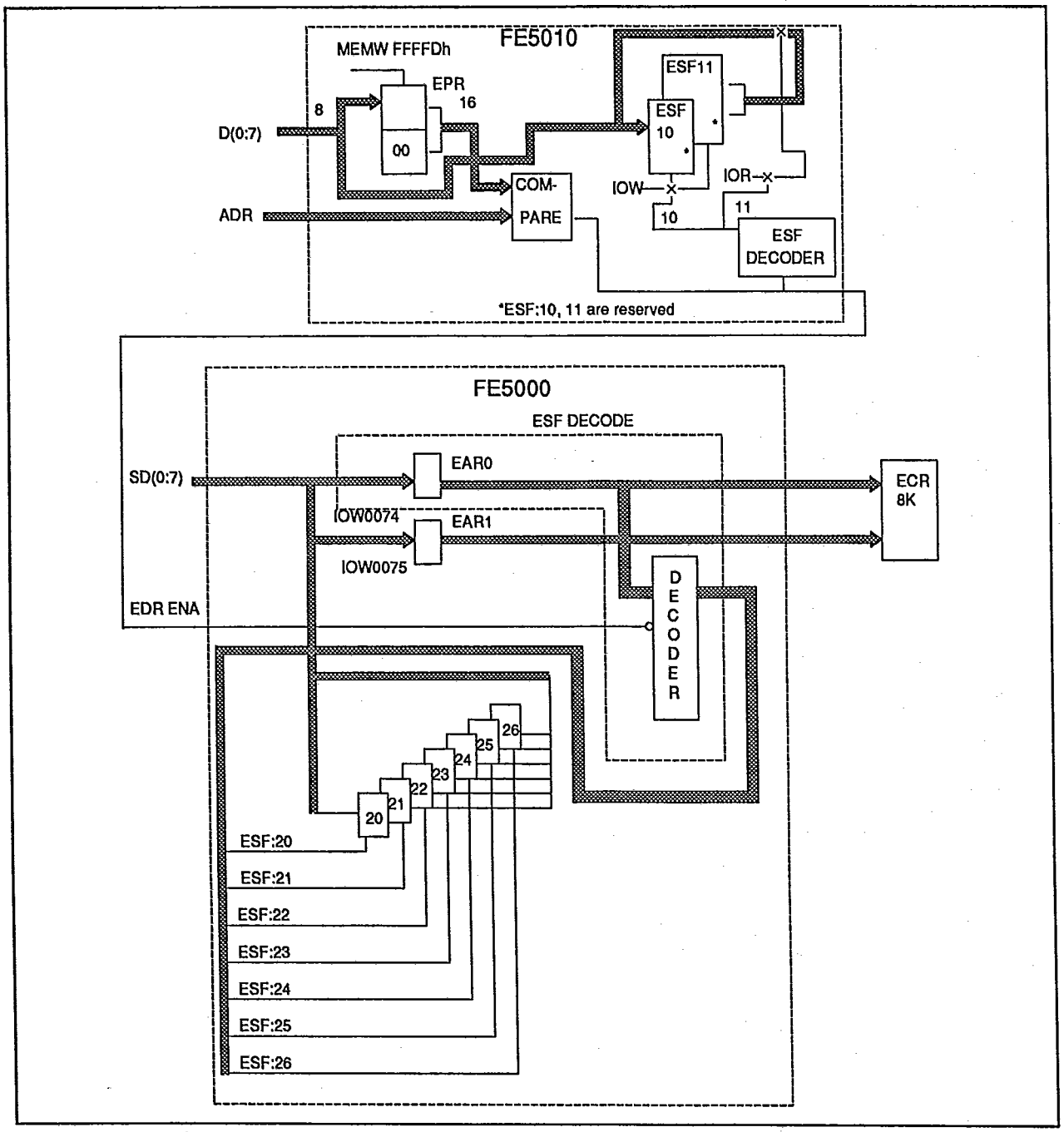


Figure 36. ECR and ESF Block Diagram

and 0076H when the RTC CMOS address port (0070H) is set to 8DH. Ports 0074H (EAR0) and 0075H (EAR1) are used to set the desired RAM address. The ECR address bus, CMOSA(12:0), consists of EAR0, the LSB of the ECR address, and bits 0–4 of EAR1, the MSB of the ECR address. Port 0076H is the data port.

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

NMI		RESERVED	RT/CMOS ADDRESS					
DIS	ENA	—	MSB	—	—	—	—	LSB

Figure 37. RTC/CMOS Address Port Register (0070H)

= Default

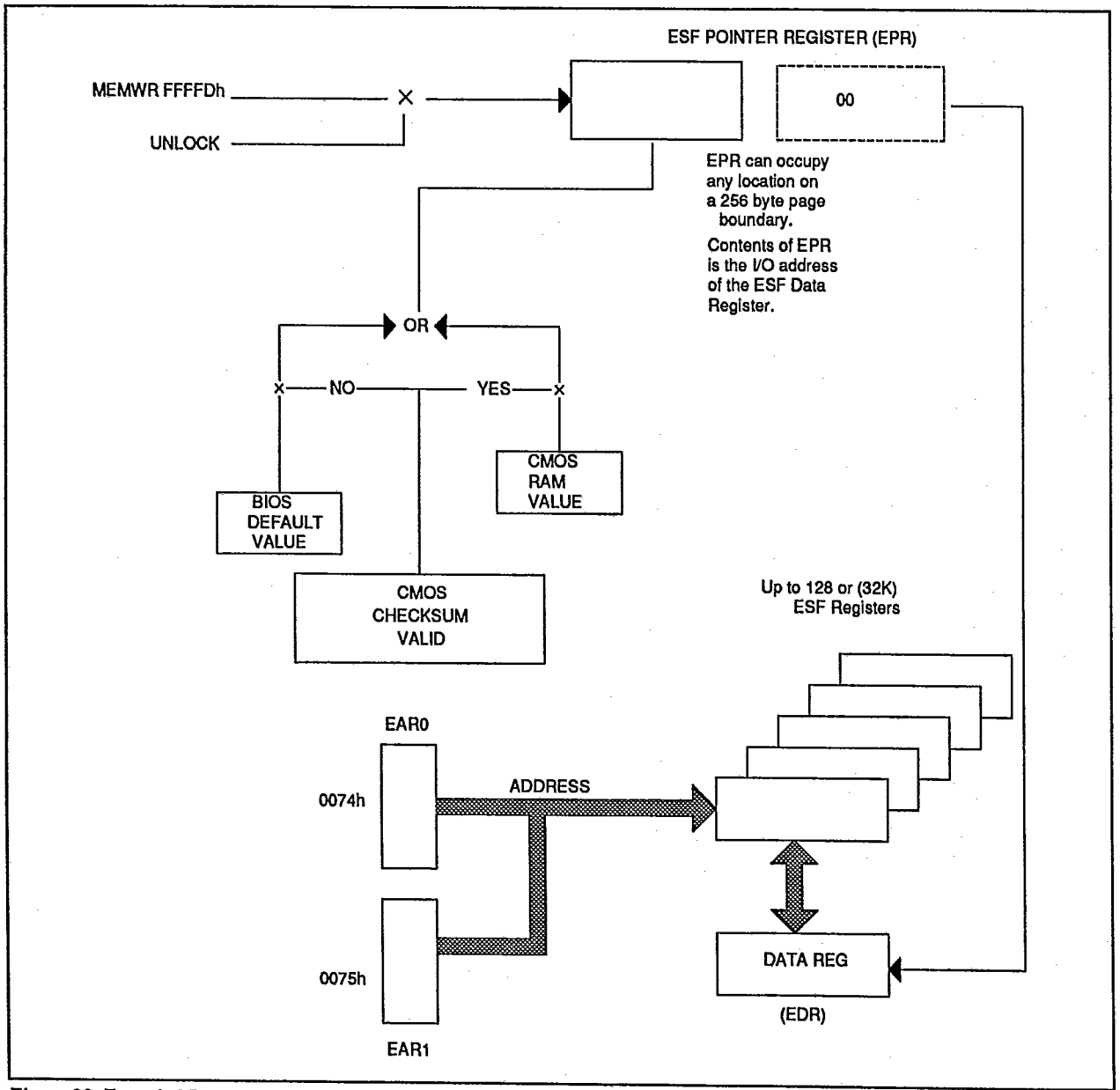


Figure 38. Extended Setup Facility Overview

9.2 EXTENDED SETUP FACILITY (ESF)

The ESF function consists of the ESF Pointer Register (EPR) and associated decode logic that generates the ESF Data Register Enable (EDRENA) output from the FE5010 to the FE5000. ESF is designed to extend the configuration architecture established with the POS features. See Figure 38 for an overview of the ESF function. ESF supports:

- Memory Map Control Registers
- Additional physical serial port (SP2)
- Programmable Port Enables A and B
- EMS control registers
- External DRAM control configuration
- System board LAN configuration
- Customer specified enhancements that could include:
  System Identification
  System Version

9.2.1 ESF Access

ESF is based on an "alternate IO space" concept similar to how IBM has implemented their Extended CMOS RAM feature. ESF space (128 locations expandable to 32K) is accessed through a single "real IO space" window called the ESF Data Register (EDR). ESF space may be implemented as either word or byte-wide at the discretion of the designer.

The EDR is pointed to by the software configurable (write only) ESF Pointer Register (EPR) located in the FE5010. The EPR is loaded by writing to memory location FFFFDH or FFFFFDH (normally a PROM). The power-on default location for the EDR is located at IO address 0700H.

The following procedure is recommended for modifying the EPR:

1. Set the value 8DH in port 0070H to disable NMI.
2. Read the System Control Port B at 0061H and test for a change in the state of bit 4 (Refresh Toggle) to synchronize to the refresh circuitry
3. Read EAR0 at 0074H (normally write only) to unlock the EPR.
4. Write the new value into the EPR (FFFFDH). This locks the EPR again.
5. Enable NMI if required.

Note that the EPR is locked when written or on the next refresh cycle, whichever occurs first.

The value in the EPR becomes the new 8-bit address of the EDR. The EDR can reside at any of 256 locations in the 64K IO space of the CPU from 0400H to FF00H.

To address the ESF IO space:

1. Write the value 8DH to port 0070H to disable NMI.
2. Write the address value to EAR0 at 0074H (and EAR1 if expanded ESF is being used).
3. Issue an IO Read or Write command to EDR Address.

The selected ESF register is determined by decoding the EAR0 (and EAR1) address value.

9.2.2 ESF Address Maps

The lower 64 bytes (EAR0 = 00H–3FH) are reserved for Faraday functions and features. The top 64 bytes (EARO

ESF ADDRESS	DEFINITION
00H–0FH	System Reserved
10H–1FH	System board core functions
20H–3FH	System board peripheral functions
40H–7FH	Customer Specified
0080H–FFFFH	Expansion (EAR0 bit 7 must be 1)

Table 8. ESF General Usage Map

ESF ADDRESS	DEFINITION
ESF:10	Reserved
ESF:11	Reserved
ESF:16	Ram Control (FE5030)
ESF:17	Bank 0 Boundary (FE5030)
ESF:18	Bank 1 Boundary (FE5030)
ESF:19	Bank 2 Boundary (FE5030)
ESF:1A	Bank 3 Boundary (FE5030)
ESF:1B	Split Memory Address (FE5030)
ESF:1C	SRBR (FE5030)
ESF:1D	Timing Control (FE5030)
ESF:1E	EMS Control (FE5030)
ESF:1F	Cache Control (FE5030)
ESF:20	Peripheral Configuration Register (PCR)
ESF:21,24	Port A, B Control Registers
ESF:22,25	Port A, B Address Register (LSB)
ESF:23,26	Port A, B Address Register (MSB)
ESF:80-FF	EMS Page Registers (FE5030)

Table 9. ESF System Address Map

=40H–7FH) are for customer use (see Table 8). All functions using ESF must include bit 7 in the decode. Bit 7 of EAR0 must be 0 when addressing only 128 ESF registers. To expand the ESF to 32,768 locations, set EAR0 bit 7 to 1 and write the second ESF address byte to EAR1.

The ESF address map in a system environment is shown in Table 9. It includes the FE5030 usage. ESF:20–ESF:26 reside in the FE5000; ESF:10 and ESF:11 reside in the FE5010 and are reserved.

9.2.3 Peripheral Configuration Register (PCR)

The PCR is assigned to ESF location 20H. It allows the additional serial port (SP2) to be configured. When PCR bit 0 = 1 (Extended Mode enabled), bits 2 and 3 in the System Board Setup register (0102H) are overridden. Figure 39 shows the PCR format.

9.2.4 Port A/B Decodes

Ports A and B are identical device enable ports configurable by software. The 16-bit starting IO address, port depth (up to 128 bytes), programmable wait state logic, and enable/disable control are provided by Ports A and B. The starting address must be on an even binary multiple of the port depth. Figure 40 shows the ESF format for Port A and B Control Registers.

10.0 NMI CONTROL

The NMI Control logic generates an NMI signal when any of the following events occur:

1. Channel CHCK line asserted (Bit 3 = 0 of Control Port B at 0061H).
2. DRAM parity error (Bit 2 = 0 of Control Port B).
3. Watchdog Time-out (Enabled by programming the Timer).

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

TIMER		RESERVED			SP1		SP1		SP2		MODE	
TEST	NORM	—	—	—	PRI	ALT	ENA	DIS	ENA	DIS	EXTD	IBM

Figure 39. Peripheral Configuration Register Format (ESF:20 Read/Write)

= Default

PORT		COMMAND WIDTH SELECT			RESERVED	I/O SPACE DEPTH		
ENA	DIS	2	1	0	—	2	1	0

6	5	4	Width (NS) [1]
0	0	0	70
0	0	1	140
0	1	0	280
0	1	1	420
1	0	0	560
1	0	1	700
1	1	0	840
1	1	1	980

[1] Any IO device may extend the cycle beyond these times given by driving CDCHRDY (FE5010) inactive.

2	1	0	Bytes
0	0	0	2
0	0	1	4
0	1	0	8
0	1	1	16
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	Reserved

Figure 40. Port A or B Control Register (ESF:21, ESF:24 Read/Write—typical)

= Default

11.0 TECHNICAL SPECIFICATIONS

11.1 ABSOLUTE MAXIMUM RATINGS

These are absolute maximum stress ratings for the device. Permanent device damage can result from exposing the device to conditions exceeding these ratings.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	(V_{DD}–V_{SS})	0	7	V
Input Voltage	V_{IABS}	V_{SS}–0.3	V_{DD}+0.3	V
Bias on output pin	V_{OABS}	V_{SS}–0.3	V_{DD}+0.3	V
Storage Temperature	T_S	-40	125	°C

11.2 NORMAL OPERATING CONDITIONS

Exposure of the device to conditions exceeding the normal operating conditions for extended periods of time can affect the long term reliability of the device.

(V_{SS} = 0 V)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Power Supply Voltage	V_{DD}	4.5	5.5	V
Ambient Temperature	T_A	0	70	°C
Input Voltage	V_{IN}	-0.3	V_{DD}+0.3	V
Power Dissipation	P_W	—	TBD	mW
Supply Current	I_{DD}	—	TBD	mA

11.3 DC CHARACTERISTICS (UNDER NORMAL OPERATING CONDITIONS)

PARAMETER	SYMBOL	MIN	MAX	UNITS
*Input capacitance @ f_C= 1 MHz	C_I	—	10	pF
*I/O Capacitance	C_{IO}	—	15	pF
Logic high input voltage	V_{IH}	2.0	—	V
Logic low input voltage	V_{IL}	—	0.8	V
*Input leakage	I_{IL}	—	±10	uA
*Tri-state output leakage	I_{OL}	—	±30	uA
*I/O Pin Leakage	I_{IOL}	—	±40	uA
OUTPUTS MHZ14 and $\overline{\text{CHCK}}$				
*Source current @ V_{OH}= 2.4 V	I_{OH}	4	—	mA
*Sink current @ V_{OL}= 0.4 V	I_{OL}	24	—	mA
OUTPUTS $\overline{\text{CDSETUP}}$ [7:0]				
Source current @ V_{OH}= 2.4 V	I_{OH}	1	—	mA
Sink current @ V_{OL}= 0.4 V	I_{OL}	6	—	mA
ALL OTHER OUTPUTS				
*Source current @ V_{OH}= 2.4 V	I_{OH}	1	—	mA
*Sink current @ V_{OL}= 0.4 V	I_{OL}	4	—	mA

***Notes:**
Pins $\overline{\text{INT1EN}}$ and $\overline{\text{INT2EN}}$ have internal pulldowns of 10 K ohms nominal value. Measurements of input capacitance and input leakage values on these pins will be affected by these resistances.

$\overline{\text{CHCK}}$ is an open drain output. An external pullup is required. Only the sink current value applies.

NMI is an open source output. An external pulldown is required. Only the source current value applies.

12.0 TIMING

PARAM	DESCRIPTION	MIN	MAX	NOTE
T1	$\overline{CHS(1:0)}$ setup to $\overline{ADL}$ on	12	—	—
T2	$\overline{ADL}$ pulse width	40	—	—
T3	$\overline{CMD}$ active from $\overline{ADL}$ on	40	—	—
T4	$\overline{CHS(1:0)}$ hold from $\overline{ADL}$ off	25	—	—
T5	$\overline{CHS(1:0)}$ hold from $\overline{CMD}$ on	30	—	—
T6	SA(15:0) setup to ADL on	20	—	—
T7	SA(15:0) setup to $\overline{CMD}$ on	60	—	—
T8	SD(7:0) setup to $\overline{CMD}$ on	—	-25	1
T9	SA(15:0) hold from $\overline{CMD}$ off	0	—	—
T10	SD(7:0) hold from $\overline{CMD}$ off	0	—	—
T11	$\overline{CDSETEN}$ setup to $\overline{ADL}$ on	45	—	—
T12	$\overline{CDSETEN}$ hold from $\overline{ADL}$ off	25	—	—
T13	$\overline{CDSETEN}$ hold from $\overline{CMD}$ on	30	—	—
T14	$\overline{PROMCSL/H}$ setup to $\overline{CMD}$ on	25	—	—
T15	$\overline{PROMCSL/H}$ hold from $\overline{CMD}$ off	0	—	—
T16	$\overline{MIO}$ setup to $\overline{ADL}$ on	45	—	—
T17	$\overline{MIO}$ hold from $\overline{ADL}$ off	25	—	—
T18	$\overline{MIO}$ hold from $\overline{CMD}$ on	30	—	—
T19	$\overline{CDSFDBK}$ setup to $\overline{CMD}$ on	10	—	—
T20	$\overline{EDRENA}$ setup to $\overline{CMD}$ on	25	—	—
T21	$\overline{EDRENA}$ hold from $\overline{CMD}$ on	0	—	—
T25	$\overline{IOR/W}$, $\overline{MEMRD/WR}$ delay from $\overline{CMD}$ on	40	—	—
T26	$\overline{MEMRD/WR}$ pulse width	—	—	2
T26	$\overline{IOR/W}$, $\overline{CS8742}$	160	—	—
T26	$\overline{IOR/W}$, $\overline{FDCCS}$	90	—	—
T26	$\overline{IOR/W}$, $\overline{SERCS1}$, $\overline{SERCS2}$	125	—	—
T26	$\overline{IOR/W}$, $\overline{PPCS}$	125	—	—
T26	$\overline{IOR/W}$, $\overline{NPS1}$	90	—	—
T26	$\overline{IOR/W}$, $\overline{CSA}$, $\overline{CSB}$	70	980	—
T27	$\overline{IOR/W}$, $\overline{MEMRD/WR}$ off to $\overline{CMD}$ off	60	—	—
T28	$\overline{SDDTR}$ on from $\overline{ADL}$ on	0	40	—
T29	$\overline{SDDTR}$ setup to $\overline{SDEN}$ on	5	—	—
T30	$\overline{SDDTR}$ hold from $\overline{SDEN}$ on	5	—	—
T31	$\overline{SDEN}$ on from $\overline{CMD}$ on	5	—	—
T32	$\overline{SDEN}$ hold from $\overline{CMD}$ off	5	—	—
T33	SDCBA on from $\overline{CMD}$ on	40	—	—
T34	SDCBA off to $\overline{IOW/R}$, $\overline{MEMRD/WR}$ off	5	—	—
T35	$\overline{CHS(1:0)}$ on to IORDY off	—	20	—
T36	IORDY on to $\overline{CMD}$ off	60	—	—
T37	SD(7:0) read access from $\overline{IOR}$ on	25	—	—
T38	SD(7:0) read hold from $\overline{IOR}$ off	5	—	—
T39	CS (ext dev) setup to $\overline{IOR/R}$, $\overline{MEMRD/WR}$ on	70	—	—
T40	CS (ext dev) hold from $\overline{IOR/W}$, $\overline{MEMRD/WR}$ on	25	—	—
T41	$\overline{RTCRD}$, $\overline{RTCWR}$, $\overline{RTCAS}$ delay from $\overline{CMD}$ on	40	—	—
T42	$\overline{RTCRD}$, $\overline{RTCWR}$, $\overline{RTCAS}$ off to $\overline{CMD}$ off	60	—	—

PARAM	DESCRIPTION	MIN	MAX	NOTE
T43	RTCRD, RTCWR, RTCAS pulse width	325	—	—
T43A	CMOSA(12:0) on from CMD on	40	—	—
T44	CDSETUP(7:0) setup to ADL on	15	—	—
T45	CDSETUP(7:0) hold from ADL on	25	—	—
T46	CDSETUP(7:0) hold from CMD on	30	—	—

Table 10. Peripheral Bus Cycle (in nsec)

Notes: 1. The FE5000 allows SD bus valid to be later than CMD active.
2. T26 for MEMRD/WR follows CMD input.

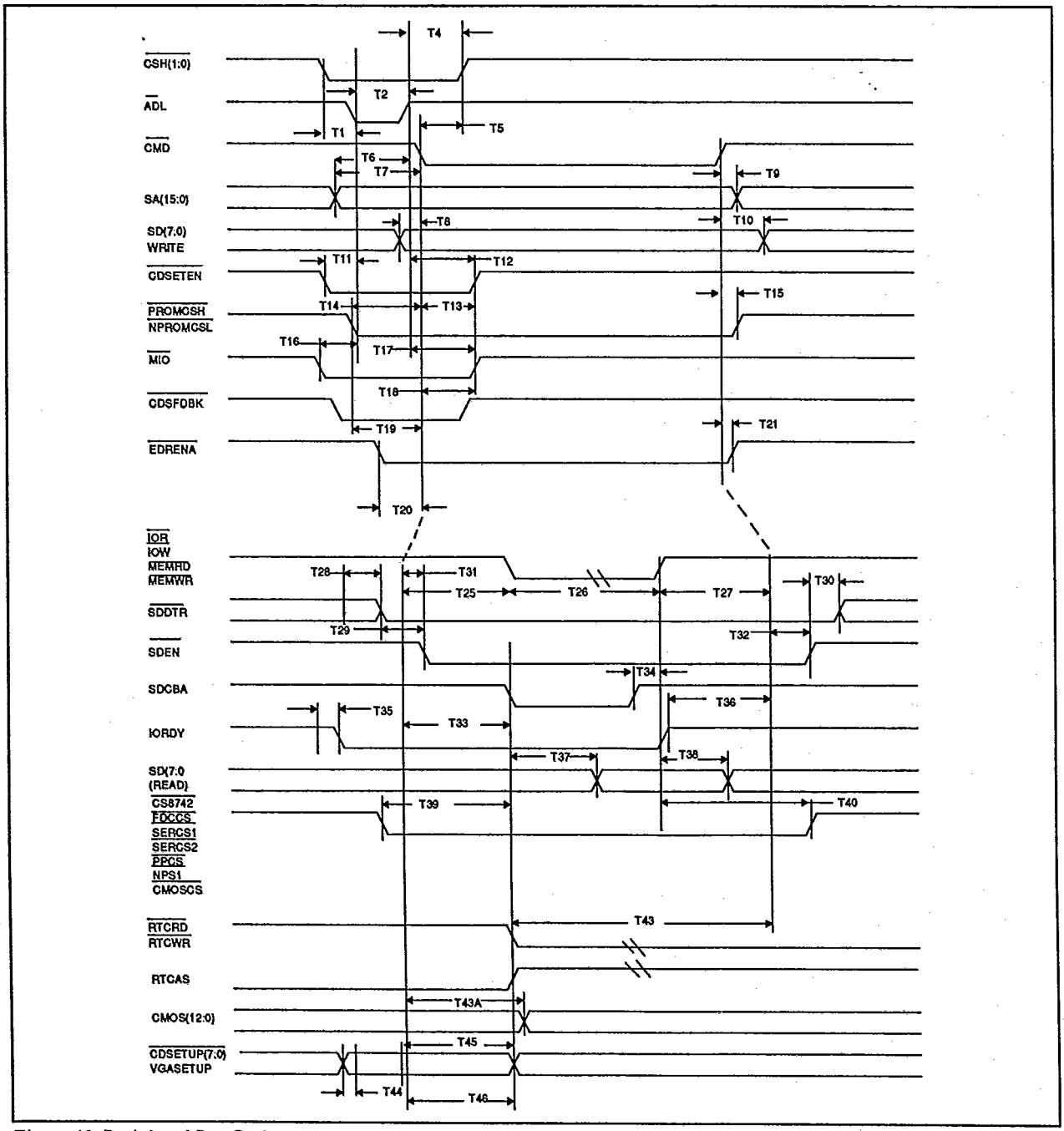


Figure 41. Peripheral Bus Cycle

PARAM	DESCRIPTION	MIN	MAX	NOTE
T1	MHZ28 period	35	—	—
T2	MHZ28 low time	17	—	—
T3	MHZ28 high time	16	—	—
T4	MHZ30 period	33	—	—
T5	MHZ30	18	—	—
T6	MHZ30 high time	15	—	—
T7	MHZ14 period	70	—	—
T8	MHZ14 high time	20	—	—
T9	MHZ14 low time	20	—	—
T10	CLK287 period	105/100	—	1
T10F	CLK287 rise time	—	10	3
T10R	CLK287 fall time	—	10	3
T11	CLK287 high time	28	—	4
T12	CLK287 low time	62	—	4
T13	CLK8742 period	105/100	—	1
T14	CLK8742 low time	33	—	—
T15	CLK8742 high time	33	—	—
T17	$\overline{\text{REFREQ}}$ period	15us	—	2

Table 11. Clock Cycle Times (in nsec except where noted)

Notes:
1. Clock derived from 28 MHZ, unless optional 30 MHZ is used.
2. 50% duty cycle.
3. Rise and fall times are measured between 0.8 V. AND 2.0 V.
4. Clock low time measured at 1.0 V, clock high time measured at 3.6 V.

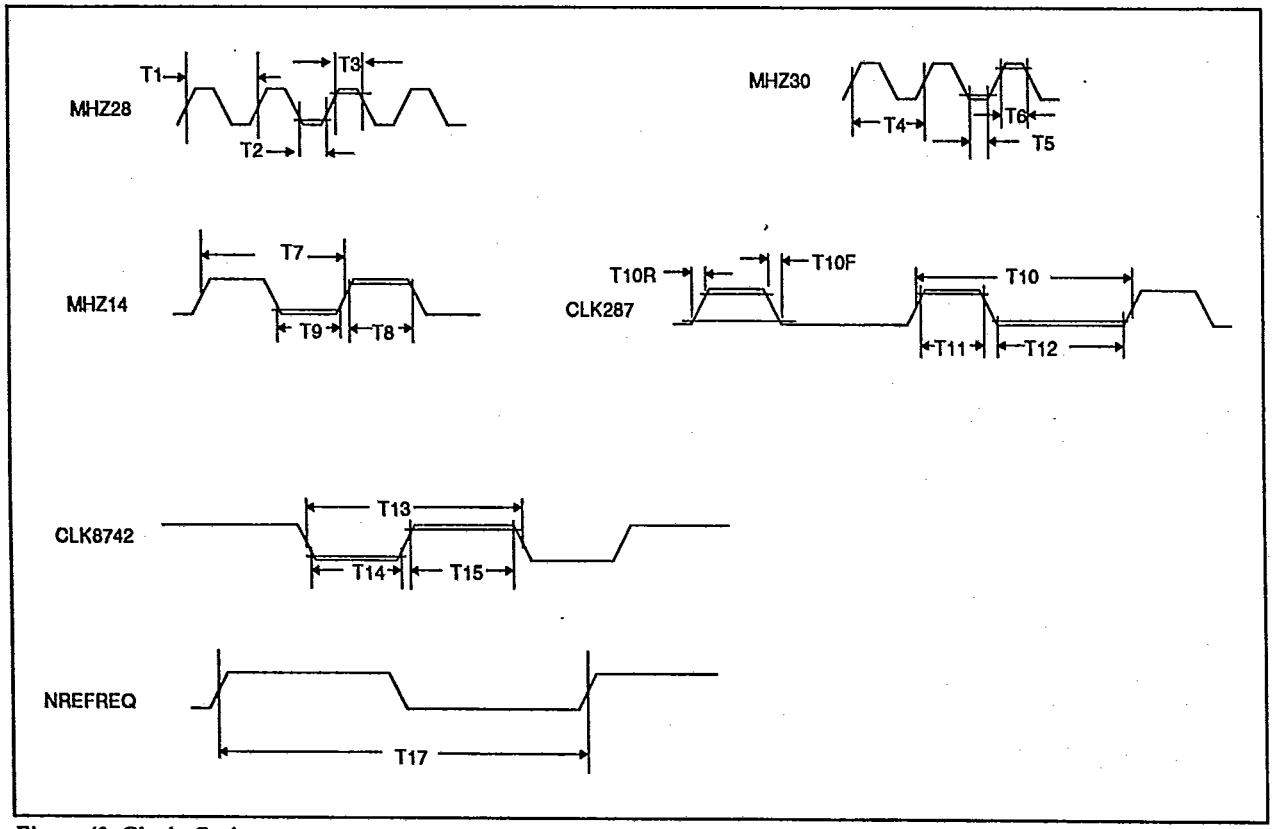


Figure 42. Clocks Cycle

PARAM	DESCRIPTION	MIN	MAX	NOTE
T1	INTR output delay	—	100	—
T2	INTR hold to INTACK on	10	32	1

Table 12. Interrupt Cycle (in nsec)

Note:
1. Interrupt inputs must be held until the first Interrupt Acknowledge cycle begins.

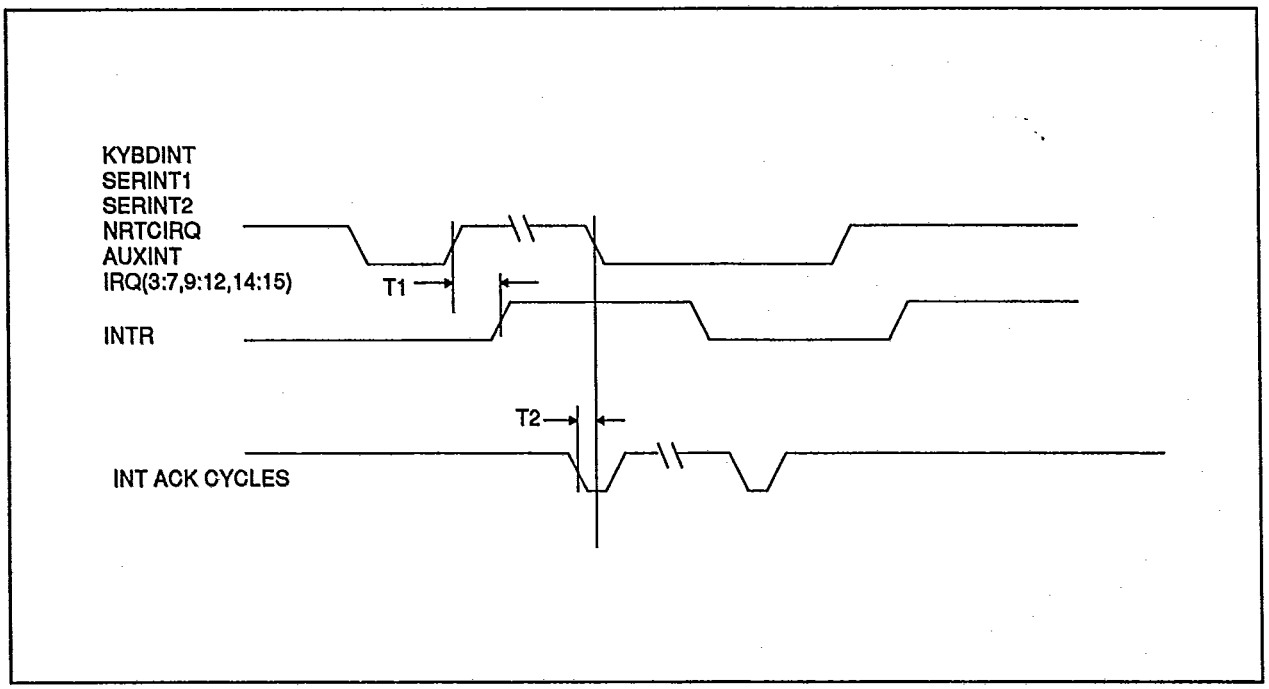


Figure 43. Interrupt Cycle

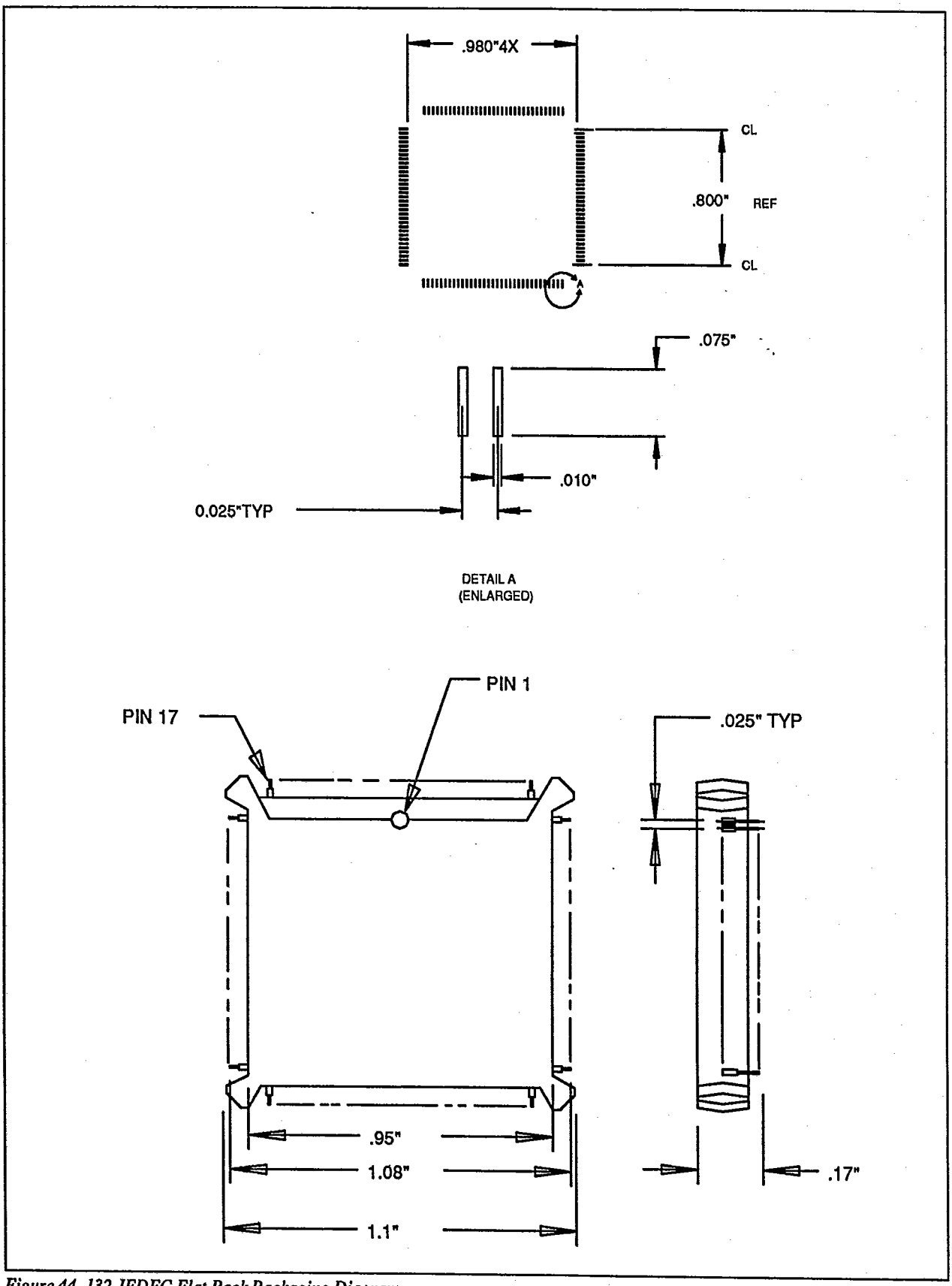
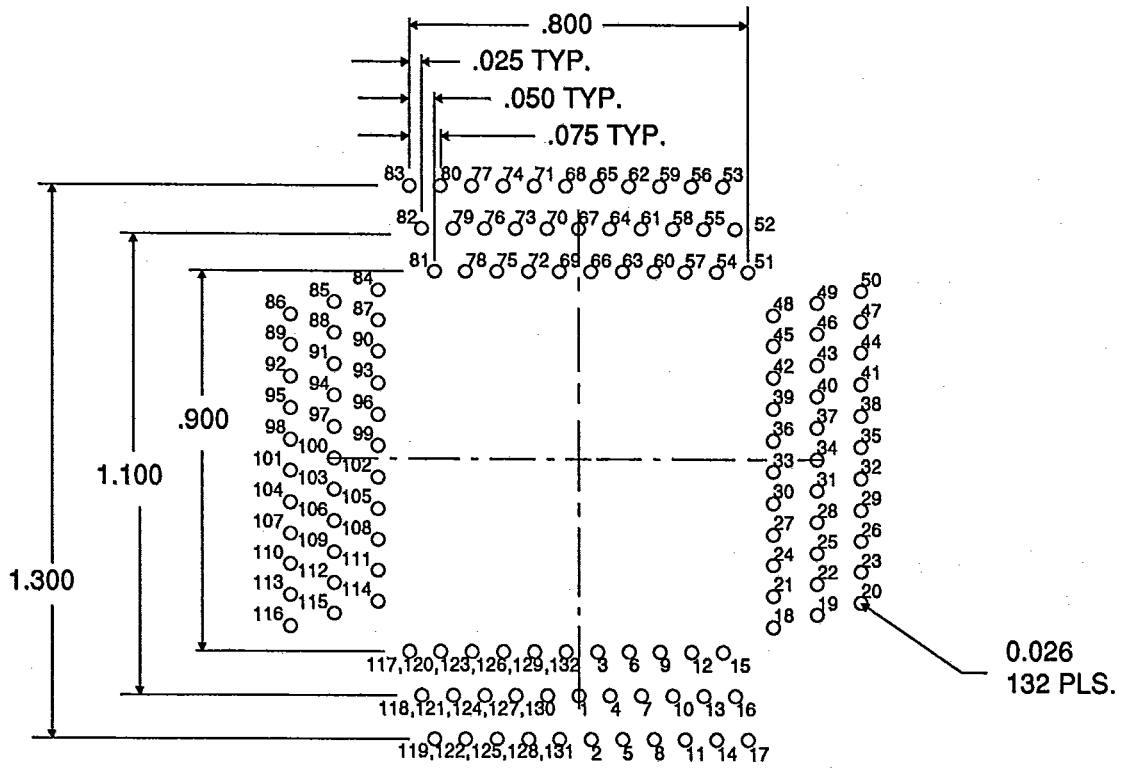


Figure 44. 132 JEDEC Flat Pack Packaging Diagram

T-52-33-15



RECOMMENDED P.C. BOARD HOLE PATTERN
SOCKET SIDE
132 POSN

Amp Incorporated
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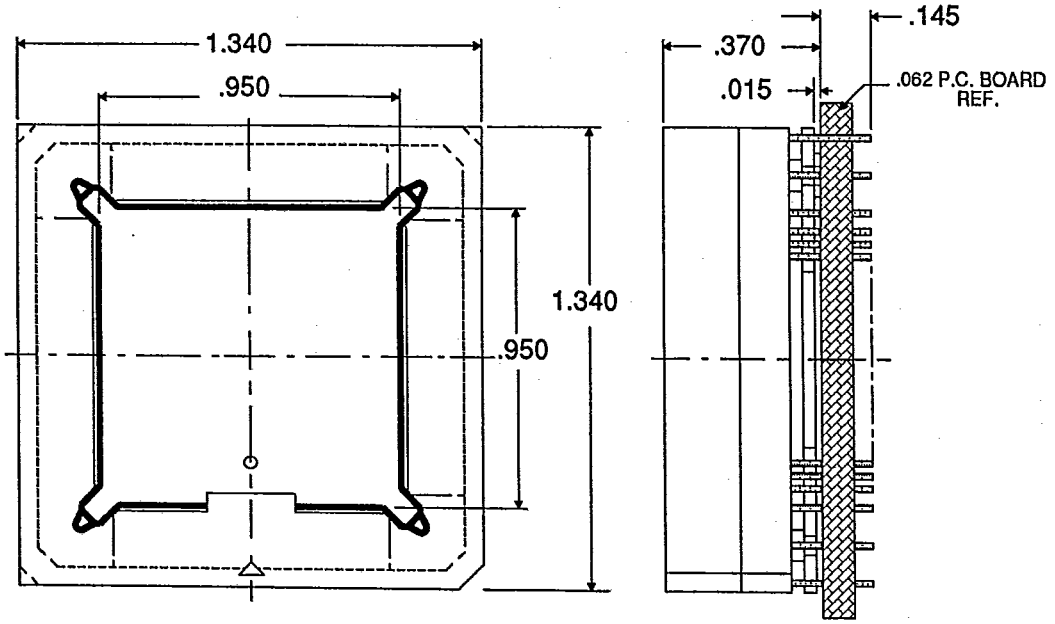

Figure 45. Socket Diagram