CMF040

TMS5220C Speech Synthesis Data Sheet

1987

Theory of Operation
Electrical Specifications

TEXAS INSTRUMENTS

TMS5220C

Speech Synthesis

Data Sheet

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1 Introduction

Texas Instruments Incorporated produces speech synthesis devices that are based on a pitch excited linear-predictive-coding (LPC) technique. Through the linear predictive coding, data that is derived from the original speech signal is converted to control parameters for a mathematical model of the vocal tract. This model is then implemented in a customized digital signal processor. The processor produces a series of digital sampled data that is a representation of an acoustic waveform. This waveform is converted to an analog electrical signal that is applied to a speaker to produce synthetic speech. The synthetic speech retains the inflections and voice characteristics of the original speech and does not have the robotic quality that is often associated with synthesis-by-rule systems.

Generation of the LPC control parameters, from a spoken word or phrase, requires the use of a Speech Development System (SDS), which is not discussed in this manual. For information concerning the use of an SDS, contact a Texas Instruments Regional Technology Center.

1.1 Description

The TMS5220C is an LPC-10 (Linear Predictive Coding with a tenth-order filter) voice synthesis function on a chip. A flexible interface structure allows a choice of data storage media for the model of the vocal tract. The interface also provides a means by which a microcontroller, external to the TMS5220C, can select the digital data. In addition to the TMS5220C, a TMS5220C based voice synthesizer system requires the following:

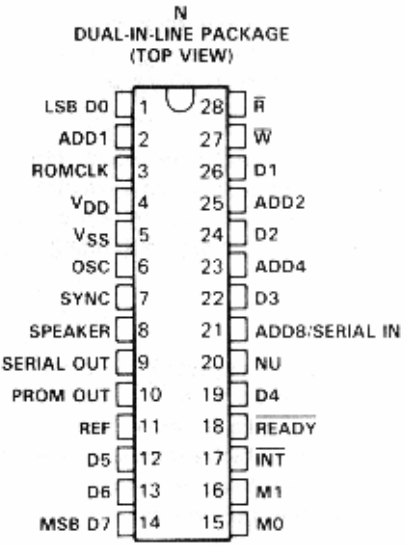
1. Storage device (e.g. ROM, RAM or TMS6100) for TMS5220C input data.
2. Host controller to direct the TMS5220C modes of operation. The host controller can be a microprocessor or an assembly of switches and simple digital logic. The overall system requirements dictate the complexity of the host controller.
3. Low-pass filter to remove switching noise from the TMS5220C output signal. A second order filter is adequate for many applications, but a higher order may be required for specific system requirements.
4. A speaker and buffer amplifier.

1.2 Key Features

- Pitch excited LPC-10 synthesis algorithm
- Choice of 4-kHz or 5-kHz voice input bandwidth
- Low data rate: 1000 to 1700 bps
- On chip 8-bit digital-to-analog converter
- Voice data input through either an 8-bit control/data bus land internal FIFO) that is primarily used with an external 8-bit host controller or a serial interface that is designed for use with a TMS6100 .

1.3 Pin Assignment and Description

Figure 1-1 shows the TMS5220C pin assignment. Table 1-1 is a pin functional description for the TMS5220C .



NU-Make no external connection

Figure 1-1. Pin Assignments

Table 1-1. Pin Functional Description

PIN NAME	NO.	I/O	DESCRIPTION
ADD1	2	O	Address 1 output (LSB) to a Voice Synthesis Memory
ADD2	25	O	Address 2 output to a Voice Synthesis Memory
ADD4	23	O	Address 4 output to a Voice Synthesis Memory
ADD8/SERIAL IN	21	I/O	Address 8 output (MSB) to a Voice Synthesis Memory or Serial Data Input
ROMCLK	3	O	Clock output to a Voice Synthesis Memory
D0	1	I/O	Memory data bit 0 (LSB)
D1	26	I/O	Memory data bit 1
D2	24	I/O	Memory data bit 2
D3	22	I/O	Memory data bit 3
D4	19	I/O	Memory data bit 4
D5	12	I/O	Memory data bit 5
D6	13	I/O	Memory data bit 6
D7	14	I/O	Memory data bit 7 (MSB)
$\overline{INT}$	17	O	Interrupt
M0	15	O	Command bit 0 to the Voice Synthesis Memory
M1	16	O	Command bit 1 to the Voice Synthesis Memory
OSC	6	I	Oscillator input
PROM OUT	10	O	Oscillator selector
$\overline{R}$	28	I	Read select
$\overline{READY}$	18	O	Data transfer cycle complete
V_{REF}	11	I	Ground reference voltage
SERIAL OUT	9	O	Serial data output
SPEAKER	8	O	Audio output
SYNC	7	O	Synchronization output
NU	20		Make no external connection
V_{DD}	4	I	−5 V supply voltage
V_{SS}	5	I	5 V supply voltage
$\overline{W}$	27	I	Write select

2 Theory of Operation

The TMS5220C accepts commands and filter parameters from the external host controller to produce synthetic speech. Figure 2-1 is a block diagram of the TMS5220C.

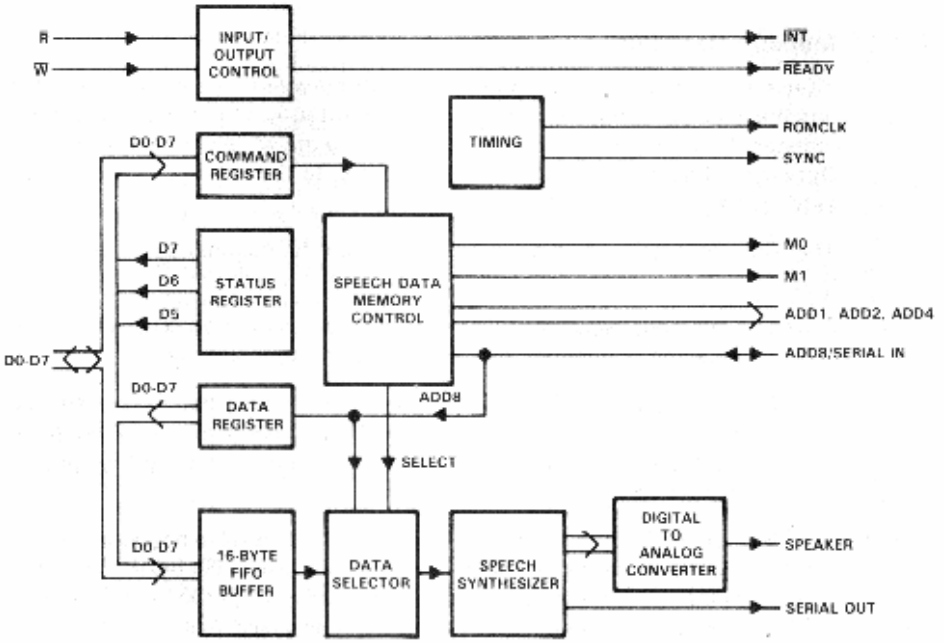


Figure 2-1. TMS5220C Voice Synthesizer Processor Block Diagram

2.1 Input/Output Structure

The TMS5220C input/output structure consists of the following sections:

1. Memory data bus interface — An 8-bit bus and read ($\overline{R}$), write ($\overline{W}$), interrupt ($\overline{INT}$), and ready ($\overline{READY}$) control signals that interface the TMS5220C to the host controller.

2. Speech ROM interface — A 4-bit address bus that interfaces the TMS5220C to a Vocabulary Read Only Memory (TMS6100 series). Address output ADD8 is also used to input serial speech data from the TMS6100 or other memories. Clock and control signals are provided for memory control.

3. Speech Output — Synthesized speech data is provided in an analog and a digital format. The analog signal comes from a current source and is discussed later. The digital speech is provided as a serial-bit stream. Clock and synchronizing signals are provided with the digital speech output.

2.1.1 Memory Data Bus

The memory data bus is an 8-bit wide path between an external controller and the registers in the TMS5220C. Data is written into the command or FIFO registers from the external controller by setting the write command ($\overline{W}$) low. Data is read from the data or status registers, to the external controller, by setting the read command ($\overline{R}$) low.

The four TMS5220C registers that interface to the memory data bus are as follows:

1. Command register — The command register is an 8-bit latch that receives commands from an external host controller.

2. FIFO register — The first-in first-out 16-byte register receives, via the memory data bus, byte wide speech data from the host controller. In addition, it outputs serial speech data to the speech synthesizer.

3. Data register — The data register is an 8-bit serial-in parallel out latch that receives serial speech data from a TMS6100 ROM. The data is buffered into parallel byte-wide words and put into the memory data bus for output to the external controller.

4. Status register (flags) — The status register is a 3-bit register that contains data on the status of the TMS5220C. The 3 bit status word is put onto the memory data bus so that it can be accessed by an external host controller.

The 8-bit memory data bus has internal pullup resistors.

2.1.1.1 Command Register

The command register receives command data from the memory data bus and holds it for the internal controller to interpret and execute. The TMS5220C acts as an attached processor to the host controller and performs its synthesis tasks when appropriate commands are sent by the host controller.

2.1.1.2 FIFO Register

The 128 bit FIFO register is organized as a 16-byte parallel-in serial-out buffer. This buffer is used to hold speech data which is input by the host controller after it has issued a Speak External command to the TMS5220C .

The synthesis section requires the data to be shifted out serially starting with the LSB from the first-in byte. A stack pointer keeps track of the location of the last-in byte. Within 50 μs after the FIFO becomes less than half full, the Buffer Low (BL) status flag is set and the interrupt signal ($\overline{INT}$) goes low. This indicates to the host controller that more data should be provided to the TMS5220C . If the buffer empties completely, the Buffer Empty (BE) status flag is set and the Talk Status (TS) flag is reset causing speech to terminate immediately. To resume speech, with data provided by the host controller, another Speak External command must be issued. The FIFO buffer is cleared at the beginning and end of the Speak External command. Also, the Reset command and the Power-Up Clear sequence will clear the buffer, reset $\overline{INT}$ to high and reset the status flags.

2.1.1.3 Data Register

The 8 bit data register is organized as a serial-in parallel-out holding register. The TMS5220C uses the register, during the execution of a Read Byte command, to convert the serial data from the TMS6100 to an 8-bit data word. This data is available to be read by the external controller (but not by the TMS5220C FIFO). The timing requirements to input the Read Byte command and to read the data from the memory data bus are defined in Section 4.

The first bit of serial data into the data register goes to the byte's most significant bit (D7). However, the serial data out of the FIFO buffer starts with the least significant bit. Therefore, if speech data is read from a TMS6100 using the Read-Byte command and then written back to the FIFO using the Speak External command, the byte must be bit reversed by the external controller.

2.1.1.4 Status Register

The three bits of the status register provide information on the state of the TMS5220C to the external controller. The status register can be read at any time by taking the Read ($\overline{R}$) input low. However, it should not be read immediately following a Read Byte command. When $\overline{R}$ goes low, the TMS5220C sends status data to the memory data bus. When the data is stable, the $\overline{READY}$ signal goes low. However, the TMS5220C is not ready to accept another read or write command for at least 12 μs. Table 2-1 describes the three status register bits and shows their corresponding memory data bus bits.

Table 2-1. Status Register Bits

MEMORY DATA BUS BIT	STATUS REGISTER BIT	DESCRIPTION
D7	TS	Talk Status (TS) is active (high) when the TMS5220C is processing speech data. It goes high at the initiation of a Speak command or after nine bytes of data are loaded into the FIFO buffer following a Speak External command. It goes inactive (low) when the stop code (Energy = 1111) is processed, a Buffer Empty (BE) condition occurs, or by a Reset command is invoked. When TS goes low, the audio output will be ramped down to zero and will be terminated on the next frame boundary.
D6	BL	Buffer Low is active (high) when the FIFO buffer is less than half full. Buffer Low is cleared when data is loaded so that the FIFO is more than half full. After the FIFO receives the ninth data byte (FIFO more than half full) in the Speak External mode, there is a delay of 50 μs before BL is set low.
D5	BE	Buffer Empty (BE) is active (high) when the FIFO buffer has run out of data while the TMS5220C is executing a Speak External command. BE is set when the last bit of the last byte in the FIFO is shifted out to the synthesis section. This causes Talk Status to be cleared. Speech is terminated at some abnormal point and the Speak External command execution is terminated. Data written to the memory data bus by the external controller will be routed to the command register.

2.1.1.5 Read and Write Signal Inputs

Activity on the memory data bus is controlled by the Read ($\overline{R}$) and Write ($\overline{W}$) inputs as shown in Table 2-2.

Table 2-2. Read and Write Functions

$\overline{R}$	$\overline{W}$	FUNCTION
H	H	TMS5220C output buffers are in a high-impedance state.
H	L	The external controller is inputting data to the command register or the FIFO.
L	H	The external controller is reading data from the data register or the status register.
L	L	Hardware Clear.

Note: A read cycle cannot be completed while $\overline{W}$ is low and a write cycle cannot be completed while $\overline{R}$ is low.

A hardware clear is performed by simultaneously holding $\overline{R}$ and $\overline{W}$ low for 1 ms. The effects are similar to a Reset command. Talk Status is cleared and any speech activity is halted. The FIFO buffer is purged (BL and BE go high). The input/output multiplexers are set to allow data to be written to the command register and read from the status register. An interrupt may be generated and should be ignored at this time.

2.1.1.6 Ready Signal Output

The TMS5220C is a slow memory device (i.e., it cannot properly respond to read/write cycle times of most controllers). Therefore, external controller wait states are required to successfully complete a read/write cycle. The TMS5220C uses the ready line to signal the controller to execute wait states until incoming data has been read or output data is stable.

The ready output goes high 100 ns after $\overline{R}$ or $\overline{W}$ goes low. A high $\overline{READY}$ signal lets the external controller know that the data transfer cycle is not complete. When the TMS5220C has established stable data on the memory data bus (for $\overline{R}$) or has completed latching data in from the bus (for $\overline{W}$), the $\overline{READY}$ signal goes low indicating that the controller may terminate the data transfer cycle. However, the TMS5220C is not ready to accept another $\overline{R}$ or $\overline{W}$ command for at least 12 μs.

2.1.1.7 Interrupt Signal Output

The interrupt signal ($\overline{INT}$) indicates changes in the status of the TMS5220C that may require attention from the external controller. $\overline{INT}$ goes high when the status register is read or if the Reset command is executed. $\overline{INT}$ goes low when Talk Status (TS) makes a high-to-low transition. However, if the TS

transition is during a Read cycle, the $\overline{INT}$ signal will not go low until the cycle is completed. In addition, $\overline{INT}$ goes low when buffer low (BL) makes a low-to-high transition indicating that more phrase data is needed by the FIFO buffer for the Speak External command.

2.1.2 Speech ROM Interface

The Speech ROM interface is designed to minimize the interface hardware between the TMS5220C and TMS6100. This interface consists of the memory address lines, the ROM clock (ROMCLK), and two memory control lines (M0 and M1). Detailed timing information is contained in the TMS6100 Data Manual.

2.1.2.1 Memory Address

Memory address is a 4-bit parallel bus (ADD8, ADD4, ADD2, ADD1) that provides addressing information to the TMS6100 and data transfer back to the TMS5220C. The speech data from the TMS6100 is a serial bit stream that is multiplexed onto the ADD8 line.

2.1.2.2 ROM Clock

The TMS5220C oscillator (OSC) is divided by 4 to produce the ROM clock (ROMCLK). This a continuous clock that is used by the TMS6100.

2.1.2.3 Memory Control Outputs

The M0 and M1 outputs control the addressing of data in the TMS6100. Table 2-3 lists the functions performed.

Table 2-3. Memory Control Function

M0	M1	FUNCTION
L	L	Idle. TMS6100 in nonoperating state.
L	H	Load address. The four bits (one nibble) of data on ADD8, ADD4, ADD2, and ADD1 are loaded into the TMS6100. Five nibbles are loaded to complete address loading (14 bits select a byte in the ROM, 4 bits are used for chip select, and 2 bits are not used).
H	L	Read. The first Read command after the Load Address is a dummy command that is used to reset a pointer internal to the TMS6100. Each Read command after the first one will cause a speech data bit to be placed on ADD8.
H	H	Read and Branch. The TMS6100 uses the current address input by the Load Address command as an indirect address for access to the start of the speech data.

2.1.3 Speech Output

The TMS5220C outputs speech data in both an analog and a digital format. Since the device is a digital processor, the analog signal is derived through a digital-to-analog converter.

2.1.3.1 Digital-to-Analog Conversion

The TMS5220C has an 8-bit digital-to-analog converter. Every sample period (125 μs for 8 kHz sampling) a new data point is converted into a current output of 0 to 1.5 mA. As shown in Figure 2-2, 0 represents the most negative speech amplitude shown.

A 3.9-kΩ resistor from the Speaker output to V_{DD} will convert the speech current to an output voltage. The voltage across the resistor will have a DC offset which can be eliminated by capacitively coupling the speech signal to filter and amplifier stages.

2.1.3.2 Digital Audio

The digital speech which is being fed to the analog-to-digital converter is also available at the Serial Out terminal on the TMS5220C. The speech is a 2's compliment value and each bit is stable when ROMCLK makes a high-to-low transition. The Sync signal provides a means of locating the speech data within a frame that is defined by 20 cycles of ROMCLK. Figure 2-3 illustrates digital speech data timing.

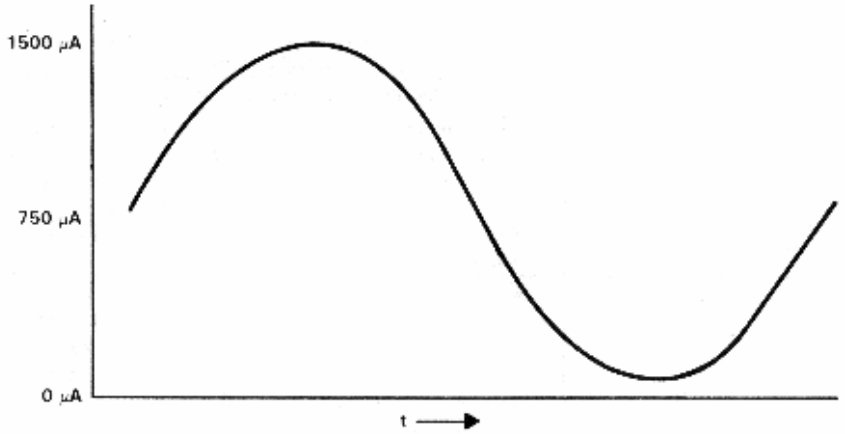


Figure 2-2. Speech Signal from Analog-to-Digital Converter

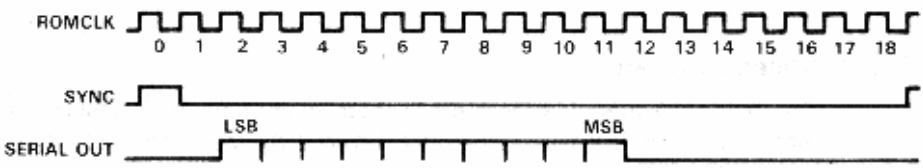


Figure 2.3. Digital Speech Data Timing

3 External Controller Commands

The external controller sends commands to the TMS5220C to specify the functions that are to be performed. The controller must know the TMS5220C operating mode. If the controller has the TMS5220C in the Speak External mode, the data placed on the memory data bus is interpreted as speech data and not as a command. The external controller puts the command on the memory data bus and pulls $\overline{W}$ low. The TMS5220C sets $\overline{READY}$ high to indicate that it is busy reading the command. When $\overline{READY}$ goes low, the TMS5220C has accepted the command. A new command can be sent to the TMS5220C after the wait time specified in Table 4-3. The commands that are available for use by the external controller are shown in Table 3-1.

Table 3-1. TMS5220C Commands and Command Format

COMMAND	COMMAND FORMAT (DATA ON MEMORY BUS)							
	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
Load Address	X	1	0	0	A	A	A	A
Speak	X	1	0	1	X	X	X	X
Speak External	X	1	1	0	X	X	X	X
Read Byte	X	0	0	1	X	X	X	X
Read and Branch	X	0	1	1	X	X	X	X
Reset	X	1	1	1	X	X	X	X

3.1 Load Address Command

The Load Address command allows the external controller to alter the address register in the TMS6100 to point to new speech data. Each Load Address command modifies four bits (one nibble) of the TMS6100 address register starting with the least-significant nibble.

Table 3-2 lists the Load Address command required to address the TMS6100 memories. Five consecutive Load Address commands are required to load a 4-bit chip select-address (selects 1 of 16 TMS6100 memory devices) and a 14-bit address (selects 1 byte in the selected TMS6100). The chip-select address is mask-programmed during the manufacture of the memory device. Preprogrammed off-the-shelf memory devices generally have a chip-select address of 0000.

Table 3-2. Load-Address Sequence

BYTE TO TMS6100	LOAD ADDRESS COMMAND				BYTE ADDRESS			
	D7	D6	D5	D4	D3	D2	D1	D0
FIRST	X	1	0	0	A3	A2	A1	A0
SECOND	X	1	0	0	A7	A6	A5	A4
THIRD	X	1	0	0	A11	A10	A9	A8
FOURTH	X	1	0	0	CS1	CS0	A13	A12
FIFTH	X	1	0	0	X	X	CS3	CS2

Where: X = Don't care
A0 through A13 = speech data address
CS0 through CS3 = chip address

3.2 Speak Command

The Speak command allows speech data to be generated from phrase data stored in the TMS6100. This command generates an internal signal that immediately causes Talk Status to be set and initiates speech synthesis calculations using the next available data from the TMS6100. Audio output begins on the following frame boundary. The TMS5220C continues to retrieve data from the TMS6100 and generates speech output until a stop code (Energy = 1111) is received and recognized. On the next frame boundary, the Talk Status is cleared and execution of the Speak command is completed.

The Reset command causes immediate termination of the Speak command and clears Talk Status. Audio output halts immediately without waiting for a frame boundary.

3.3 Speak External Command

This command allows the external controller to supply speech data to the TMS5220C from some memory other than the TMS6100. Upon receipt of a Speak External command, the following occur:

1. The TMS5220C purges the FIFO buffer
2. BL and BE go high causing an interrupt to be generated
3. Data put on the memory data bus by the external controller is routed to the FIFO buffer
4. When the BL status becomes false (a minimum of 9 bytes have been loaded into the FIFO) Talk Status is set and speech synthesis calculations begin using data from the FIFO buffer.

5. Data continues to be taken from the FIFO buffer until a stop code (Energy = 1111) or the BE abnormal termination occurs.

After executing a Speak External command, all data that is transferred to the TMS5220C goes into the FIFO buffer until a stop code (Energy = 1111) is read by the TMS5220C, a BE status occurs, or a hardware clear occurs.

3.4 Read Byte Command

The Read Byte command allows the external controller to access the next eight bits from the TMS6100 (byte boundaries are ignored). To access data or text at a particular address, the full address is first loaded into the TMS6100 using the Load Address command.

3.5 Read and Branch Command

The Read and Branch command allows the TMS5220C to access speech data via an indirect addressing scheme. This feature is typically used in conjunction with a look-up table that is stored in the TMS6100. Each look up table entry occupies two bytes.

The advantage of this approach is in the use of standardized software and hardware for different applications. One example is the use of several languages in a common control system. Each word for the different languages is stored in the same place in the look-up table contained in each TMS6100.

To perform the Read and Branch operation, the look-up table address is first loaded into the TMS6100 address register with Load Address commands. Execution of the Read and Branch command ends with the TMS6100 ready to read speech data starting at the address pointed to by the address contained in the look-up table. This command cannot be used in multiple TMS6100 applications.

3.6 Reset Command

The Reset command allows the external controller to halt the Speak command and to put the TMS5220C into a known state. Reset performs the following functions:

1. Clears the Talk Status and halts speech activity immediately
2. The FIFO buffer is purged (BE and BL go high)
3. The Input/Output paths are set to their default condition so that a Write signal ($\overline{W}$) will put data on the memory data bus into the Command register and a Read signal ($\overline{R}$) will put the contents of the Status register onto the memory data bus.

4. The Interrupt line ($\overline{INT}$) goes high.

The Reset command cannot halt a Speak External command because it will be interpreted as speech data. A hardware reset will stop a Speak External command.

The Reset command can require up to 800 ms to complete the register clearing operations. The Hardware Reset only takes 1 ms for the same function.

4 System Timing

This manual describes all TMS5220C timing at an 8-kHz sample rate of the original spoken speech. This rate requires the system clock to run at 640 kHz if the internal RC oscillator is used or at 320 kHz if an external clock is provided. Variations from this rate will cause the pitch of the speech to vary. A system timing comparison for 8 kHz and 10 kHz sampling rates is provided in Table 4-1.

Table 4-1. System Timing Comparison

PARAMETER	10-kHz SAMPLE RATE	8-kHz SAMPLE RATE	UNIT
Frame period (200 samples/frame)	20	25	ms
Sample rate	10	8	kHz
Sample period	100	125	μs
ROM clock rate	200	160	kHz
ROM clock period	5	6.25	μs
RC oscillator rate	800	640	kHz
RC oscillator period	1250	1562.5	ns

4.1 System Clock

The two possible sources for the System Clock are the internal RC oscillator or an external 0-V to 5-V clock. The internal RC oscillator is active when the PROMOUT output is open, connected to V_{REF} or V_{DD}. PROMOUT is connected to V_{SS} for operation with an external clock.

An external resistor [Figure 4-1(a)] sets the internal oscillator frequency. The oscillator can be adjusted to correspond to the sampling frequency that was used when the speech was encoded. Use of a shunt capacitor is recommended to prevent circuit layout and environmental noise from affecting device operation. To adjust the oscillator, monitor the frequency at ROMCLK. This buffered output, which is one-fourth the oscillator frequency, is not affected by the input capacitance of the measurement equipment.

An external clock can be applied to the OSC input [Figure 4-1(b)]. The clock input signal must be 0 V to 5 V with a frequency of 320 kHz for an 8-kHz sampling rate.

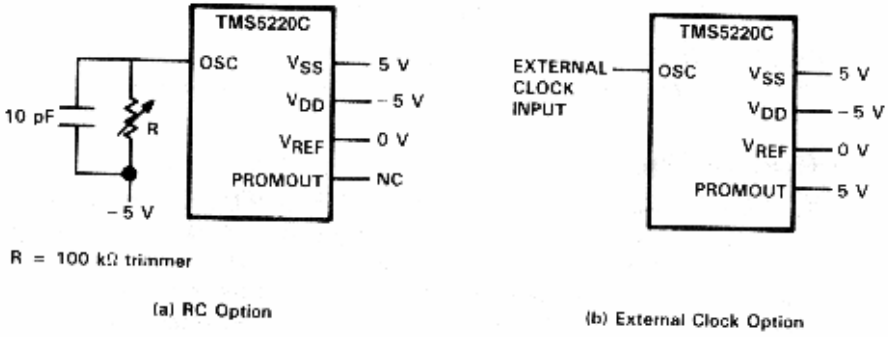


Figure 4-1. System Clock

4.2 Power-Up Sequence

The power supply voltages (V_{DD} and V_{SS}) must be stable within 2 ms for proper initialization of the TMS5220C. If the power-up transition takes longer than 2 ms, a hardware reset must be generated after the voltages have stabilized. Figure 4-2 shows the power-up sequence timing waveforms. Table 4-2 lists the power-up sequence timing requirements.

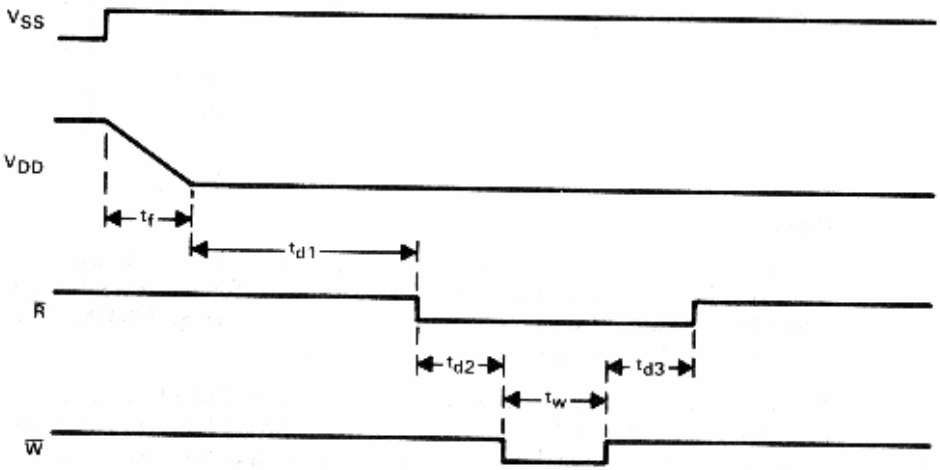


Figure 4-2. Power-Up Sequence Timing Diagram

NOTE: When Read and Write are both low, the data bus (D0 thru D7) will go low.

Table 4-2. Power-Up Sequence Timing Requirements

PARAMETER		MIN	MAX	UNIT
t_f	Fall time, V_{DD}		2	μs
t_w	Pulse duration, $\overline{W}$	200		ns
t_{d1}	Delay time, V_{DD} low to $\overline{R}$ low	5		μs
t_{d2}	Delay time, $\overline{R}$ low to $\overline{W}$ low		50	ns
t_{d3}	Delay time $\overline{W}$ high to $\overline{R}$ high		50	ns

4.3 Write Cycle for Commands

The timing requirements for Read-and-Branch, Load Address, Speak, Speak External, and Reset commands are shown in Figure 4-3 and listed in Table 4-3.

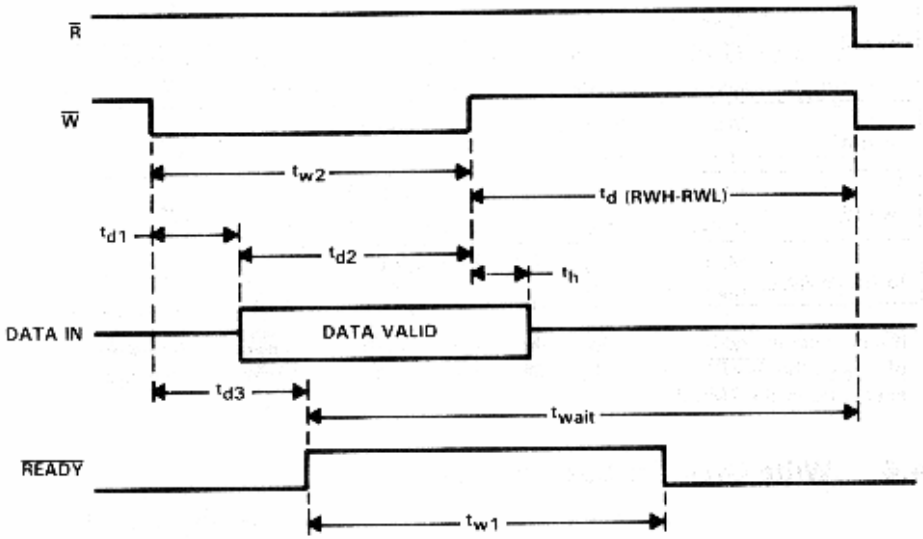


Figure 4-3. Write Cycle for Commands Timing Diagram

Table 4-3. Write Cycle for Commands Timing Requirements

PARAMETER			MIN	MAX	UNIT
t_{d1}	Delay time, $\overline{W}$ low to data valid			3	μs
t_{d2}	Delay time, data in valid to $\overline{W}$ high		200		ns
t_{d3}	Delay time, $\overline{W}$ low to $\overline{READY}$ high			100	ns
t_h	Hold time, $\overline{W}$ high to data in		100		ns
t_{w1}	Pulse duration, $\overline{READY}$ high		18	26	μs
t_{w2}	Pulse duration, $\overline{W}$ low		200		ns
t_{wait1}	Wait time, Read and Branch Command from $\overline{READY}$ high to next allowable command†		595		μs
t_{wait2}	Wait time, Load Address Command from $\overline{READY}$ high to next allowable command†		42		μs
t_{wait3}	Wait time, Speak Command from $\overline{READY}$ high to next allowable command	Preceded by Load Address Command	287		μs
		Not preceded by Load Address Command	56		
t_{wait4}	Wait time, Speak External Command high to next allowable command†		42		μs
t_{wait5}	Wait time, Reset Command from $\overline{READY}$ high to next allowable command†		800		ms
$t_{d\ (RWH-RWL)}$	Minimum time from $\overline{R}$ (or $\overline{W}$) high to the next $\overline{R}$ (or $\overline{W}$) low		12		μs

† If a new command is issued prior to the completion of the present command (before the end of t_{wait}), the $\overline{READY}$ signal will go high and stay high until the present command is finished executing in the TMS5220C.

4.4 Write Cycle for Speech Data

The timing requirements for speech data input after the Speak-External command has been invoked are shown in Figure 4-4 and listed in Table 4-4.

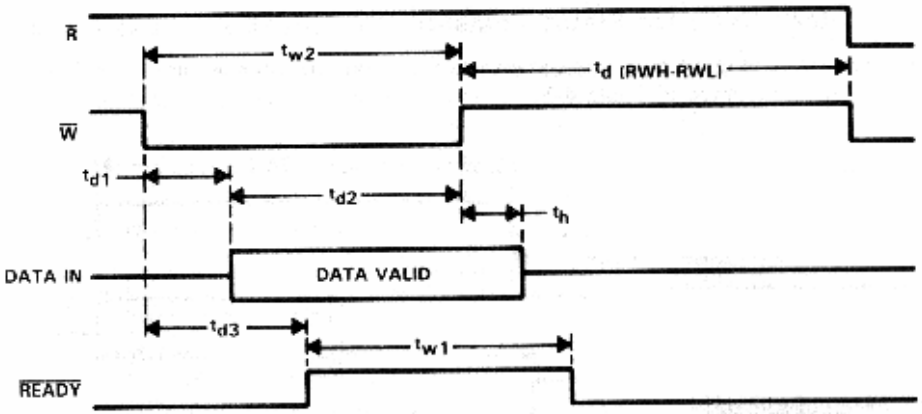


Figure 4-4. Write Cycle for Speech Data Timing Diagram

Table 4-4. Write Cycle for Speech Data Timing Requirements

PARAMETER		MIN	MAX	UNIT
t_{d1}	Delay time, $\overline{W}$ low to data valid		3	
t_{d2}	Delay time, data invalid to $\overline{W}$ high	200		ns
t_{d3}	Delay time, $\overline{W}$ low to $\overline{READY}$ high		100	ns
t_h	Hold time, $\overline{W}$ high to data in	100		ns
t_{w1}	Pulse duration, $\overline{READY}$ high	18	26	µs
t_{w2}	Pulse duration, $\overline{W}$ low	200		ns
$t_{d\ (RWH-RWL)}$	Minimum time from $\overline{R}$ (or $\overline{W}$) high to the next $\overline{R}$ (or $\overline{W}$) low	12		µs

4.5 Read Cycle for Status Transfer

The read cycle timing requirements for status transfer are shown in Figure 4 5 and listed in Table 4-5.

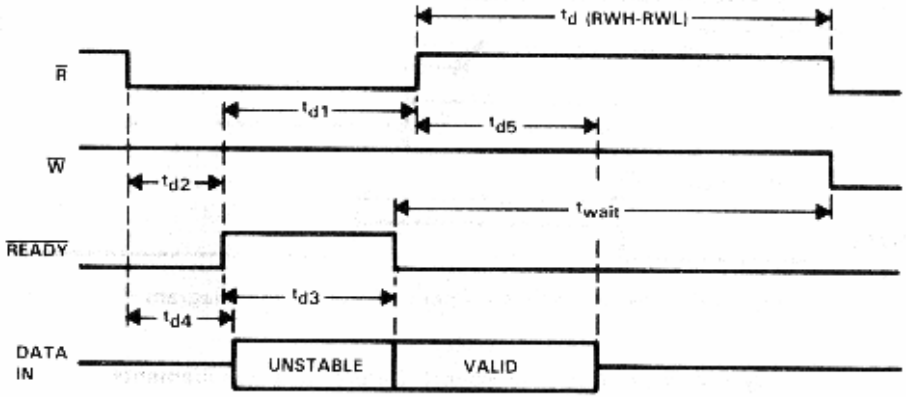


Figure 4-5. Read Cycle for Status Transfer Timing Diagram

Table 4-5. Read Cycle for Status Transfer Timing Requirements

PARAMETER		MIN	MAX	UNIT
t_{d1}	Delay time, $\overline{READY}$ high to $\overline{R}$ high	6		μs
t_{d2}	Delay time, $\overline{R}$ low to $\overline{READY}$ high		100	ns
t_{d3}	Delay time, $\overline{READY}$ high to data valid (stable)	6	11	μs
t_{d4} †	Delay time, $\overline{R}$ low to data bus driven (output unstable)			μs
t_{d5}	Delay time, $\overline{R}$ high to data output disabled	2	10.5	μs
t_{wait}	Wait time, $\overline{R}$ low to next allowable command	12		μs
$t_{d\ (RWH-RWL)}$	Minimum time from $\overline{R}$ (or $\overline{W}$) high to the next $\overline{R}$ (or $\overline{W}$) low	12		μs

†The typical value of t_{d4} is equal to $t_{d3} - 2$ μs.

4.6 Read-Byte Sequence

The Read-Byte timing requirements for reading data from the Data register are shown in Figure 4-6 and listed in Table 4-6.

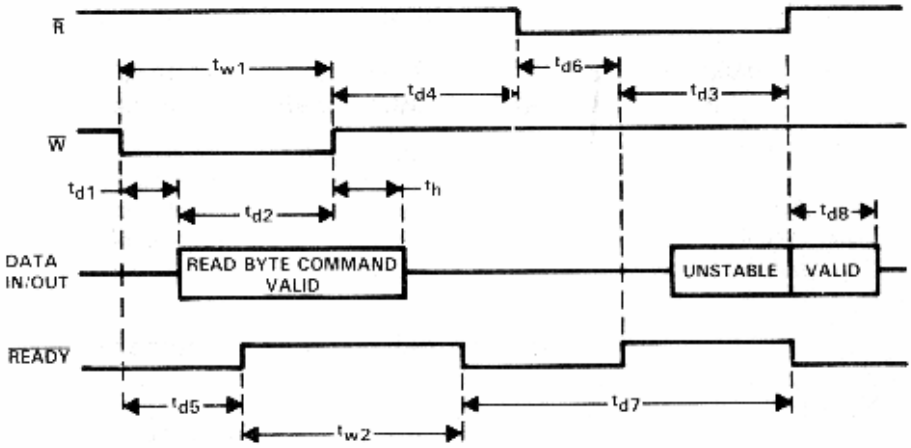


Figure 4-6. Read-Byte Sequence Timing Diagram

Table 4-6. Read-Byte Sequence Timing Requirements

	PARAMETER		MIN	MAX	UNIT
t_{d1}	Delay time, $\overline{W}$ low to data valid			3	μs
t_{d2}	Delay time, data valid to $\overline{W}$ high		200		ns
t_{d3}	Delay time, $\overline{READY}$ high to $\overline{R}$ high		8		μs
t_{d4}	Delay time, $\overline{W}$ high to $\overline{R}$ low		12		μs
t_{d5}	Delay time, $\overline{W}$ low to $\overline{READY}$ high			100	ns
t_{d6}	Delay time, $\overline{R}$ low to $\overline{READY}$ high			100	ns
t_{d7}	Delay time, $\overline{READY}$ low	No previous Load Address Command		320	μs
	(write) to $\overline{READY}$ low (read)	Previous Load Address Command		440	
t_{d8}	Delay time, $\overline{R}$ high to data output disabled		4	9	μs
t_h	Hold time, data in after $\overline{W}$ high		100		ns
t_{w1}	Pulse duration, $\overline{W}$ low		200		ns
t_{w2}	Pulse duration, $\overline{READY}$ high (write)			26	μs

5 Electrical Characteristics

5.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)

Any pin with respect to V_{SS} . . . . . −15 V to 0.3 V
Continuous total dissipation . . . . . 600 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −40°C to 70°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds 260°C

5.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{SS}	4.75	5	5.25	V
Supply voltage, V_{REF}		0		V
Supply voltage, V_{DD}	5.25	-5	-4.75	V
High-level input voltage, V_{IH} (see Note 1)	V_{SS}-0.6		V_{SS}	V
Low-level input voltage, V_{IL} (see Note 2)	V_{DD}		V_{SS}-4	V
Operating free-air temperature, T_A	0		70	°C
Operational frequency (external RC)	620		825	kHz

NOTES: 1. Pullup resistors are provided on all data and select inputs. This permits direct drive from TTL-compatible devices.
2. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic voltage levels only.

5.3 Electrical Characteristics Over Full Range of Operating Conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	D0-D7, $\overline{W}$, $\overline{R}$, $\overline{INT}$	I_{OH} = 0.4 mA	2.4		V_{SS}	V
		ROMCLK, ADD1-ADD8, M0, M1	I_{OH} = 100 μA	V_{SS} − 0.5		V_{SS}	
V_{OL}	Low level output voltage	D0-D7, $\overline{W}$, $\overline{R}$, $\overline{INT}$	I_{OL} = 1.6 mA	V_{REF} − 0.5		VREF + 0.5	V
		ROMCLK, ADD1-ADD8, M0, M1	I_{OL} = 100 μA			V_{SS} + 0.5	
I_{REF}	Supply current from V_{REF} (see Note 3)				3	5	mA
I_{DD}	Supply current from V_{DD} (see Note 3)				−10	−35	mA
C_i	Input capacitance, except data bus				15		pF
C_o	Output capacitance, except data bus				15		pF
C_L	Load capacitance, data bus			25		300	pF

†Typical values are at V_{SS} = 5 V, V_{DD} = −5 V, T_A = 25°C.

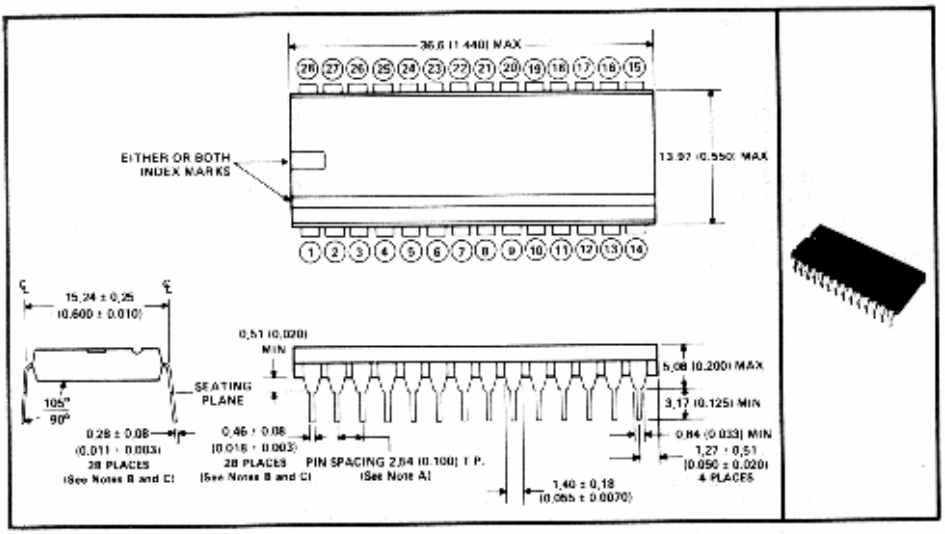
NOTE 3: Currents out of a terminal are given a negative value. I_{REF} and I_{DD} are sourced from the current into terminal V_{SS} (I_{SS}).

5.4 Static Discharge Protection

All inputs and outputs are guarded against electrostatic damage by state-of-the-art protection devices incorporated on the device.

6 Mechanical Specifications

6.1 28-Pin N-Package



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

6.2 Environmental

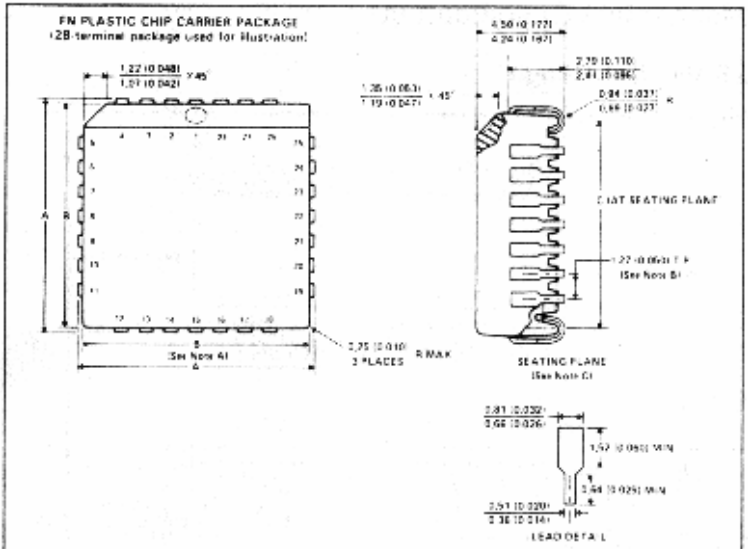
6.2.1 Temperature

The TMS5220C is characterized for operation from 0°C to 70°C and can be stored in temperatures from −40°C to 70°C.

6.2.2 Humidity

The TMS5220C is characterized to operate at 85% relative humidity at 35°C. It can be stored at 95% humidity at 55°C.

PLCC (PLASTIC LEADED CHIP CARRIER) SQUARE PACKAGE



JEDEC OUTLINE	NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
MO-047AA	20	9,78 (0.385)	10,03 (0.395)	8,89 (0.350)	9,04 (0.356)	7,87 (0.310)	8,38 (0.330)
MO-047AB	28	12,32 (0.485)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	10,41 (0.410)	10,92 (0.430)
MO-047AC	44	17,40 (0.685)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	15,49 (0.610)	16,00 (0.630)
MO-047AE	68	25,02 (0.985)	25,27 (0.995)	24,13 (0.950)	24,33 (0.958)	23,11 (0.910)	23,62 (0.930)

All dimensions and notes for the specified JEDEC outline apply.

Notes: A. Centerline of center pin each side is within 0,10 (0.004) of package centerline as determined by dimension B.

B. Location of each pin is within 0,127 (0.005) of true position with respect to center pin on each side.

C. The lead contact points are planar within 0,10 (0.004).

All linear dimensions are in millimeters and parenthetically in inches

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