CLOCK SIGNAL GENERATION CIRCUIT (CGC) FOR A DIGITAL TV SYSTEM

GENERAL DESCRIPTION

The SAA9057A is a clock signal generation circuit (CGC) which generates all clock signals required for a digital TV system utilizing the SAA90XX family of devices. The circuit operates in either the phase-locked-loop mode (PLL) or voltage controlled oscillator mode (VCO).

Features

- PLL mode generates clock signals at 2, 3 and 4 times the LFCO frequency (line frequency control)
- PLL frequency multiplier
- Skew control for temperature and load independent phase relationship between the clock signals
- Skew sense inputs
- Power failure detection circuit
- 3-state outputs
- VCO mode (bypassing the PLL)

Applications

- Digital TV system
- Digital TV with feature box and picture memories
- VCO, frequency divider and buffer

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Digital supply voltage		V_{DDD}	4.5	5.0	5.5	V
Analog supply voltage range		V_{DDA}	5.0	–	5.5	V
Digital supply current		I_{DD}	–	–	60	mA
Analog supply current		I_{DDA}	6	–	18	mA
Total power dissipation		P_{tot}	–	–	1.1	W
Operating ambient temperature range		T_{amb}	0	–	+70	°C

PACKAGE OUTLINE

20-lead DIL; plastic (SOT146).

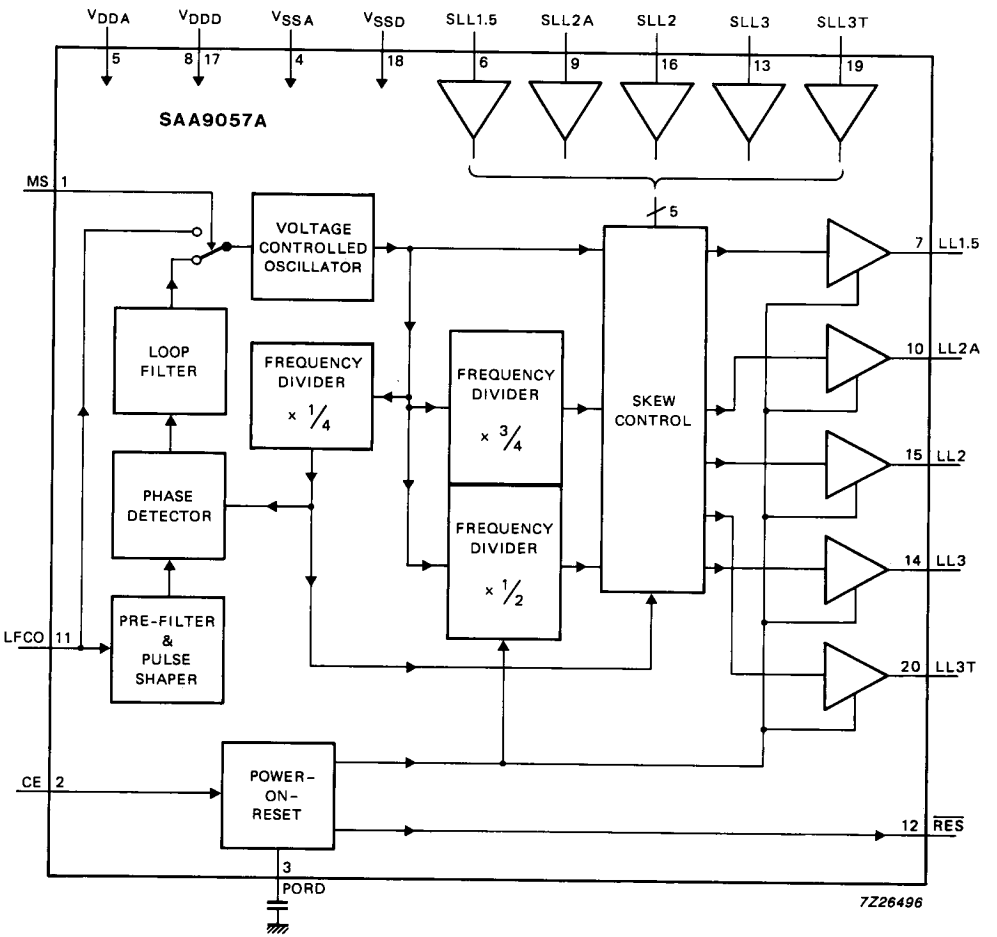

Fig.1 Block diagram.

PINNING

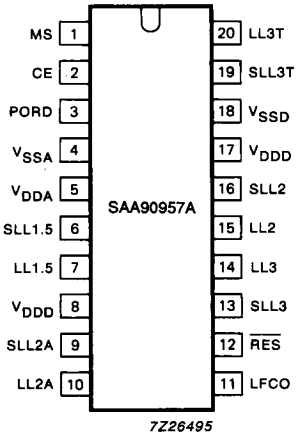

Fig.2 Pinning diagram.

DEVELOPMENT DATA

pin no.	mnemonic	description
1	MS	Mode select input. PLL mode (MS = LOW), the CGC generates clock signals using the LFCO as reference frequency. VCO mode (MS = HIGH), the PLL is disabled and the LFCO is connected to the control input of the VCO. In this mode the device operates as a VCO, frequency divider and buffer.
2	CE	Chip enable input. A HIGH level at CE enables the output buffers. A LOW level disables the buffers (HIGH impedance 3-state). The VCO operates from an internally generated frequency.
3	PORD	Power-ON reset delay. An external capacitor at this pin determines the duration of the reset state.
4	V_{SSA}	Analog ground.
5	V_{DDA}	Analog power supply.
6	SLL1.5	SLL1.5 senses if the LL1.5 output requires skew control. If no external clock driver is utilized, SLL1.5 must be connected to LL1.5. If an external buffer is utilized, SLL1.5 senses the clock signal at the buffer output.
7	LL1.5	LL1.5 is a line-locked clock signal of 4 times the LFCO input frequency. The clock signal is rectangular with a 50% duty factor.
8	V_{DDD}	Digital power supply.
9	SLL2A	SLL2A senses if the LL2A output requires skew control. If no external clock driver is utilized, SLL2A must be connected to LL2A. If an external buffer is utilized, SLL2A senses the clock signal at the buffer output.

PINNING (continued)

pin no.	mnemonic	description
10	LL2A	LL2A is a line-locked clock signal of 3 times the LFCO input frequency. The clock signal is rectangular with a 50% duty factor. This output is the reference frequency for the internal control loops and should be used as the clock signal for an analog-to-digital converter.
11	LFCO	Line frequency control input. This signal, received from the SAA9050/SAA9051, is a multiple of the line frequency (6.75 MHz). It is the reference frequency for all clock signals generated by the CGC.
12	$\overline{RES}$	RESET output (active LOW). This output indicates the reset state (HIGH or LOW). After a power-ON or power failure $\overline{RES}$ goes LOW and remains in this state for a period that is determined by the external capacitor connected to the pin PORD. If the supply voltage, slowly or rapidly, decreases below the operating range (power failure)*, $\overline{RES}$ goes LOW. After the power supply returns within the operating range and the POR delay is completed, $\overline{RES}$ goes HIGH. This signal can be used to reset the entire digital TV system. When CE is LOW, the $\overline{RES}$ output will be disabled (HIGH impedance state). C_L at $\overline{RES}$ should be < 100 nF.
13	SLL3	SLL3 senses if the LL3 output requires skew control. If no external clock driver is utilized, SLL3 must be connected to LL3. If an external buffer is utilized, SLL3 senses the clock signal at the buffer output.
14	LL3	LL3 is a line-locked clock signal of 2 times the LFCO input frequency. The clock signal is for general use and is rectangular with a 50% duty factor.
15	LL2	LL2 is a line-locked clock signal of 3 times the LFCO input frequency. The clock signal is for general use and is rectangular with a 50% duty factor.
16	SLL2	SLL2 senses if the LL2 output requires skew control. If no external clock driver is utilized, SLL2 must be connected to LL2. If an external buffer is utilized, SLL2 senses the clock signal at the buffer output.
17	V_{DDD}	Digital power supply.
18	V_{SSD}	Digital ground.
19	SLL3T	SLL3T senses if the LL3T output requires skew control. If no external clock driver is utilized, SLL3T must be connected to LL3T. If an external buffer is utilized SLL3T senses the clock signal at the buffer output.
20	LL3T	LL3T is a line-locked clock signal of 2 times the LFCO input frequency. The clock signal is rectangular with a 50% duty factor.

* See section "APPLICATION INFORMATION"; Fig. 4, reset waveform.

FUNCTIONAL DESCRIPTION

The SAA9057A generates all clock signals required for a digital TV system utilizing the SAA90XX family of devices. Optional extras (feature box etc.) can be driven via external buffers, this is advantageous for a digital TV system based on display standard conversion concepts. The frequency of the reference signal LFCO, a 6.75 MHz triangular waveform from the SAA9050/SAA9051, is multiplied by the PLL to 27 MHz (LL1.5). This clock signal is frequency divided to produce LL2 and LL3, using ratios of 3:4 and 1:2 respectively.

To achieve temperature and load independent phase relationship between the clock signals, each output is skew controlled. All clock signals are rectangular waveforms with a 50% duty factor. If no external clock buffers are used, the skew controls are connected to the clock signal outputs.
If external buffers are used, the skew controls check the clock signal at the buffer outputs. The clock signal output lines go HIGH during an internal power-ON reset period, see Fig.4.

The $\overline{\text{RES}}$ output signal indicates the reset state (HIGH or LOW). This output can be used to drive other power-ON reset circuits and provides the SAA9057A with a capability to reset a entire digital TV system. The reset time is determined by the external capacitor connected to pin PORD. It is important that a signal, within the specified ranges, is applied to LFCO before $\overline{\text{RES}}$ goes HIGH.

The SAA9057A will operate as an oscillator and frequency divider, if the phase detector and the loop filter of the PLL are disabled (MS = HIGH) and the control input for the VCO is connected to the pin LFCO.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	I_{OM} = 20 mA	V_{DDD}/V_{DDA}	−0.5	7.0	V
Input voltage		V_I	−0.5	7.0	V
Output voltage		V_O	−0.5	7.0	V
Total power dissipation		P_{tot}	−	1.1	W
Storage temperature range		T_{stg}	−65	+150	°C
Operating ambient temperature range		T_{amb}	0	+70	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal handling precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

CHARACTERISTICS

V_{DDA} = 5 V to 5.5 V; V_{DDD} = 4.5 V to 5.5 V; f_{LFCO} = 6.25 MHz to 7.25 MHz;
T_{amb} = 0 °C to +70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Digital supply voltage range		V_{DDD}	4.5	–	5.5	V
Digital supply current	note 1	I_{DDD}	–	–	60	mA
Analog supply voltage range		V_{DDA}	5.0	–	5.5	V
Analog supply current range		I_{DDA}	6	–	18	mA
Inputs						
Input leakage current	except LFCO	I_{IL}	–	–	10	μA
Input capacitance	except LFCO	C_I	–	–	5	pF
LFCO input capacitance		C_{LFCO}	–	–	10	pF
CE input voltage						
LOW		V_{IL}	0	–	0.8	V
HIGH		V_{IH}	2.4	–	V_{DDA}	V
LFCO input voltage		V_{LFCO}	0	–	V_{DDA}	V
Input signal LFCO amplitude (peak-to-peak value)		$V_{LFCO(p-p)}$	1	–	V_{DDA}	V
LFCO input frequency		f_{LFCO}	6.25	–	7.25	MHz
Outputs						
Output leakage current	note 2; CE = LOW	I_{OL}	−10	–	10	μA
$\overline{RES}$ output voltage HIGH	I_{OH} = −0.5 mA	V_{OH}	2.4	–	V_{DDD}	V
$\overline{RES}$ output voltage LOW	I_{OL} = 2 mA	V_{OL}	0	–	0.4	V
$\overline{RES}$ delay time	note 3; see Fig.4	t_d	20	–	200	ms

Notes to the characteristics

1. With 40 pF load at all outputs.
2. All outputs in 3-state.
3. Measured with a 100 nF capacitor at pin 3.

TIMING CHARACTERISTICS (see Fig.3)

T_{amb} = 0 °C to + 70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
LL1.5, LL2, LL2A, LL3, LL3T						
Output voltage LOW	I_{OL} = 2 mA	V_{OL}	0	–	0.6	V
Output voltage HIGH	I_{OH} = –0.5 mA	V_{OH}	2.6	–	V_{DDD}	V
Output frequency						
LL1.5		$f_{LL1.5}$	–	–	$4f_{LFCO}$	MHz
LL2		f_{LL2}	–	–	$3f_{LFCO}$	MHz
LL2A		f_{LL2A}	–	–	$3f_{LFCO}$	MHz
LL3		f_{LL3}	–	–	$2f_{LFCO}$	MHz
LL3T		f_{LL3T}	–	–	$2f_{LFCO}$	MHz
Composite rise time	notes 1 and 2	t_{comp}	–	–	9	ns
Duty factor	note 1					
LL1.5			40	–	60	%
LL2			40	–	60	%
LL2A			43	–	57	%
LL3			43	–	57	%
LL3T			43	–	57	%

Notes to the timing characteristics

1. f_{LFCO} = 7.0 MHz, with a 40 pF output load (typically 6.75 MHz).
2. The composite rise time is the time duration from all clocks = LOW to all clocks = HIGH (within 0.6 V to 2.6 V, includes rise time, skew and jitter).

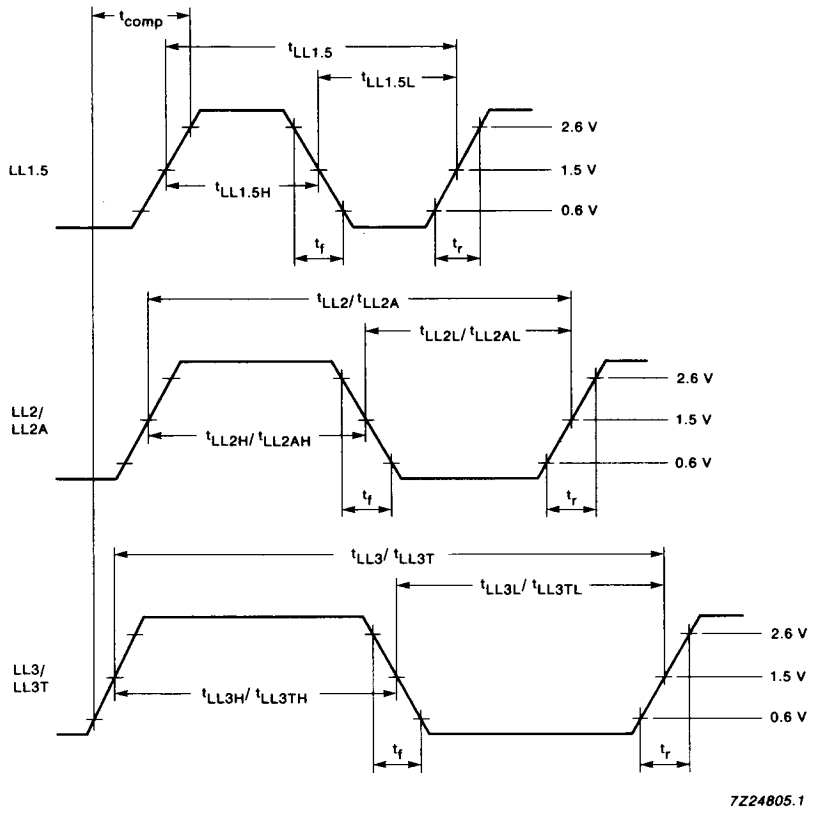

Fig.3 Timing waveform.

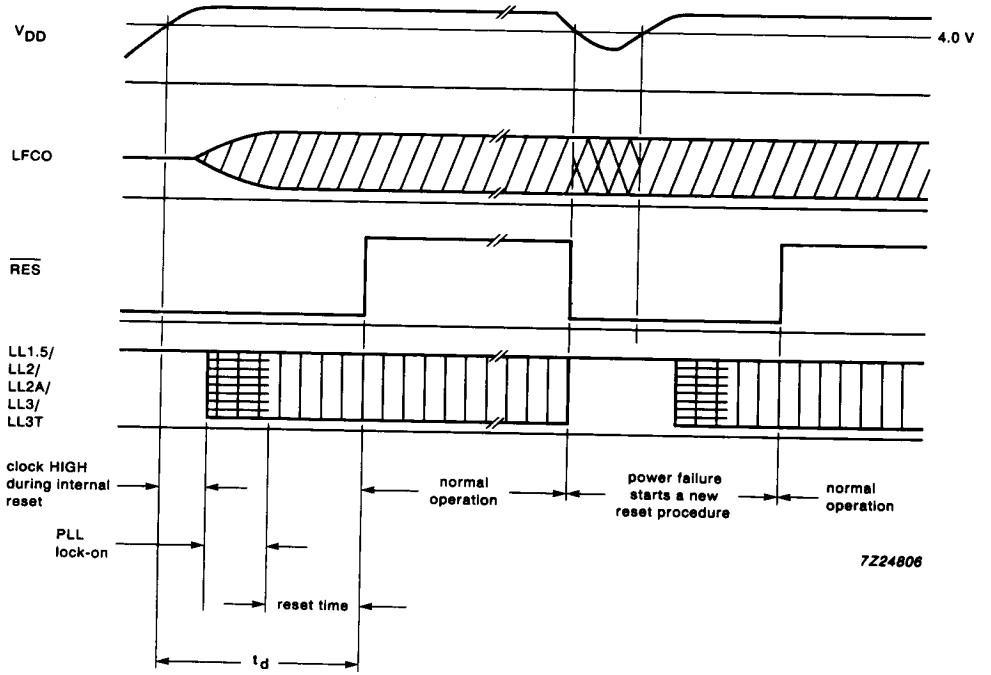

Fig.4 Reset waveform.

INTERNAL PIN CONFIGURATIONS

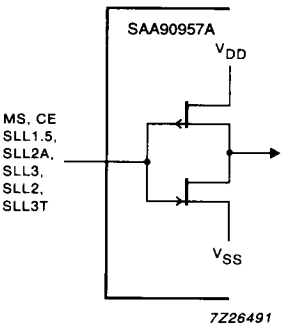

Fig.5 MS, CE, SLL2A, SLL3, SLL2 and SLL3T inputs.

DEVELOPMENT DATA

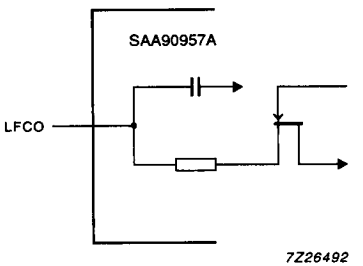

Fig.6 LFCO input.

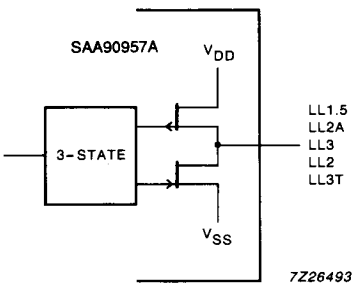

Fig.7 LL1.5, LL2A, LL2, LL3 and LL3T outputs.

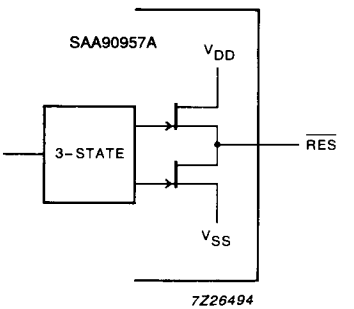

Fig.8 RES output.

APPLICATION INFORMATION

PLL

Table 1 Characteristics

parameter	symbol	typ.*	unit
Natural frequency	ω_n	6×10^5	1/s
Damping coefficient	δ	1	
Jitter		1.7	ns
Lock-in range	Δf	2 to 8	MHz
Rise and fall time (0.8 V to 2.0 V)	t_r, t_f	3	ns

Supply

To obtain optium performance from the SAA9057A, the following points should be taken into consideration:

- Supply pins must be connected to ground via a ceramic capacitor.
- Ground connections should be as inductance-free as possible. Therefore, a ground-plane layout would be preferable.
- Analog supply must be decoupled to avoid ripple over from another supply.
- LFCO signal and analog supply voltage must refer to the V_{SSA} pin. However, a separation of the digital and analog ground is not essential.

* Typical values are measured on a sample basis and are not guarenteed for the complete voltage and temperature range.

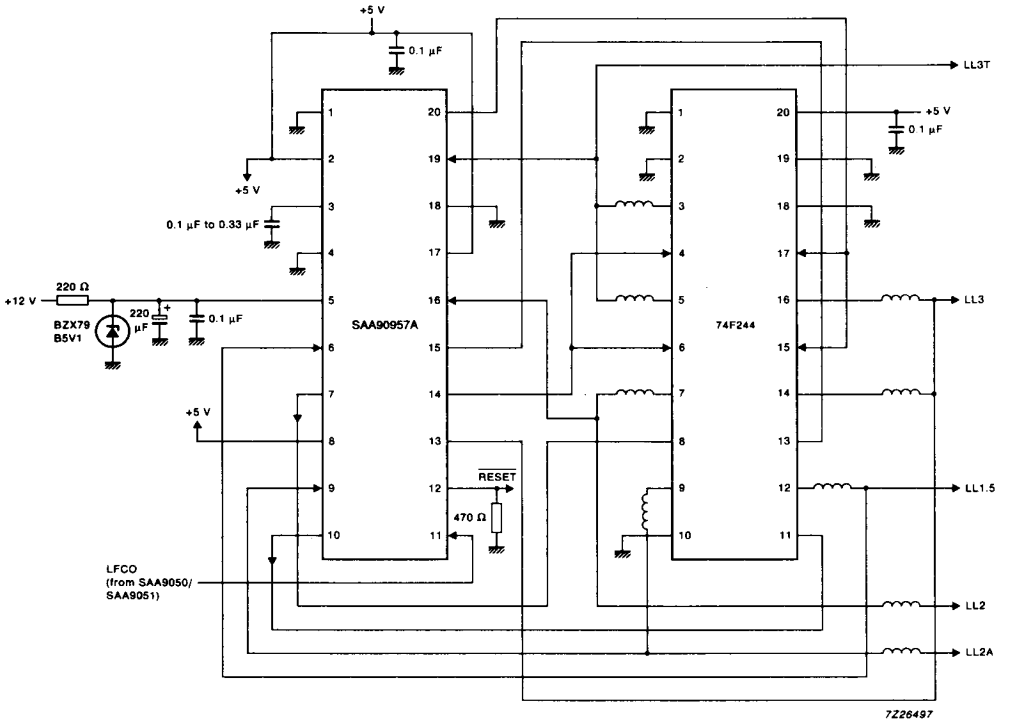

Fig.9 Application diagram; to prevent RF reflections it is recommended that the coils shown are of the square-loop ferrite core type.