MSM514256A

262,144-WORD × 4-BITS DYNAMIC RAM

GENERAL DESCRIPTION

The MSM514256A is a new generation dynamic RAM organized as 262,144 words by 4 bits. The technology used to fabricate the MSM514256A is OKI's CMOS silicon gate process technology. The device operates at a single +5V power supply. Its I/O pins are TTL compatible.

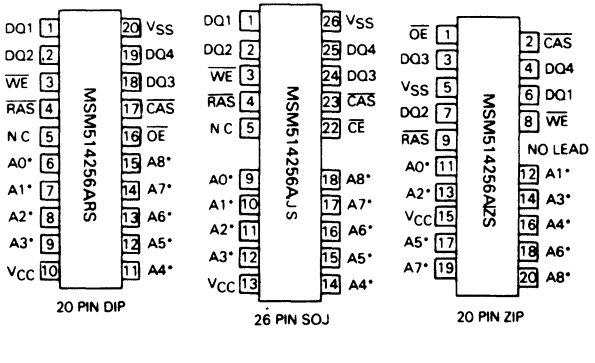
FEATURES

- Silicon gate, tripple polysilicon CMOS, 1-transistor memory cell
- Family organization
- 262,144 words by 4 bits

Family	Access Time (MAX)	Cycle Time (MIN)	Power Dissipation	
			Operating (MAX)	Standby (MAX)
MSM514256A-70	70ns	140ns	468mW	5.5mW
MSM514256A-8A/80	80ns	160ns	413mW	
MSM514256A-1A/10	100ns	190ns	358mW	

- Single +5V supply, ±10% tolerance
- Input: TTL compatible, address input, data input latch
- Output: TTL compatible, tristate, nonlatch
- Refresh: 512 cycles/8 ms
- Output impedance controllable through early write and $\overline{OE}$ operations
- Fast page mode, read/write capability
- $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh, $\overline{RAS}$ only refresh capability
- "Gated" $\overline{CAS}$
- Built-in V_{BB} generator circuit

PIN CONFIGURATION (TOP VIEW)



* Refresh Address

Pin Names	Function
A0 to A8	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
DQ1 to DQ4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)
N.C.	No Connection

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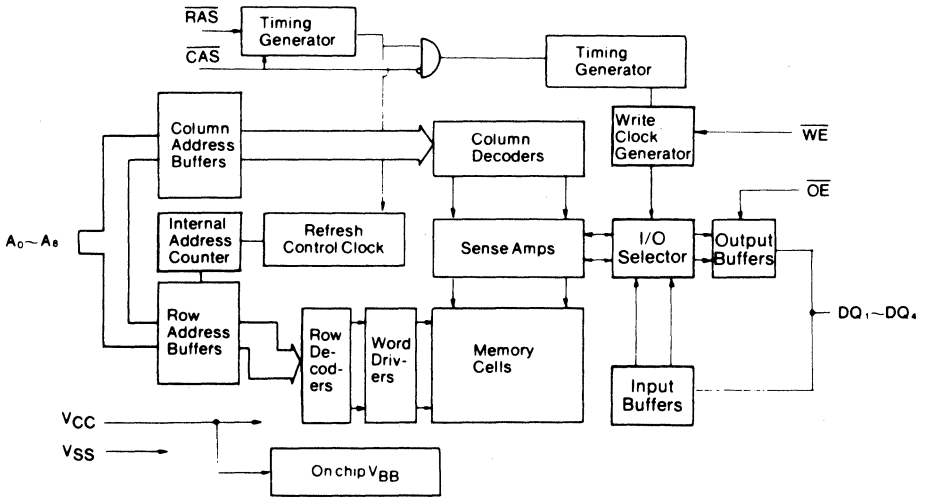
FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to V_{SS}	VT	Ta = 25°C	−1.0 to +7.0	V
Short circuit output current	Ios	Ta = 25°C	50	mA
Power dissipation	P_D	Ta = 25°C	1	W
Operating temperature	Topr	–	0 to +70	°C
Storage temperature	Tstg	–	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to +70°)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply Voltage	V_{CC}	–	4.5	5.0	5.5	V
	V_{SS}	–	0	0	0	V
Input high voltage	V_{IH}	–	2.4	–	6.5	V
Input low voltage	V_{IL}	–	−1.0	–	0.8	V

DC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = 0 to +70°C)

Parameter	Symbol	Conditions		MSM514256 A-8A		MSM514256 A-1A		MSM514256 A-70		MSM514256 A-80		MSM514256 A-10		Unit	Noto
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Output high voltage	V_{OH}	I_{OH} = −5.0mA		2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output low voltage	V_{OL}	I_{OL} = 4.2mA		0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	
Input leakage current	I_{LI}	OV≦VI≦6.5V; all oter pins not under test=OV		−10	10	−10	10	−10	10	−10	10	−10	10	μA	
Output leakage current	I_{LO}	D_{OUT}disable OV≦VO≦5.5V		−10	10	−10	10	−10	10	−10	10	−10	10	μA	
Average power supply current* (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, T_{RC}=min		−	75	−	65	−	85	−	75	−	65	mA	
Power supply current* (Standby)	I_{CC2}	$\overline{RAS}$=V_{IH} $\overline{CAS}$=V_{IH} D_{OUT}=Hz	TTL	−	2	−	2	−	2	−	2	−	2	mA	
			MOS	−	1	−	1	−	1	−	1	−	1		
Average power supply current* ($\overline{RAS}$ only represh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH} t_{RC}=min		−	75	−	65	−	85	−	75	−	65	mA	
Average power supply current* ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$		−	75	−	65	−	85	−	75	−	65	mA	
Average power supply current* (Fast page mode)	I_{CC7}	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min		−	60	−	60	−	75	−	65	−	60	mA	

***Note:** I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	TYP	MAX	Unit
Input capacitance (A0 to A8)	C_{IN1}	−	−	6	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{IN2}	−	−	7	pF
Output capacitance (DQ1 to DQ4)	$C_{I/O}$	−	−	7	pF

AC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = 0 to +70°C) Note 1, 2, 3

Parameter	Symbol	MSM514256 A-8A		MSM514256 A-1A		MSM514256 A-70		MSM514256 A-80		MSM514256 A-10		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Refresh period	t_{REP}	–	8	–	8	–	8	–	8	–	8	ms	
Random read or write cycle time	t_{RC}	160	–	190	–	140	–	160	–	190	–	ns	
Read/write cycle time	t_{RWC}	215	–	255	–	195	–	215	–	255	–	ns	
Fast page mode cycle time	t_{PC}	55	–	55	–	45	–	50	–	55	–	ns	
Fast page mode read/write cycle time	t_{PRWC}	110	–	120	–	100	–	105	–	120	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	80	–	100	–	70	–	80	–	100	ns	4.5
Access time from $\overline{CAS}$	t_{CAC}	–	25	–	30	–	20	–	20	–	25	ns	4.5
Access time fro columu address	t_{AA}	–	40	–	50	–	35	–	40	–	50	ns	4.6
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	50	–	50	–	40	–	45	–	50	ns	4
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	–	0	–	0	–	0	–	0	–	ns	4
Output buffer turn-off delay	t_{OFF}	0	20	0	20	0	20	0	20	0	20	ns	
Transition time	t_T	3	50	3	50	3	50	3	50	3	50	ns	3
$\overline{RAS}$ prechrge time	t_{RP}	70	–	80	–	60	–	70	–	80	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	70	10000	80	10000	100	10000	ns	
$\overline{RAS}$ pulse width (Fast page mode cycle only)	t_{RASP}	80	100000	100	100000	70	100000	80	100000	100	100000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25	–	30	–	20	–	20	–	25	–	ns	
$\overline{CAS}$ precharge time (Fast page mode cycle only)	t_{CP}	10	–	10	–	10	–	10	–	10	–	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10000	30	10000	20	10000	20	10000	25	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	–	100	–	70	–	80	–	100	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	55	25	70	22	50	22	60	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	20	40	20	50	17	35	17	40	20	50	ns	6
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	10	–	10	–	10	–	ns	
Row address set-up time	t_{ASR}	0	–	0	–	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	15	–	15	–	12	–	12	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	0	–	0	–	0	–	ns	
Column address hold time	t_{CAH}	15	–	20	–	15	–	15	–	20	–	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	60	–	75	–	55	–	60	–	75	–	ns	

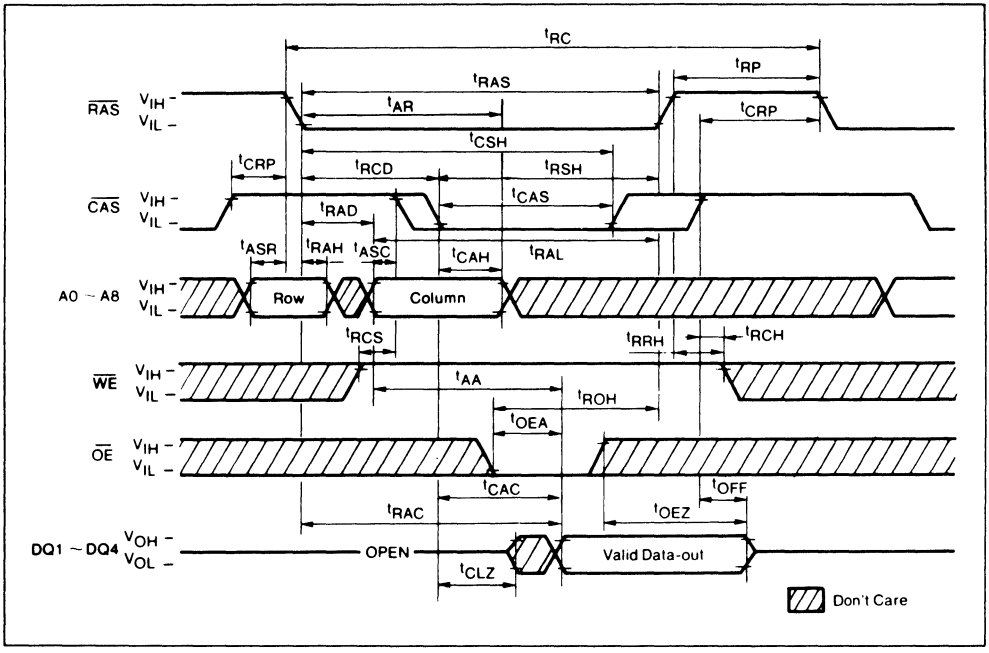
AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSM514256 A-8A		MSM514256 A-1A		MSM514256 A-70		MSM514256 A-80		MSM514256 A-10		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Column address to $\overline{RAS}$ qead time	t_{RAL}	40	–	50	–	35	–	40	–	50	–	ns	
Read command set-up time	t_{RCS}	0	–	0	–	0	–	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	0	–	0	–	0	–	ns	8
Write connand hold time from $\overline{RAS}$	t_{WCR}	60	–	75	–	55	–	60	–	75	–	ns	
Write command set-up time	t_{WCS}	0	–	0	–	0	–	0	–	0	–	ns	7
Write command hold time	t_{WCH}	15	–	20	–	15	–	15	–	20	–	ns	
Write command pulse width	t_{WP}	15	–	20	–	15	–	15	–	20	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	–	25	–	20	–	20	–	25	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	–	25	–	20	–	20	–	25	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	0	–	0	–	0	–	ns	
Data-in hold time	t_{DH}	15	–	20	–	15	–	15	–	20	–	ns	
Data-ds hold time from $\overline{RAS}$	t_{DHR}	60	–	75	–	55	–	60	–	75	–	ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	55	–	65	–	50	–	50	–	60	–	ns	7
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	110	–	135	–	100	–	110	–	135	–	ns	7
Column address to $\overline{WE}$ delay time	t_{AWD}	70	–	85	–	65	–	70	–	85	–	ns	7
Read command hold time reference to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	10	–	10	–	ns	8
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	–	10	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time (CAS before $\overline{RAS}$)	t_{CHR}	30	–	30	–	30	–	30	–	30	–	ns	
$\overline{CAS}$ active delay fron $\overline{RAS}$ preharge	t_{RPC}	10	–	10	–	10	–	10	–	10	–	ns	
$\overline{CAS}$ precharge time (Refresh counter test)	t_{CPT}	40	–	50	–	40	–	40	–	50	–	ns	
$\overline{CAS}$ precharge time	t_{CPN}	10	–	15	–	10	–	10	–	15	–	ns	
$\overline{RAS}$ hold time reference to $\overline{OE}$	t_{ROH}	20	–	20	–	20	–	20	–	20	–	ns	
Access time from $\overline{OE}$	t_{OEA}	–	20	–	25	–	20	–	20	–	25	ns	
$\overline{OE}$ delay time	t_{ODE}	20	–	25	–	20	–	20	–	25	–	ns	
$\overline{OE}$ to data output guffer turn-off delay	t_{OEZ}	0	20	0	25	0	20	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20	–	25	–	20	–	20	–	25	–	ns	

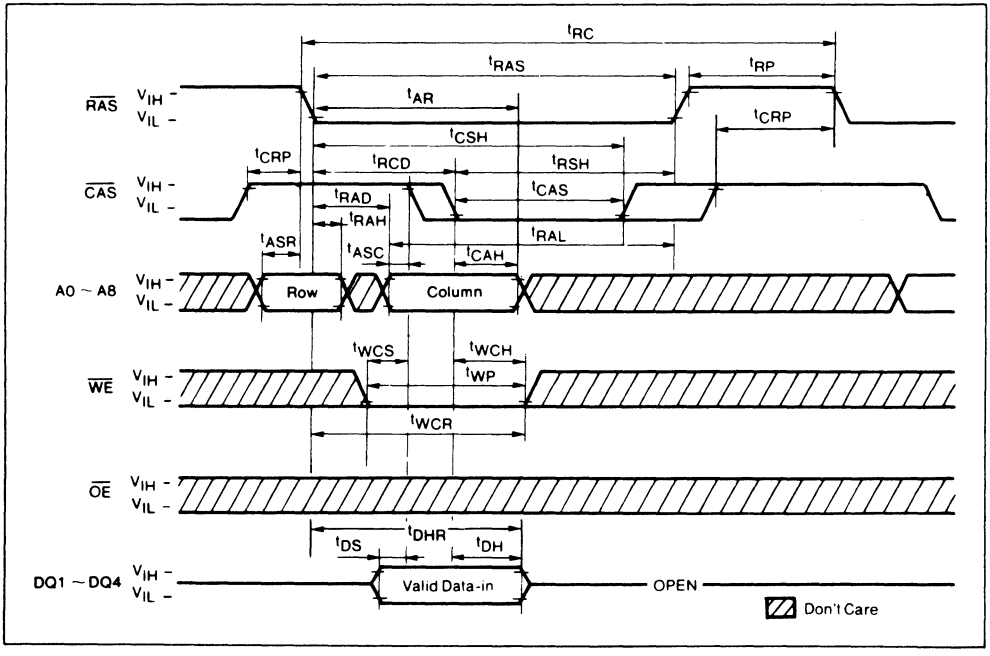
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.
2. The AC characteristics assume at $t_T = 5$ ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 2TTL + 100 pF.
5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusiveiy by t_{CAC}.
6. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
7. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min.) the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min.), $t_{RWD} \geqq t_{RWD}$ (min.) and $t_{AWD} \geqq t_{AWD}$ (min.), the cycle is read/write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

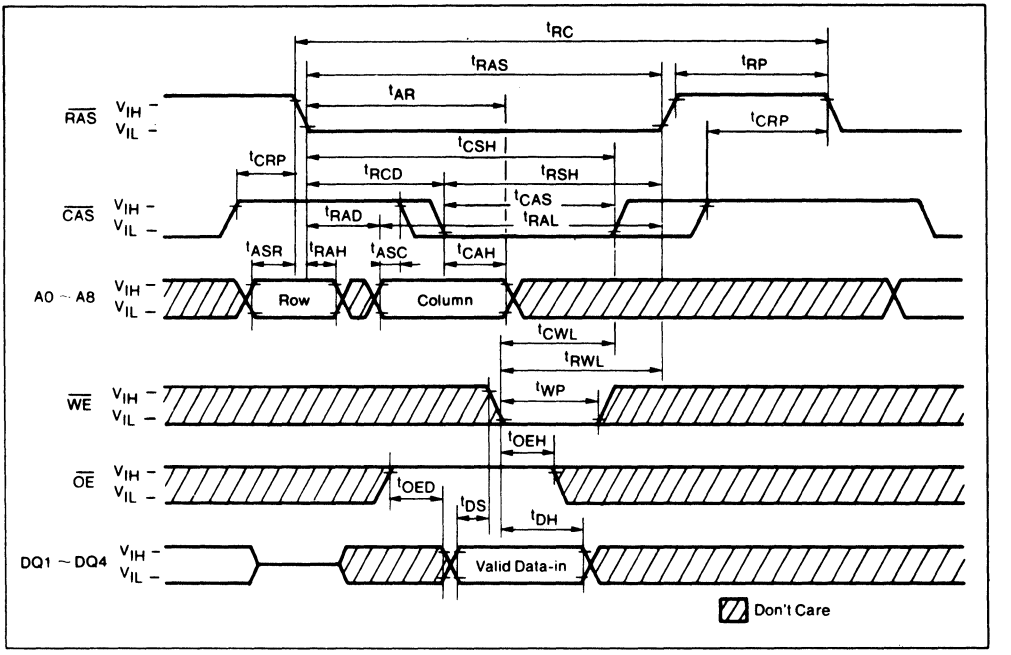
READ CYCLE



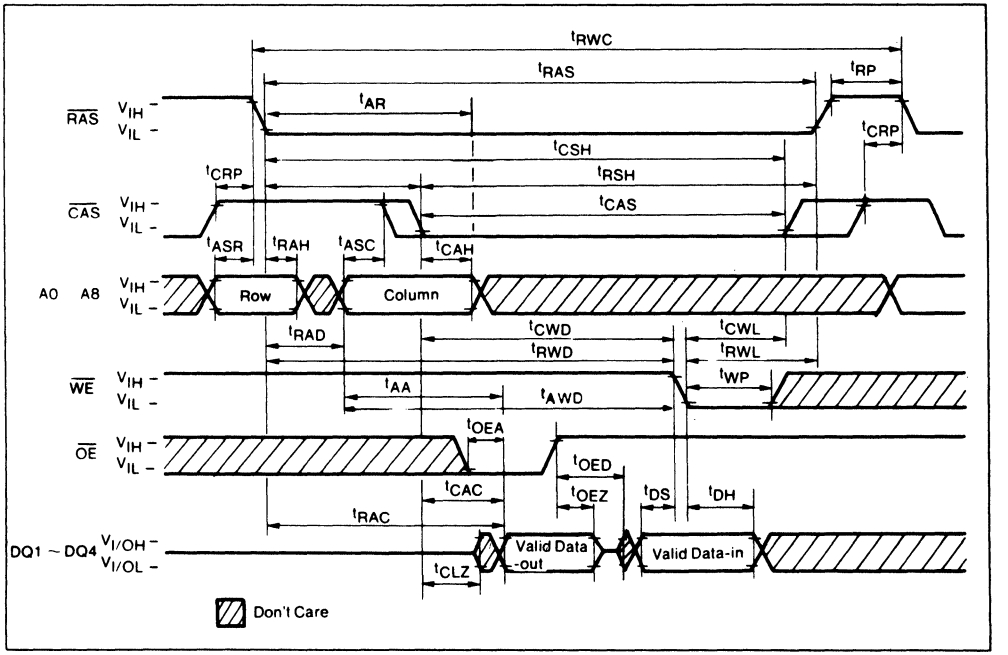
WRITE CYCLE (EARLY WRITE)



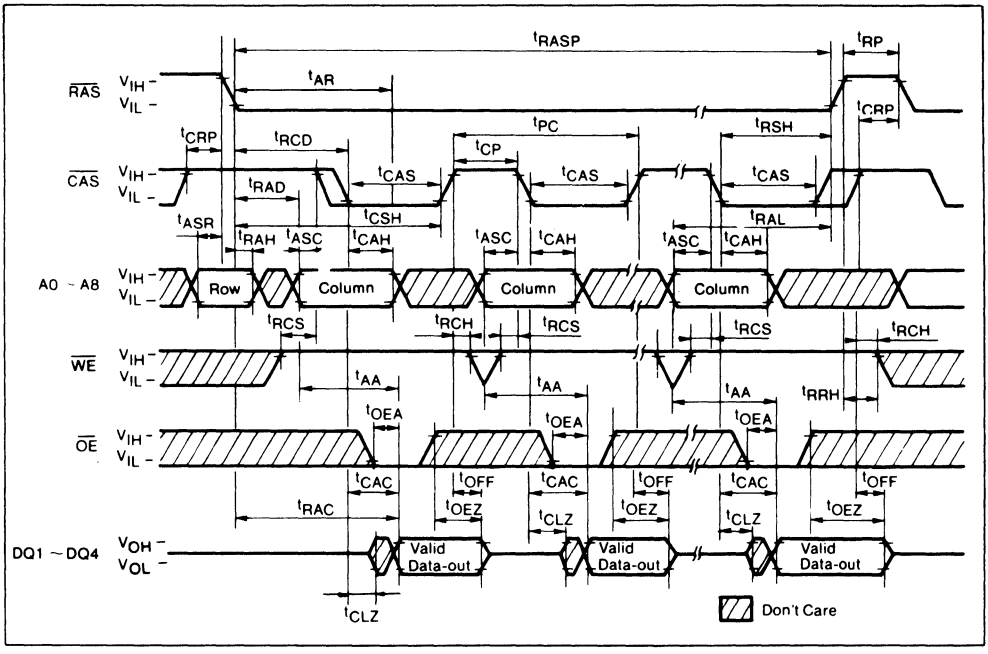
WRITE CYCLE ($\overline{OE}$ CONTROL WRITE)



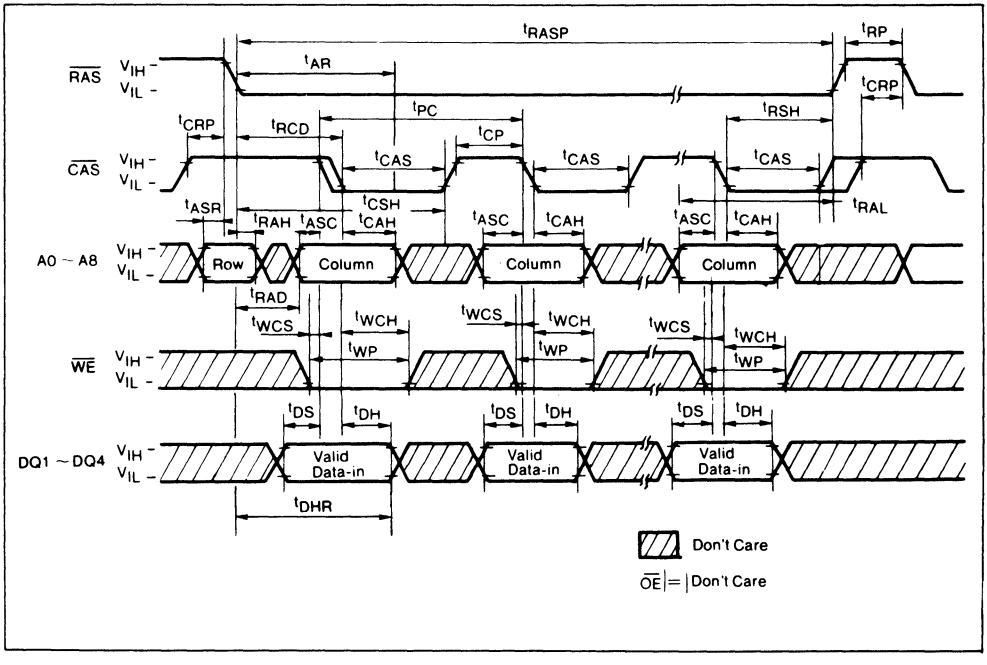
READ/WRITE CYCLE



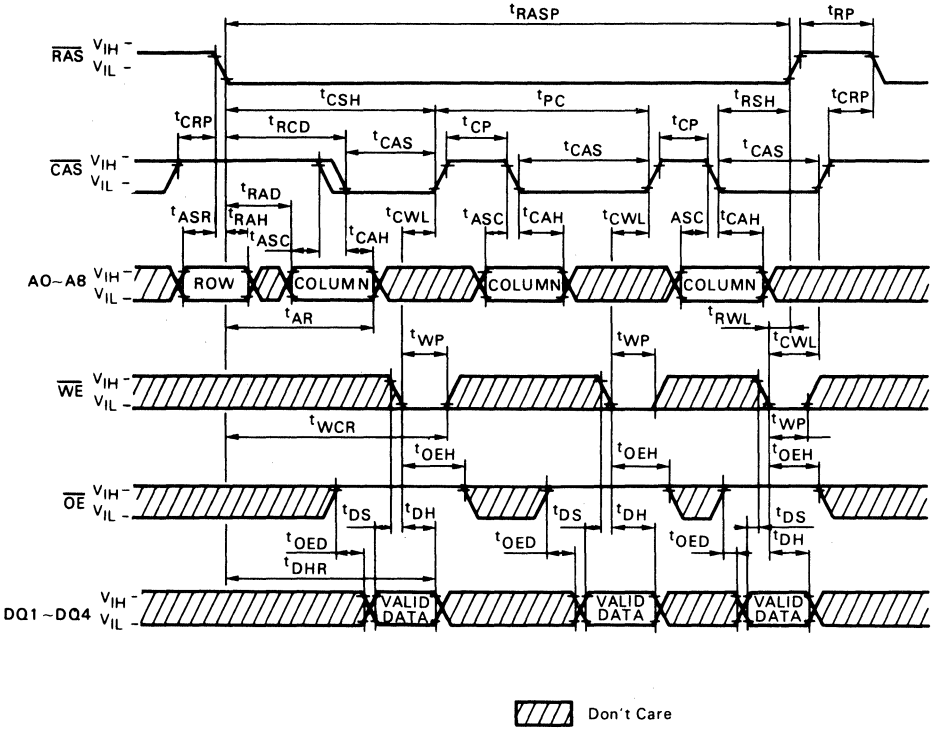
FAST PAGE MODE READ CYCLE



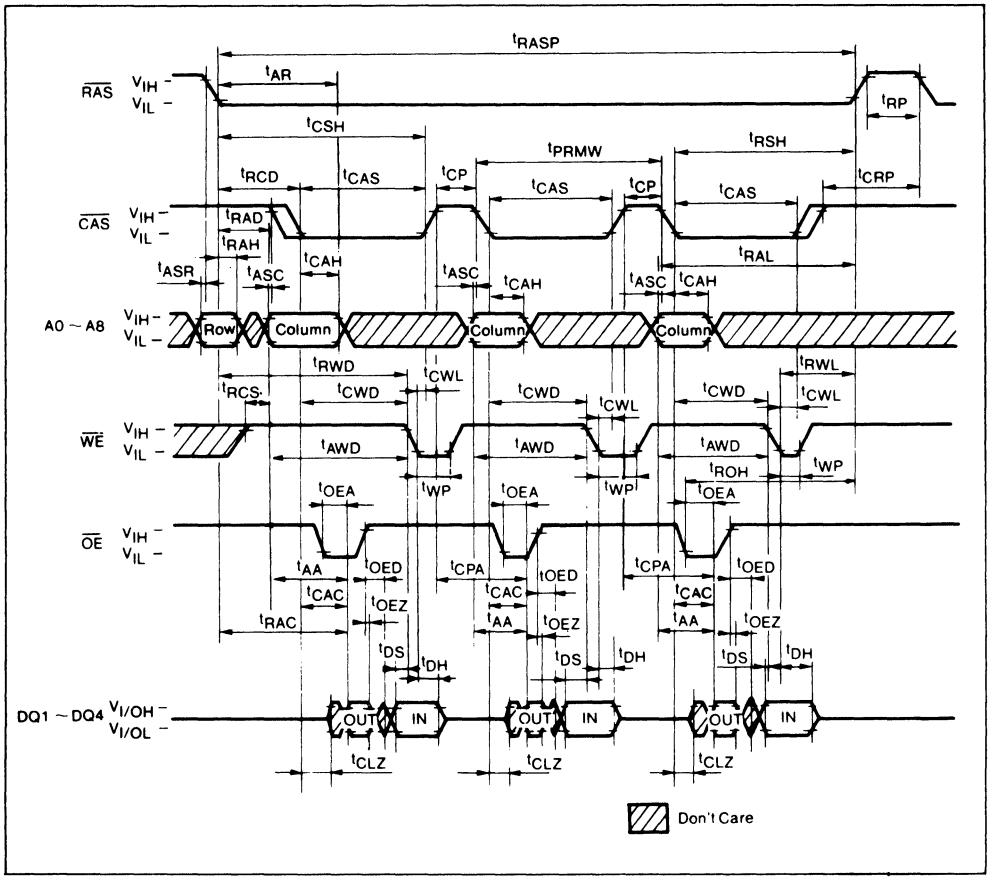
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



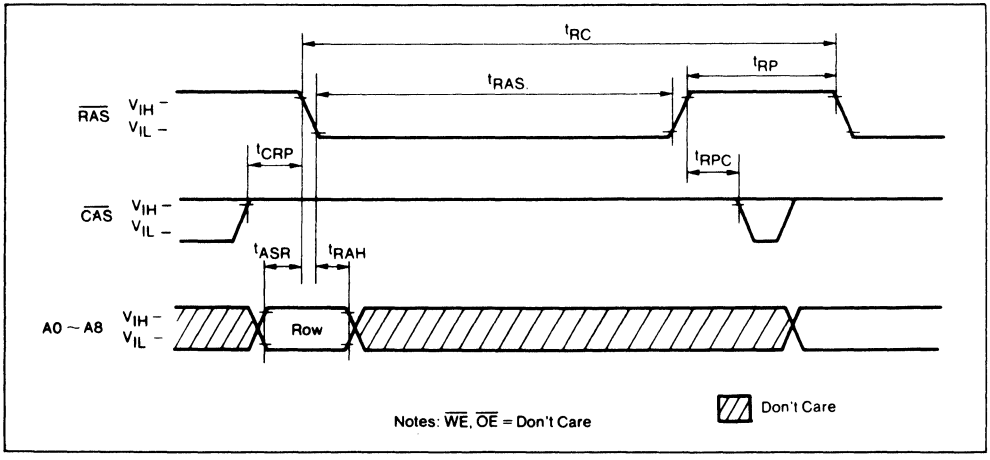
FAST PAGE MODE WRITE CYCLE($\overline{OE}$ CONTROL WRITE)



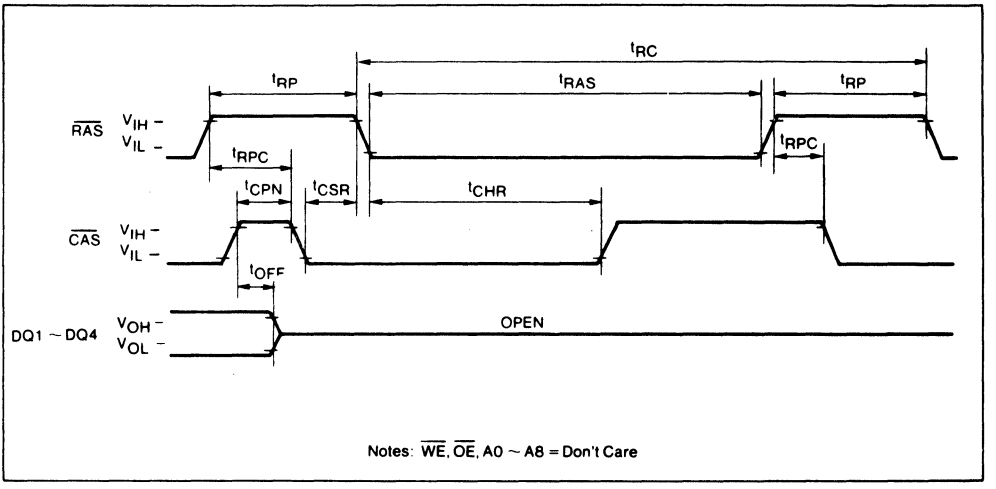
FAST PAGE MODE READ/WRITE CYCLE



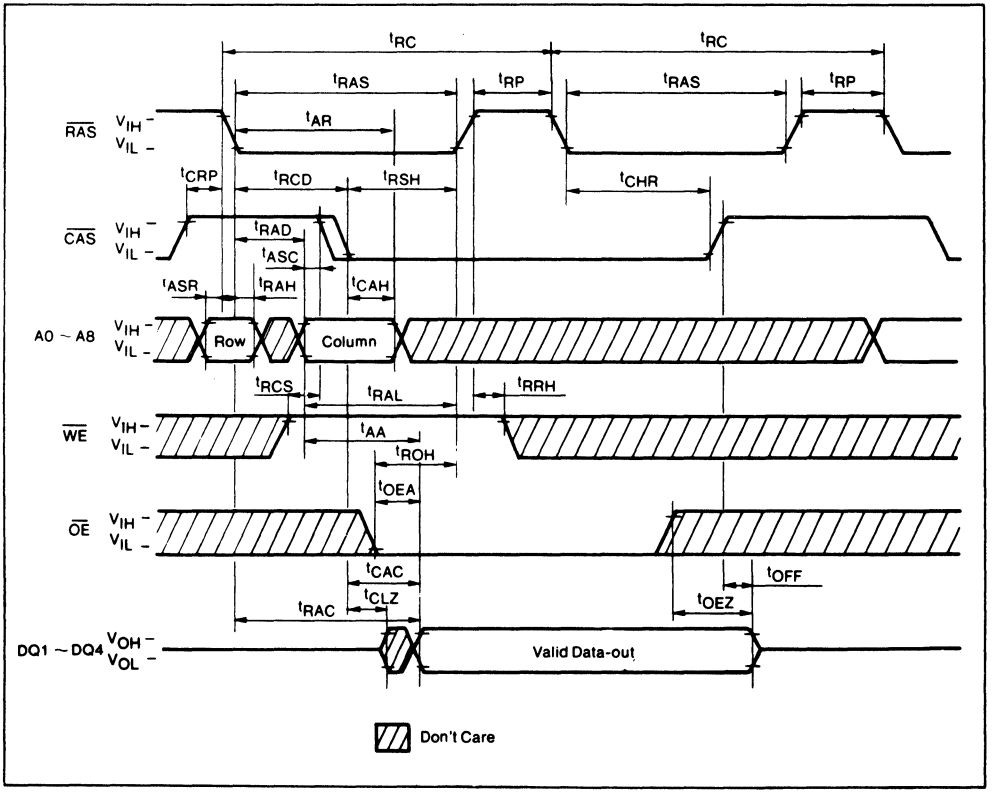
RAS ONLY REFRESH CYCLE



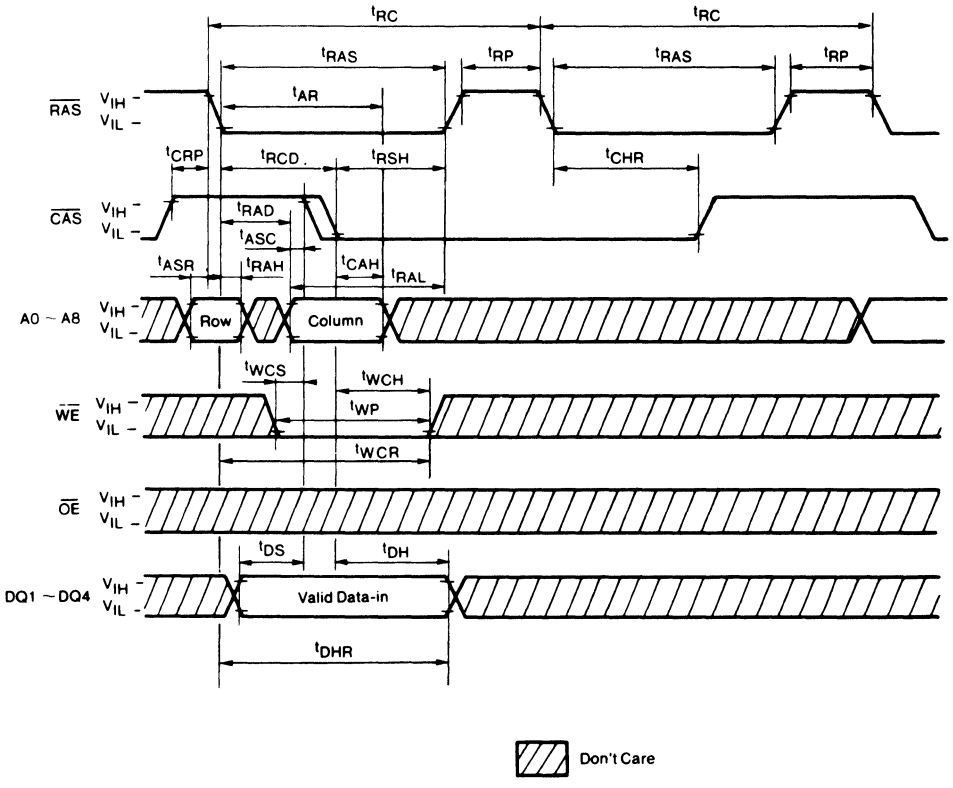
$\overline{CAS}$ BEFORE $\overline{RAS}$ AUTO REFRESH CYCLE



HIDDEN REFRESH READ CYCLE



HIDDEN REFRESH WRITE CYCLE



CAS BEFORE RAS REFRESH COUNTER TEST