# OKI semiconductor

# MSM51257AL

## 32,768-WORD x 8-BIT CMOS STATIC RAM

## GENERAL DESCRIPTION

The MSM51257ALRS/GS is a 32768-word by 8-bit CMOS RAM static RAM featuring 5V power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very to use. The MSM51257ALRS/GS is also a CMOS silicon gate device which requires very low power during standby (standby current of 100μA) when there is no chip selection.
$\overline{CS}$ and $\overline{OE}$ signals enable OR ties with the output terminals of other chips, thereby facilitating simple memory expansion and bus line control etc.

## FEATURES

- Single 5V Supply
- 0°C ~ 70°C
- Low Power Dissipation
  Standby; 0.55 mW MAX
  Operation; 385 mW MAX
- High Speed (Equal Access and Cycle Time)
  85-120 ns MAX
- Direct TTL Compatible. (Input and Output)
- 3-State Output
- 28-pin DIP PKG
- 28-pin FLAT PKG

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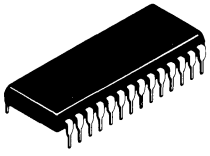
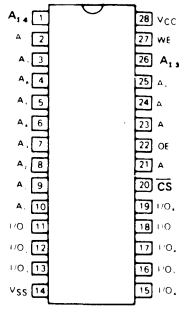
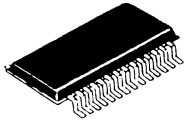


### PIN CONFIGURATION

(Top View)




$A_0 \sim A_{14}$ : Address INPUTS
$I/O_1 \sim I/O_8$ : Data Input/Output
$\overline{CS}$ : Chip Select
$\overline{WE}$ : Write Enable
$\overline{OE}$ : Output Enable
$V_{CC}$, $V_{SS}$ : Supply Voltage



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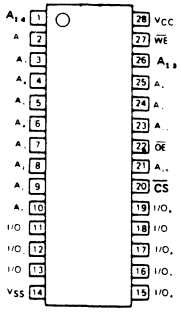
(Top View)

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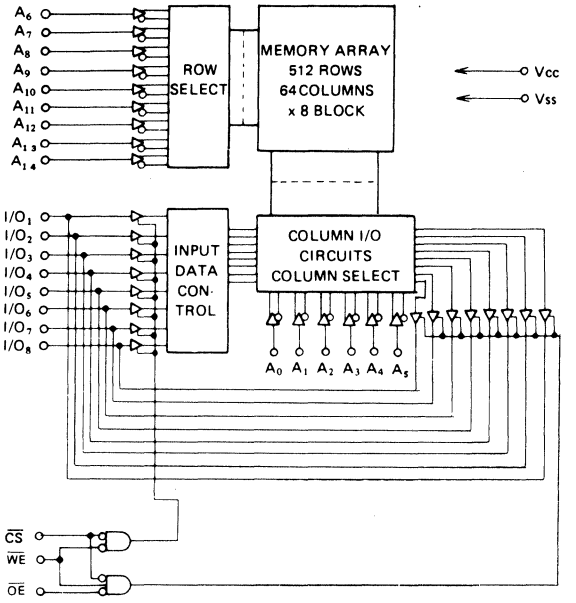
## FUNCTIONAL BLOCK DIAGRAM

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## TRUTH TABLE

| Mode | $\overline{CS}$ | $\overline{WE}$ | $\overline{OE}$ | I/O Operation |
|---|---|---|---|---|
| Standby | H | X | X | High Z |
| Read | L | H | H | High Z |
| | L | H | L | $D_{OUT}$ |
| Write | L | L | X | $D_{IN}$ |

X : H or L

## ABSOLUTE MAXIMUM RATINGS

| Rating | Symbol | Value | Unit | Conditions |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | −0.3 to 7.0 | V | Respect to GND |
| Input Voltage | $V_{IN}$ | −0.3 to $V_{CC}$ + 0.3 | V | |
| Operating Temperature | $T_{opr}$ | 0 to 70 | °C | |
| Storage Temperature | $T_{stg}$ | −55 to 150 | °C | |
| Power Dissipation | $P_D$ | 1.0 | W | Ta = 25°C |

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## RECOMMENDED OPERATING CONDITION

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5 | 5.5 | V | 5V ± 10% |
| | $V_{SS}$ | | 0 | | V | |
| Data Retention Voltage | $V_{CCH}$ | 2 | 5 | 5.5 | V | |
| Input Voltage | $V_{IH}$ | 2.2 | | $V_{CC}$ + 0.3 | V | 5V ± 10% |
| | $V_{IL}$ | −0.3 | | 0.8 | V | |
| Output Load | $C_L$ | | | 100 | pF | |
| | TTL | | | 1 | | |

## DC CHARACTERISTICS

($V_{CC}$ = 5V ±10%, $T_a$ = 0°C to +70°C)

| Paramter | Symbol | MSM51257AL | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input Leakage Current | $I_{LI}$ | −1 | | 1 | μA | $V_{IN}$ = 0 to $V_{CC}$ |
| Output Leakage Current | $I_{LO}$ | −1 | | 1 | μA | $\overline{CS}$ = $V_{IH}$ or $\overline{OE}$ = $V_{IH}$ $V_{I/O}$ = 0 to $V_{CC}$ |
| Output Voltage | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = −1 mA |
| | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 2.1 mA |
| Standby Supply Current | $I_{CCS}$ | | 2 | 100 | μA | $\overline{CS}$ ≧ $V_{CC}$ − 0.2V $V_{IN}$ = 0 to $V_{CC}$ |
| | $I_{CCS1}$ | | | 3 | mA | $\overline{CS}$ = $V_{IH}$ |
| Operating Supply Current | $I_{CCA}$ | | | ① | mA | MIN CYCLE, $I_{OUT}$ = 0 mA |

① 51257AL-85 80 mA 51257AL-10/12 70 mA

## AC CHARACTERISTICS

### Test Condition

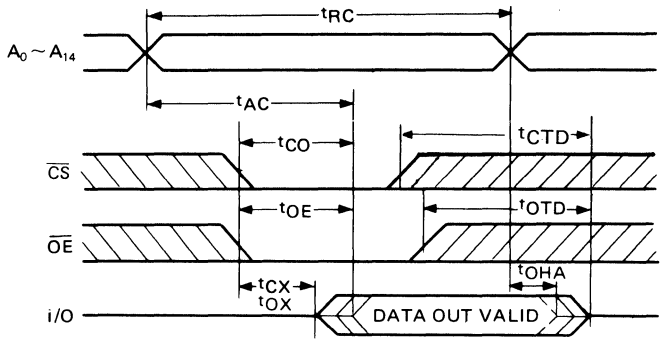
| Parameter | Conditions |
|---|---|
| Input Pulse Level | $V_{IH}$ = 2.4V, $V_{IL}$ = 0.6V |
| Input Rise and Fall Times | 5ns |
| Input and Output Timing Reference Level | 1.5V |
| Output Load | $C_L$=100 pF, 1 TTL Gate |

## READ CYCLE

($V_{CC}$ = 5V ± 10%, $T_a$ = 0°C to 70°C)

| Parameter | Symbol | MSM51257AL-85 | | MSM51257AL-10 | | MSM51257AL-12 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Read Cycle Time | $t_{RC}$ | 85 | | 100 | | 120 | | ns |
| Address Access Time | $t_{AC}$ | | 85 | | 100 | | 120 | ns |
| Chip Enable Access Time | $t_{CO}$ | | 85 | | 100 | | 120 | ns |
| Output Enable to Output Valid | $t_{OE}$ | | 45 | | 50 | | 60 | ns |
| Chip Selection to Output Active | $t_{CX}$ | 10 | | 10 | | 10 | | ns |
| Output Hold Time From Address Change | $t_{OHA}$ | 5 | | 10 | | 10 | | ns |
| Output 3-state from Output Disable | $t_{OTD}$ | | 30 | | 35 | | 35 | ns |
| Output 3-state from Chip Deselection | $t_{CTD}$ | | 30 | | 35 | | 35 | ns |
| Output Enable to Output Active | $t_{OX}$ | 5 | | 5 | | 5 | | ns |

## READ CYCLE




**Notes:** 1. A Read occurs during the overlap of a low $\overline{CS}$, a low $\overline{OE}$ and a high $\overline{WE}$.
2. $t_{CTD}$ and $t_{OTD}$ are specified by the time when DATA OUT is floating.

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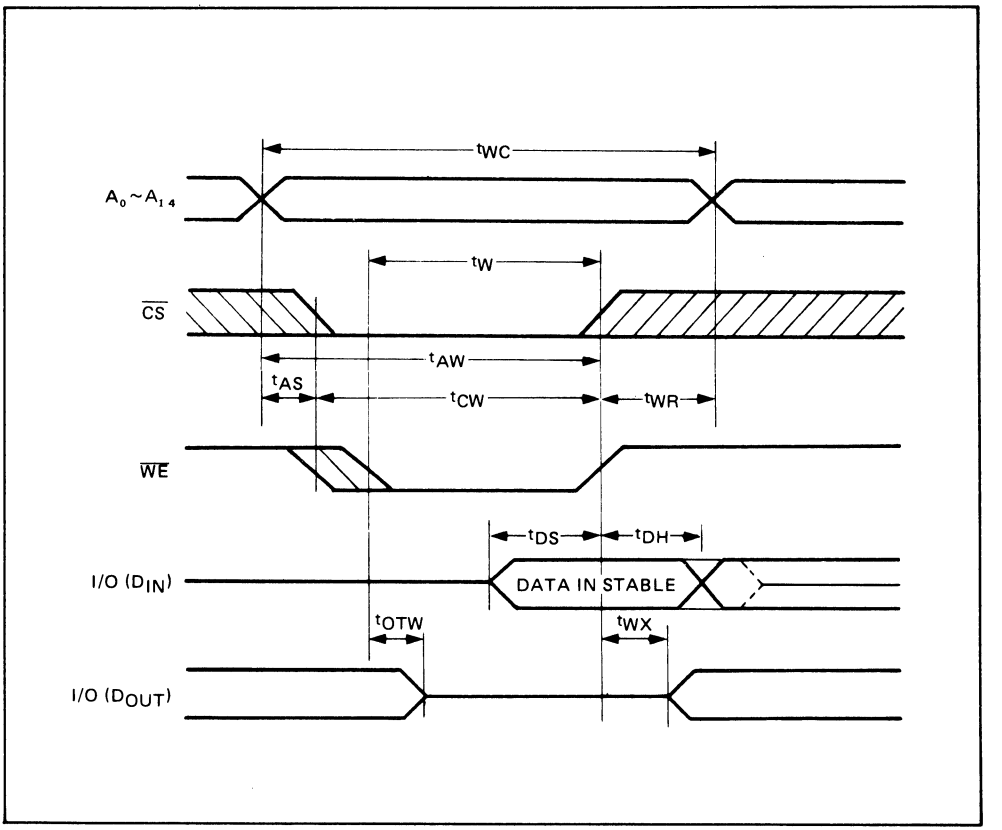
## WRITE CYCLE

($V_{CC}$ = 5V ± 10%, $T_a$ = 0°C to +70°C)

| Item | Symbol | MSM51257AL-85 | | MSM51257AL-10 | | MSM51257AL-12 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Write Cycle Time | $t_{WC}$ | 85 | | 100 | | 120 | | ns |
| Address to Write Setup Time | $t_{AS}$ | 0 | | 0 | | 0 | | ns |
| Write Time | $t_W$ | 70 | | 75 | | 90 | | ns |
| Write Recovery Time | $t_{WR}$ | 5 | | 10 | | 10 | | ns |
| Data Setup Time | $t_{DS}$ | 40 | | 40 | | 50 | | ns |
| Data Hold from Write Time | $t_{DH}$ | 0 | | 0 | | 0 | | ns |
| Output 3-State from Write | $t_{OTW}$ | 0 | 30 | 0 | 35 | 0 | 35 | ns |
| Chip Selection to End of Write | $t_{CW}$ | 75 | | 90 | | 100 | | ns |
| Address Valid to End of Write | $t_{AW}$ | 75 | | 90 | | 100 | | ns |
| Output Active from End of Write | $t_{WX}$ | 5 | | 5 | | 5 | | ns |

**Notes:** 1. A Write Cycle occurs during the overlap of a low $\overline{CS}$, and a low $\overline{WE}$.
2. $\overline{OE}$ may be both high and low in a Write Cycle.
3. $t_{AS}$ is specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs last.
4. $t_W$ is an overlap time of a low $\overline{CS}$, and a low $\overline{WE}$.
5. $t_{WR}$, $t_{DS}$ and $t_{DH}$ are specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs first.
6. $t_{OTW}$ is specified by the time when DATA OUT is floating, not defined by output level.
7. When I/O pins are Data output mode, don't force inverse signal to those pins.

## WRITE CYCLE



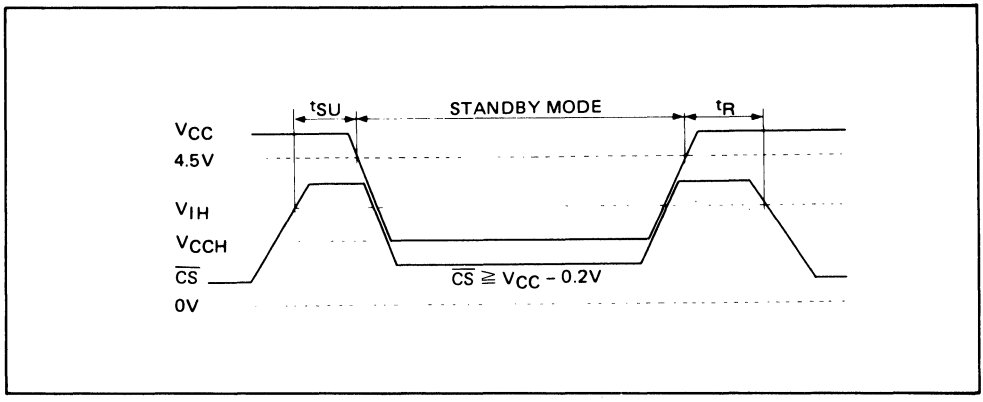

## LOW $V_{CC}$ DATA RETENTION CHARACTERISTICS

($T_a$ = 0°C to +70°C, unless otherwise noted)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| $V_{CC}$ for Data Retention | $V_{CCH}$ | 2 | | 5.5 | V | $\overline{CS} \geqq V_{CC} - 0.2V$ |
| Data Retention Current | $I_{CCH}$ | | 1 | 50 | μA | $V_{CC}$ = 3V, $\overline{CS} \geqq V_{CC} - 0.2V$ |
| CS to Data Retention Time | $t_{SU}$ | 0 | | | ns | |
| Operation Recovery Time | $t_R$ | *$t_{RC}$ | | | ns | |

* $t_{RC}$ = Read Cycle Time

## $\overline{CS}$ CONTROL




## CAPACITANCE

(Ta = 25°C, f = 1MHz)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Input/Output Capacitance | $C_{I/O}$ | | | 10 | pF |
| Input Capacitance | $C_{IN}$ | | | 10 | pF |

**Note:** This parameter is periodically sampled and not 100% tested.