MSM16811

1,024 BIT SERIAL E²PROM

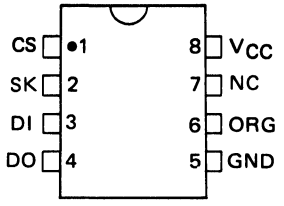
FEATURES:

- CMOS Floating Gate Technology
- Single +5-volt supply
- Eight pin plastic package
- 64 x 16 or 128 x 8 user selectable serial memory
- Compatible with NS9346
- Self timed programming cycle with Auto erase
- Word and chip erasable
- Operating Range 0°C to 70°C
- 10,000 erase/write cylces
- 10 year data retention

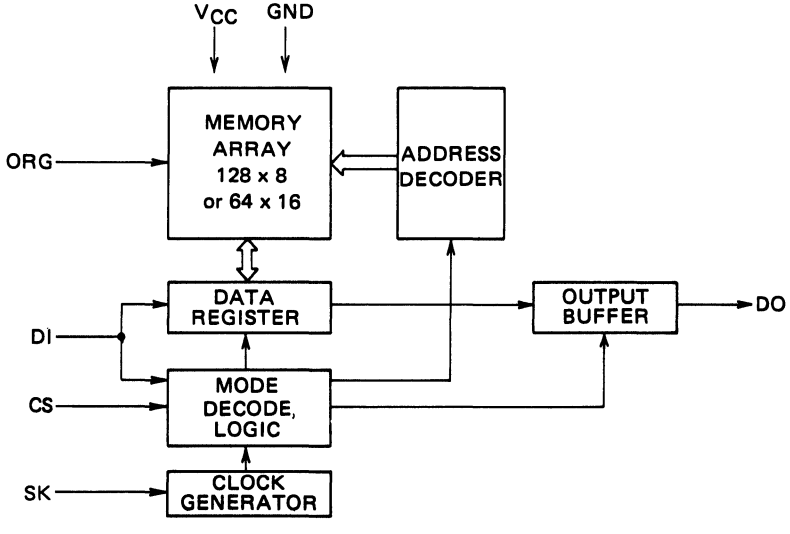
PIN CONFIGURATION

8 Pin Dual-In-Line
8 Pin S.O. Package

TOP VIEW



BLOCK DIAGRAM



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PIN FUNCTIONS			
CS	Chip Select	ORG	Memory Array Organization Selection Input. When the ORG pin is connected to +5 V the 64 x 16 organization is selected. When it is connected to ground the 128 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pull-up device will select the 64 x 16 organization.
SK	Clock Input		
DI	Serial Data Input		
DO	Serial Data Output		
V_{CC}	+5 V Power Supply		
NC	Non Connection		
GND	Ground		

			INSTRUCTION SET				
			Address		Data		
Instruction	Start Bit	Opcode	128 x 8	64 x 16	128 x 8	64 x 16	Comments
READ	1	1 0	A_6–A_0	A_5–A_0			Read Address A_N–A_0
ERASE	1	1 1	A_6–A_0	A_5–A_0			ERASE Address A_N–A_0
WRITE	1	0 1	A_6–A_0	A_5–A_0	D_7–D_0	D_{15}–D_0	WRITE Address A_N–A_0
EWEN	1	0 0	11XXXXX	11XXXX			Program Enable
EWDS	1	0 0	00XXXXX	00XXXX			Program Disable
ERAL	1	0 0	10XXXXX	10XXXX			Erase All Addresses
WRAL	1	0 0	01XXXXX	01XXXX	D_7–D_0	D_{15}–D_0	Program All Addresses

Power-On Data Protection Circuitry: During power-up all modes of operation are inhibited until V_{CC} has reached a level of between 2.8 and 3.5 volts. During power-down the source data protection circuitry acts to inhibit all modes when V_{CC} has fallen below the voltage range of 2.8 to 3.5 volts.

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Supply Voltage	V_{CC}	Ta = 25 °C	−0.3 ~ 7	V
Input Voltage	V_I		−0.3 ~ V_{CC} + 0.3	V
Output Voltage	V_O		−0.3 ~ V_{CC} + 0.3	V
Storage Temperature	T_{STG}		−55 ~ + 150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as recommended. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Parameter	Symbol	Range	Unit
Supply Voltage	V_{CC}	5 ± 10 %	V
Temperature Range	Ta	0 ~ 70	°C
Data Hold Temperature	Ta	0 ~ 70	°C

DC CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, Ta = −0 ~ 70°C, unless otherwise specified.)

Parameter	Symbol	Condition	MIN	MAX	Unit
Supply Voltage	V_{CC}		4.5	5.5	V
Power Supply Current	I_{CC1}	V_{CC} = 5.5 V CS = 1		3	mA
	I_{CC2}	V_{CC} = 5.5 V CS = 0 DI = 0 or V_{CC}		100	μA
"L" Input Voltage	V_{IL}		−0.1	0.8	V
"H" Input Voltage	V_{IH}		2.0	V_{CC} + 1	V
"L" Output Voltage	V_{OL}	TTL I_{OL} = 2.1 mA		0.4	V
		CMOS I_{OL} = 100 μA		0.1	V
"H" Output Voltage	V_{OH}	TTL I_{OH} = −400 μA	2.4		V
		CMOS I_{OH} = −100 μA	V_{CC}−0.5		V
Input Leakage Current	I_{LI}	V_{in} = 5.5 V		10	μA
Output Leakage Current	I_{LO}	V_{out} = 5.5 V CS = 0		10	μA

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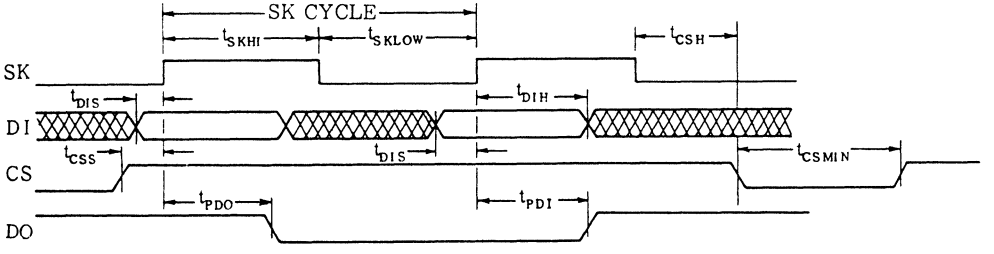
AC CHARACTERISTICS

Parameter	Description	Test Condition	Min	Typ	Max	Units
t_{CSS}	CS Setup Time		0.2			μs
t_{CSH}	CS Hold Time		0			μs
t_{DIS}	DI Setup Time		0.4			μs
t_{DIH}	DI Hold Time		0.4			μs
t_{PD1}	Output Delay to 1	CL = 100pF V_{OL} = 0.8V, V_{OH} = 2.0 V_{IL} = 0.45V, V_{IH} = 2.4			2	μs
t_{PD0}	Output Delay to 0				2	μs
t_{HZ}	Output Delay to HiZ				0.4	μs
t_{EW}	Erase / Write Pulse Width				10	ms
t_{CSMIN}	Min CS Low Time		1			μs
t_{SKHI}	Min SK High Time		1			μs
t_{SKLOW}	Min SK Low Time		1			μs
t_{SV}	Output Delay to Status Valid	C_L = 100 pF			1	μs
SK_{MAX}	Maximum Frequency		0		250	kHz



Synchronous Timings

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DEVICE OPERATION

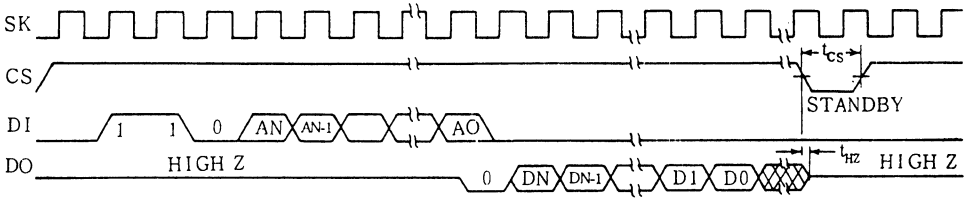
The MSM 16811 has 7 instructions that allow it to read, erase, or write. Each instruction consists of a start bit logical '1', an opcode field (2 bits or 4 bits) and an address field (6 or 7 bits).

The DO pin is a multiplexed pin. It is used as Data Out during the Read mode. It can also be used as a Ready Busy status indicator in programming mode. In all the other modes DO is tri-stated.

During power-up, all modes of operation are disabled and the device comes up in a program disabled state. An EWEN instruction has to be issued before starting to program.

At power-down, when V_{CC} falls below a level of approximately 3V, the data protection circuitry inhibits all modes of operation and an EWDS instruction is executed internally.

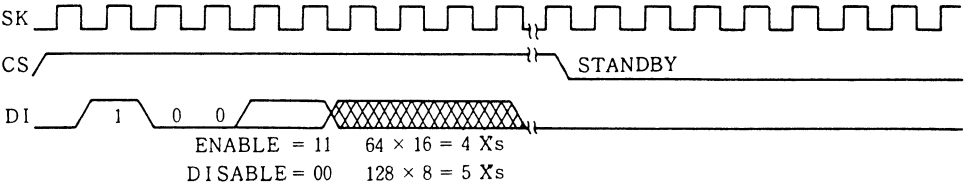
READ MODE



Organization	A_N	D_N
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

The READ instruction reads the contents of the addressed register. It outputs data serially on the DO pin. After the instruction is decoded, a dummy bit (logical "0") precedes the output data string.

ERASE/WRITE ENABLE AND DISABLE



After power-up and before starting any programming instruction the EWEN instruction has to be issued. Once it has been issued, it will remain active until an EWDS instruction takes place. The EWDS instruction is provided to avoid any accidental programming of the part. The READ instruction is independent from the EWEN and EWDS instructions.

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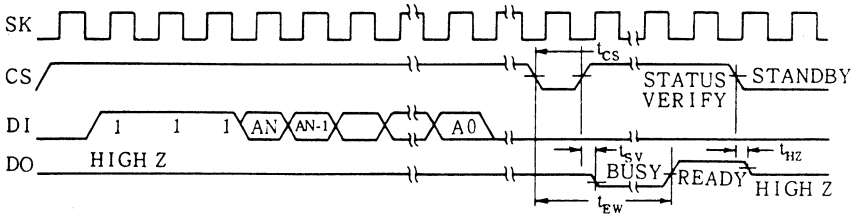
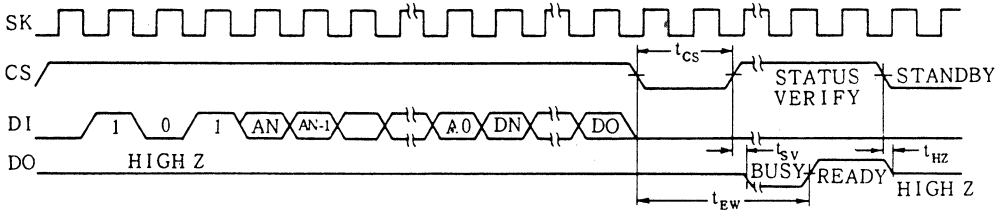
ERASE MODE



After an ERASE instruction has been shifted in. CS is dropped low. This will set the beginning of the self timed erase sequence. If CS is then brought high (after observing t_{CS} spec) the DO pin will act as a status indicator. It will remain low as long as the chip is programming. It will go high after all the bits of the addressed register have been set to a logical '1'.

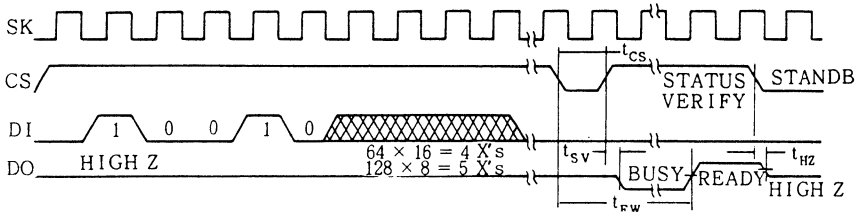
WRITE MODE



After a WRITE instruction has been shifted in with the corresponding 8 bits or 16 bits of data, CS is dropped low. This will set the beginning of the self timed programming sequence. If CS is brought high during the programming time (after observing the t_{CS} specification), the DO pin will act as a status indicator — it will remain low as long as the chip is programming. It will go high after all the bits of the addressed register have been set to their proper value. With the MSM16811 it is NOT neccessary to erase a memory location before the WRITE instruction.

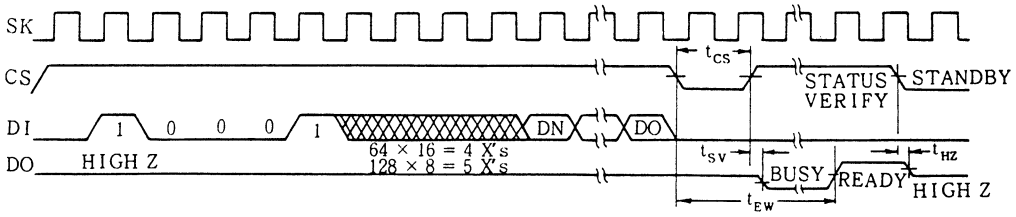
Configuration	A_N	D_N
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

ERASE ALL



This instruction is provided to erase the whole chip. Besides its different opcode, the ERAL instruction is identical to the ERASE instruction.

WRITE ALL



This instruction is provided to write simultaneously all the registers. All the registers must be erased before doing a WRAL operation. Besided its different opcode, the WRAL instruction is identical to the WRITE instruction.

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