TROPIC™—A Front End Description

National Semiconductor
Application Note 850
Joel Martinez

OVERVIEW

This application note describes the DP8025 Token-Ring Protocol Interface Controller (TROPIC) Front End Macro (FEM). The FEM is one internal block within TROPIC. TROPIC's analog FEM is transformer coupled directly to the Token-Ring system. The analog circuitry converts distorted receive signals into square wave signals used by TROPIC's digital circuitry. The receiver includes an external equalization circuit to make the conversion process more reliable. The driver circuit provides sufficient drive capability to transmit signals across the ring with acceptable distortion at the receiver end. The FEM does not decode or encode signals. The Protocol Handler (PH) performs the encoding and decoding function.

This application note supplements the DP8025-TROPIC datasheet. Application Note 816, "Layout Guidelines for a Token Ring Adapter Using the DP8025" illustrates the recommended layout for the FEM.

INTRODUCTION

The TROPIC Front End Macro (FEM) combined with external equalization circuitry and components provides the modulation/demodulation function by which digital data is propagated over the analog transmission medium. Specifications and requirements of the FEM operation at 4 Mbps and 16 Mbps are included in the discussions. Performance objectives are given for the FEM and the transmission system operating at both speeds. For brevity in tables and figures, braces-{ } denote items pertaining only to 16 Mbps operation. Parameters or combinations of parameters required to meet these objectives are defined and specified.

Unless otherwise specified, the functional definitions and tests are described assuming the external components given in Appendix A. The connection of these components is shown in *Figures 6a* and *6b* in Appendix A. *Figure 6c* in Appendix A lists the component values and tolerances.

DIFFERENTIAL MANCHESTER CODE

Differential Manchester coding used in Token Ring has four symbols; binary 1, binary 0, non-data J and K. The symbols used in the Token Ring physical layer are shown in Table I. Binary ones and zeroes have mid-bit transitions which convey inherent timing information on the channel. Binary "zeroes" transition at the beginning. Binary "ones" do not transition at the beginning. Non-data J and K do not have mid-bit transitions. K transitions at the start of the bit boundary (also called a "negative code violation"), while J does not (also called a "positive code violation").

The symbols are transmitted through the medium in the form of differential Manchester encoding that is characterized by two signal elements per symbol—the leading and trailing element. The leading element polarity is dependent on the trailing element of the previously transmitted symbol. The polarity of three elements must be known to decode a single symbol; the trailing element of the previous symbol, and the leading and trailing elements of the current symbol.

TABLE I. Token Ring Differential Manchester Code Symbols

Symbol	Description	Transition @ beginning	Transition @ mid-bit
0	binary zero	yes	yes
1	binary one	no	yes
J	non-data "J"	no	no
K	non-data "K"	yes	no

An example of differential Manchester coding is illustrated in *Figure 1a*. Let's decode a few of the symbols. A change in polarity (transition) between the trailing element and leading element at the beginning of the bit boundary, ***a***, narrows the possibilities to a binary zero or a non-data K, as shown in Table I column "Transition @ beginning". A transition at mid-bit, ***b***, leaves us to conclude the symbol is a binary zero. Let's try another, a lack of transition at bit boundary ***c*** narrows the possibilities to a binary one and non-data J. A transition at mid-bit, ***d***, leaves us to conclude the symbol is a binary one.

J and K appear within the Starting Delimiter and Ending Delimiter fields as shown in *Figures 1b* and *1c*. Frame fields are discussed in the following section.

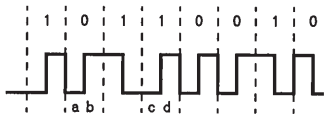

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FIGURE 1a. Differential Manchester Data Stream Example

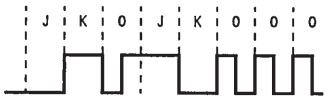

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FIGURE 1b. SD Field is Always JK0JK00

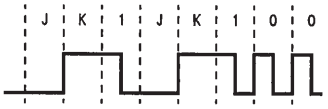

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FIGURE 1c. The First Six Bits of the ED Field is Always JK1JK1

The basic transmission units on a Token Ring Network are tokens and frames. Tokens and frames traveling around the ring are differential Manchester encoded.

TOKEN RING FRAME

A Token Ring frame contains several fields; Starting Delimiter (SD), Access Control (AC), Frame Control (FC), Destination Address (DA), Source Address (SA), Information field, Framecheck Sequence (FCS), Ending Delimiter (ED) and Frame Status (FS) as shown in *Figure 2*.

A single 24-bit frame called a *token* continuously traverses the ring. A token consists of three fields; SD, AC and ED. A station must acquire the token before transmitting data onto the network.

The two other frames are the data frame and the MAC frame which control certain management functions on the Token Ring Network.

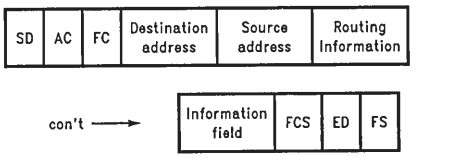

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FIGURE 2. Token Ring Frame has several fields. A token is a special frame which has only three fields; SD, AC and ED.

A brief description of the frame fields shown in *Figure 2* are given in the following.

- Starting Delimiter (SD): This field indicates the beginning of a frame. SD is a single byte with the pattern shown in *Figure 1b*.
- Access Control (AC): This field is a single byte which contains priority information and indicates a token or frame.
- Frame Control (FC): This field is a single byte which indicates the frame as data or MAC-Media Access Control.
- Destination Address: Destination address identifies the station that is to copy the frame. This address always consists of six bytes.
- Source Address: Source address identifies the station that originated the frame. This address always consists of six bytes.
- Routing Information: Optional routing information follows the source address when the frame leaves the ring. This field, when present, consists of a 2-byte routing control field and up to eight 2-byte route designators.
- Information Field: Information Field contains an integral number of bytes of data. In an IBM Token-Ring Network, a ring station can hold a token for 10 ms, which limits the maximum frame size that a station can transmit.
- Framecheck Sequence (FCS): This field contains a 4-byte cyclic redundancy check (CRC) performed on the FC, DA, SA and information fields.
- Ending Delimiter (ED): ED is a single byte where the first six bits of the field indicate end of frame. One bit indicates error and another indicates whether successive frames will follow.
- Frame Status (FS): FS is a single byte field that indicates if the destination station recognized the address and successfully copied the frame.

FRONT END

A block diagram of the FEM and its associated external components is shown in *Figure 3*. The FEM provides the interface functions necessary to transmit and receive differential Manchester encoded data over the transmission channel. These functions consist of the following:

- Equalization of incoming received signal.
- Detection of the received signal.
- Clock recovery and retiming of the received data.
- Transmission of output data.
- Ring Insertion.

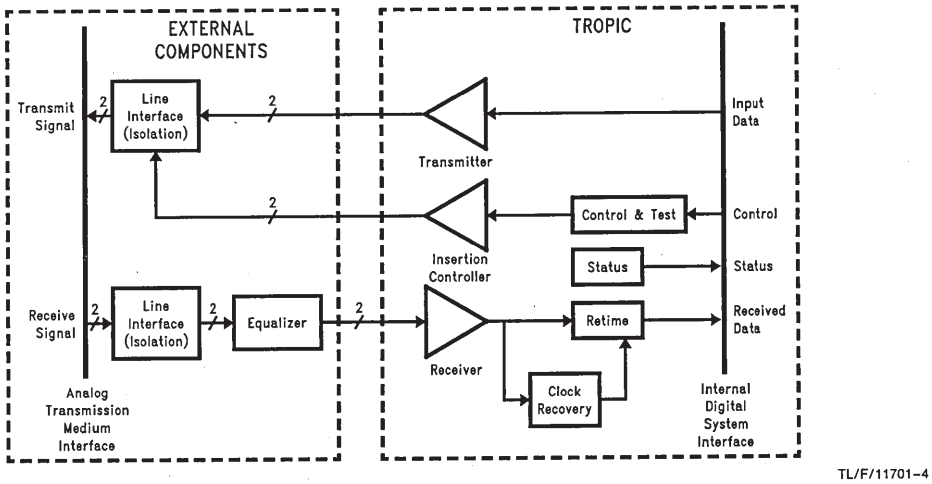

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FIGURE 3. Front End Macro (FEM) Functional Block Diagram Includes the TROPIC Internal Blocks and the External Equalizer Block

TIMING

Table II describes the timing characteristics of the system at the two bit rates—4 Mbps and 16 Mbps.

TABLE II. 4 Mbps and 16 Mbps Timing Characteristics

Parameter	4 Mbps	16 Mbps
720° = bit length	250 ns	62.5 ns
360° = half-bit length or mid-bit	125 ns	31.25 ns
1°	347 ps	87 ps
Clock Rate	8 MHz	32 MHz
All 0's pattern (idles)	4 MHz	16 MHz
All 1's pattern	2 MHz	8 MHz

RECEIVER

The FEM receiver consists of the following blocks; Receiver, Clock Recovery and Retime as shown in *Figure 3*. Data passes through the Equalizer and Receiver to the Retime and Clock Recovery block which samples half bit elements of the differential Manchester coded signal. The FEM receiver passes these signal elements to the internal digital system interface which decodes the signal elements to data bits (binary zeroes and one's) or code violations (non-data J's and K's). The performance of the FEM and transmission system depends upon the detectability of the half bit signal elements as shown in *Figure 4*.

The concept of a minimum valid signal at the FEM receiver input or Equalizer output is fundamental to detecting signal elements in the system environment. This minimum valid signal results from the worst case communication system distortions and has the minimum "EYE" pattern that the receiver must be expected to demodulate. The EYE pattern is determined by communication system parameters such as loss, noise and distortion from the transmission medium and equalizer circuit. System performance is determined largely by how accurately the local clock can define the center of the data EYE and the accuracy that the data sample is discerned in the presence of noise. The height and width of the window EYE must meet receiver requirements to reliably sample incoming signals. The EYE height specifies the minimum signal amplitude that the receiver is able to reliably detect a high or low. Signals with amplitudes falling within the EYE cannot be reliably detected as a high or low. The EYE width specifies the minimum phase range required by the PLL to lock onto and retime incoming signals.

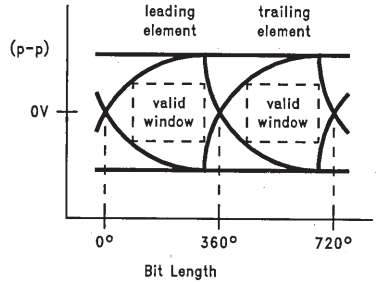

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FIGURE 4. A bit is sampled at the leading and trailing symbol elements. The window formed by the EYE pattern must meet receiver input requirements.

RECEIVE TIMING ALIGNMENT

All stations on a ring derive their clock from the Active Monitor which is the first station inserted into the ring. If the active monitor is de-inserted from the ring, another station takes its place as the Active Monitor. There is always one and only Active Monitor per ring. The Active Monitor sets the timing for the rest of the ring via the retiming of frames and tokens as they pass through the Active Monitor.

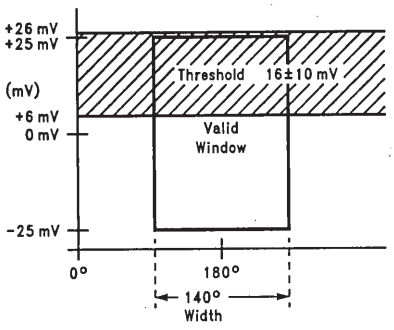
Each station, including the active monitor, recovers the clock embedded in the differential Manchester encoded signals when receiving frames or tokens. The difference between an Active Monitor and other stations is in transmitting frames and tokens back onto the ring. Stations use the recovered clock (the output of the clock recovery circuit of *Figure 3*) when transmitting differential Manchester encoded data while the Active Monitor uses a local reference clock (this clock is provided by the 32 MHz crystal). Frames and tokens coming out of the Active monitor have no jitter because they use a local reference clock. Jitter accumulates as the frame or token moves downstream from the active monitor. Each successive station will add jitter to the signal or frame until it has gone full circle back to the Active Monitor where the jitter is removed and the frame or token is transmitted jitter-free. The Active Monitor always receives the worse case accumulated jitter since it is the last station on the ring. Accumulated jitter increases with increasing number of stations and cable lengths between the Active Station and downstream station.

There are various sources of jitter on the ring which are illustrated in *Figure 7*. The jitter sources are found internal and external to the TROPIC. Transferred jitter, transmit channel jitter, concentrator jitter and receive channel jitter are sources external to the TROPIC. PLL jitter and transmitter jitter are sources internal to the TROPIC.

- Transferred jitter represents the accumulated jitter for all stations between the Active Monitor and current station.
- Transmit channel jitter is the jitter contributed by the lobe cable between the UMIC and the concentrator.
- Concentrator or TCU (Trunk Coupling Unit) jitter is the jitter contributed by the concentrator unit.
- Receive channel jitter is the sum of the jitter contributed by the lobe cable between the concentrator and the UMIC, the concentrator jitter and the transmit channel jitter. When using active concentrators (also called Retimed TCU's) the receive channel jitter is only the jitter contributed by the lobe cable between the concentrator and the UMIC.
- PLL jitter is the jitter contribution by the PLL of the current station, with zero transferred jitter.
- Transmitter jitter is the jitter contributed by the transmitter.

The receiver EYE width budget takes into account signal misalignment caused by a variety of sources including the jitter elements discussed above. The receiver PLL and set-up and hold times internal to TROPIC must also be accounted for in the timing budget.

To accommodate for worse case misalignment, the EYE width shall be greater than 140° at 4 Mbps and 240° at 16 Mbps as illustrated in *Figure 5*. The equalizer enables the incoming signals to meet the timing requirements specified above to ensure that the receiver samples valid data. The EYE width specification allows for jitter contribution from a variety of sources both internal and external to the TROPIC.



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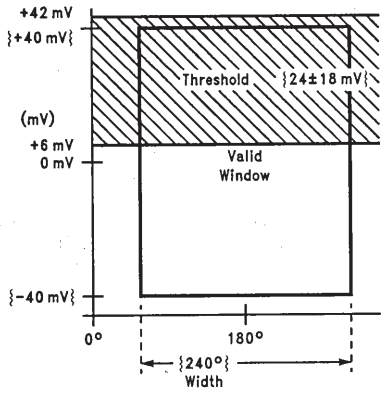
a) Window for 4 Mbps



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b) Window for 16 Mbps

FIGURE 5. The EYE must meet the receiver window characteristics above to maintain signal integrity.
a) Window characteristic for 4 Mbps.
b) Window characteristic for 16 Mbps.

RECEIVE THRESHOLD AND HYSTERESIS

The EYE height must be at least 50 mV peak to peak at 4 Mbps {80 mV peak to peak at 16 Mbps} to accurately detect high and low signal levels. The FEM receiver input threshold is 16±10 mV peak to peak (6 mV to 26 mV) at 4 Mbps{24±18 mV peak to peak (6 mV to 42 mV) at 16 Mbps}. The threshold offset prevents low level noise from being interpreted as data signals. Input signals below the threshold will not be detected by the receiver. Input signals above the threshold will be received and passed on to the data re-timing latch and to the phase detector in the clock recovery block with no alteration. The receiver has no hysteresis.

EQUALIZER CIRCUIT

The equalizer circuit is external to the TROPIC and located between the isolation transformer and the receiver as shown in *Figure 5*. The equalizer is a high pass filter which compensates for lowpass behavior of the cable plant. The cable distorts the signal as it propagates down the line causing inter-symbol interference (inter-symbol interference forms the eye pattern) at the receiving station. The eye pattern formed by signals directly from the isolation interface (without equalization) will not meet the minimum "EYE" that the receiver requires to sample data. The equalizer filters the signals coming from the isolation interface to meet the minimum "EYE" which the TROPIC receiver requires to accurately sample data.

The external equalization circuit is composed of resistors, capacitors and two LM3045's (npn transistor array) as illustrated in *Figure 6a* in Appendix A. Signals proceed from right to left of the schematic. *Ring In A* and *Ring In B* are connected to the lobe cable which attaches to the ring. *RINB* and *RINA* are connected to TROPIC's receive pins. One LM3045 (Q1′–Q5′) is used for the 16 Mbps equalization circuitry and the other is used for the 4 Mbps (Q1–Q5) equalization circuitry. The choice of ring speed is software programmable, which in turn selects the proper equalizer via TROPIC's output control pins *~16 Mbps* and *~4 Mbps*. When running at the 16 Mbps ring speed, *~16 Mbps* is low (disabling the 4 Mbps circuitry (Q1–Q5)) and *~4 Mbps* output is in TRI-STATE® (enabling the 16 Mbps circuitry (Q1′–Q5′)). In the 4 Mbps mode *~16 Mbps* is in TRI-STATE and *~4 Mbps* is low.

Follow the recommended layout rules given in the "Layout Guidelines for the Token Ring Adapter Using the DP8025" to reduce the incident of improper layout that may adversely affect the equalizer circuit.

The 16 Mbps equalizer filter is composed of R24, R5 and C7. The 4 Mbps equalizer filter is composed of R33, R32 and C16. These combined with the transistors form high-pass filters which compensates for the lowpass cable characteristics. C14 and C15 decouples the DC component of the signal coming from the equalizer.

INPUT IMPEDANCE AND FILTERING

To prevent loading on the equalizer circuit, the magnitude of the differential input impedance of the FEM receiver is greater than 750Ω below 16 MHz and drops no more then 6 dB/octave from 16 MHz to 64 MHz. To provide protection against external noise, the receiver input has a lowpass filter with a single pole, located at 16±3.5 MHz for 4 Mbps operation and at 64±14 MHz for 16 Mbps operation.

COMMON MODE REJECTION

The FEM input has the following common mode rejection over the range of input signal levels:

TABLE III. Common Mode Rejection

Spectrum	Common Mode Rejection
0–8 MHz	> 40 dB
8–80 MHz	> (6 dB/octave decrease from 8 MHz value)

DATA RETIMING LATCH

Once data passes through the Receiver, shown in *Figure 3*, the data clock is extracted in the Clock Recovery block and used to realign the received data. The FEM con- tains a latch which samples the data according to the recovered clock and holds until the next clock cycle. Realigned data, still in Manchester coding, proceeds to the Protocol Handler. The Protocol Handler converts the serial Manchester encoded data stream into byte parallel data usable by the Multiprocessor Unit (MPU) within TROPIC. Information on the PH and MPU is found in the DS8025 TROPIC data sheet.

CLOCK RECOVERY—PLL

The recovered data clock is derived from the incoming differential Manchester coded signal by means of a Phase-Locked Loop (PLL) timing circuit in the FEM. The PLL uses the inherent timing information from the mid-bit transitions of the incoming binary data. The basic objective of the PLL is to derive a data clock which defines the center of the valid data EYE-Ideal Sampling Point (as shown in *Figure 5*) in a stable manner. The performance of the communication system using the FEM is heavily dependent on the characteristics of the PLL. We highly recommend using the procedures given in "Layout Guidelines for a Token Ring Adapter Using the DP8025" —Application Note 816 when laying out external capacitors and resistors associated with PLL4 and PLL16 pins.

TRANSMITTER

In the transmit mode the Protocol Handler encodes the data into differential Manchester code then sends it to FEM. The FEM transmitter drives the data stream to the isolation interface as shown in *Figure 3*. The transmitter output ROUTA and ROUTB are complimentary open-collector outputs with a nominal differential swing of ±4.0V. The differential voltage between ROUTA and ROUT B is referred to as TRANSMIT DATA.

The rise and fall times (measured from 10% to 90%) of the TRANSMIT DATA is below 58°.

RING INSERTION

The ring insertion mechanism places a DC voltage on the medium interface. The DC voltage output on PHANTA and PHANTB is transparent with respect to the TRANSMIT DATA. When "ON", the driver activates a relay in the Multistation Access Unit (MAU) and inserts the station into the ring. When "OFF", the station is de-inserted from the ring. To assure prompt de-insertion in the case of power-off on a slowly decaying voltage supply, the phantom drive will turn off using an undervoltage detection circuit. An undervoltage is detected if the supply voltage is less than 4.0±0.4V and is decaying faster than 0.2 V/s. The phantom voltage will drop from 4V to below 1V within 350 ms of the undervoltage.

Under fault conditions where the transmission cable wires are accidentally shorted to ground, the FEM limits the available current to a value between 4 mA and 20 mA. Under normal operation the current from PHANTA and PHANTB is 1 mA.

APPENDIX A: DETAILED EXTERNAL FEM CIRCUITRY

TABLE IV. LM3045 NPN Transistor Array Pin Description

npn	C	B	E
Q1	1	2	3
Q2	5	4	3
Q3	8	6	7
Q4	11	9	10
Q5	14	12	13

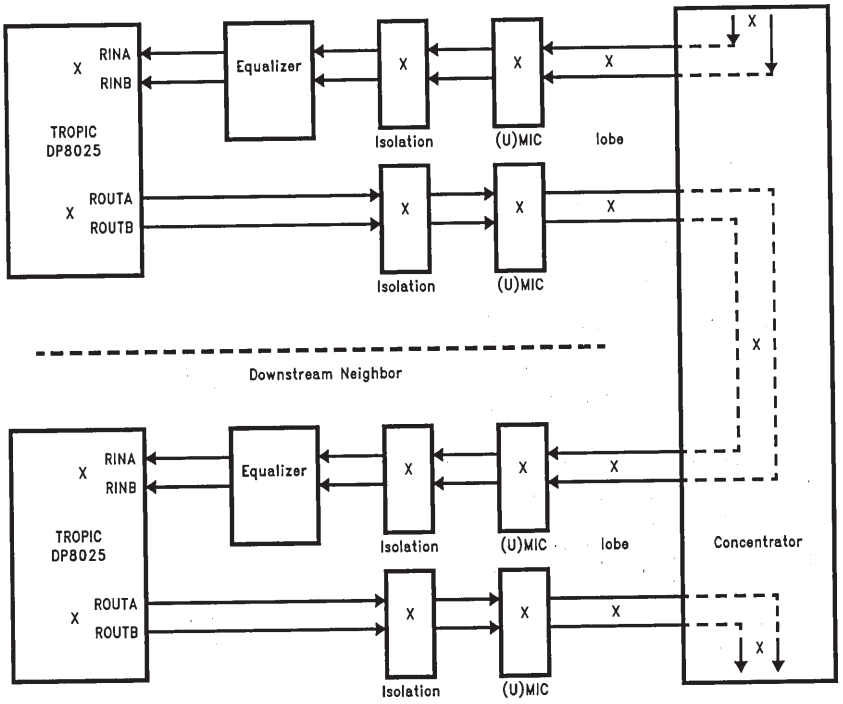
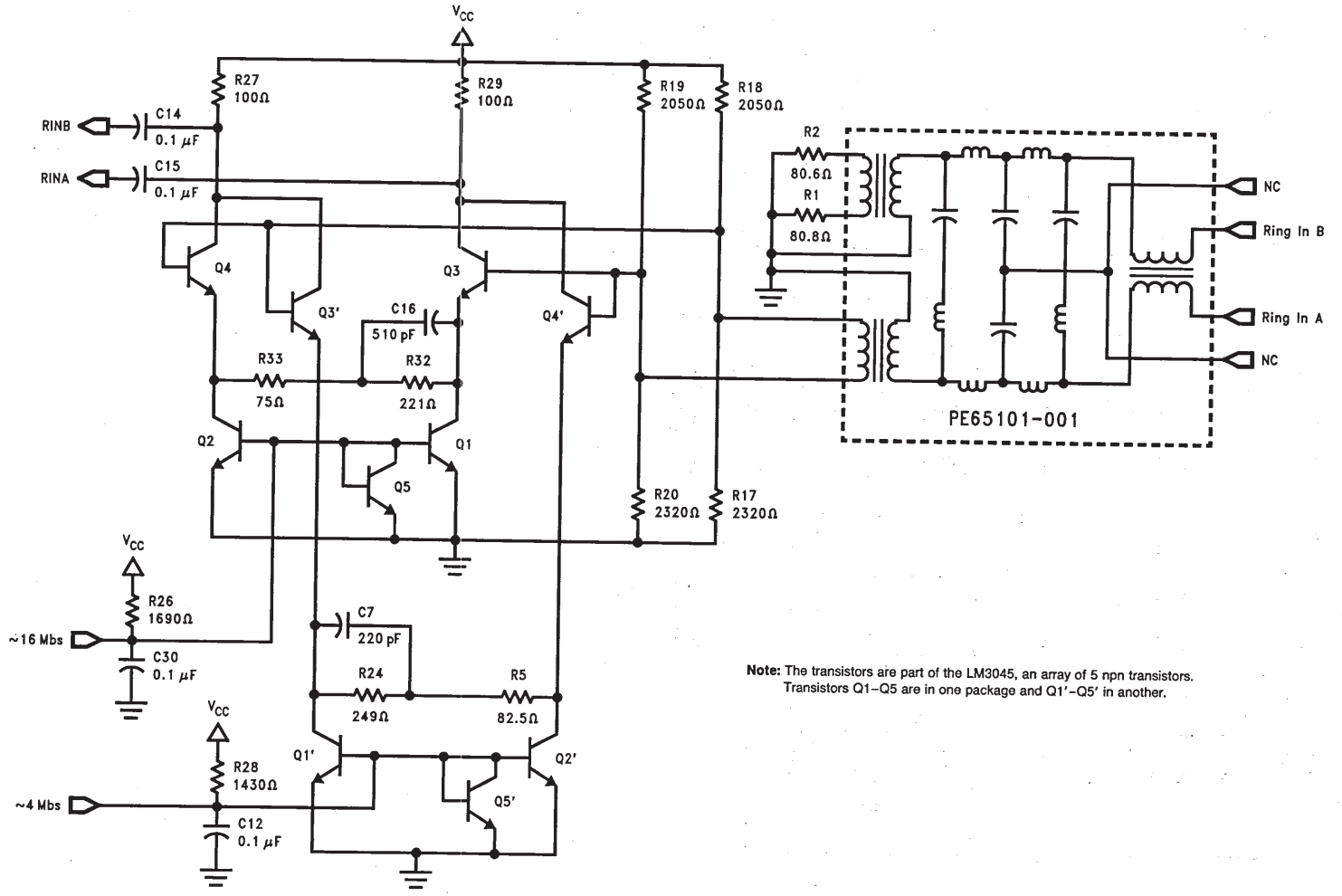


FIGURE 7. Token Ring Signal Path and Sources of Jitter (Jitter Sources are Designated with an "X")



Note: The transistors are part of the LM3045, an array of 5 npn transistors. Transistors Q1–Q5 are in one package and Q1′–Q5′ in another.

FIGURE 6a. Receiver External Components Schematic

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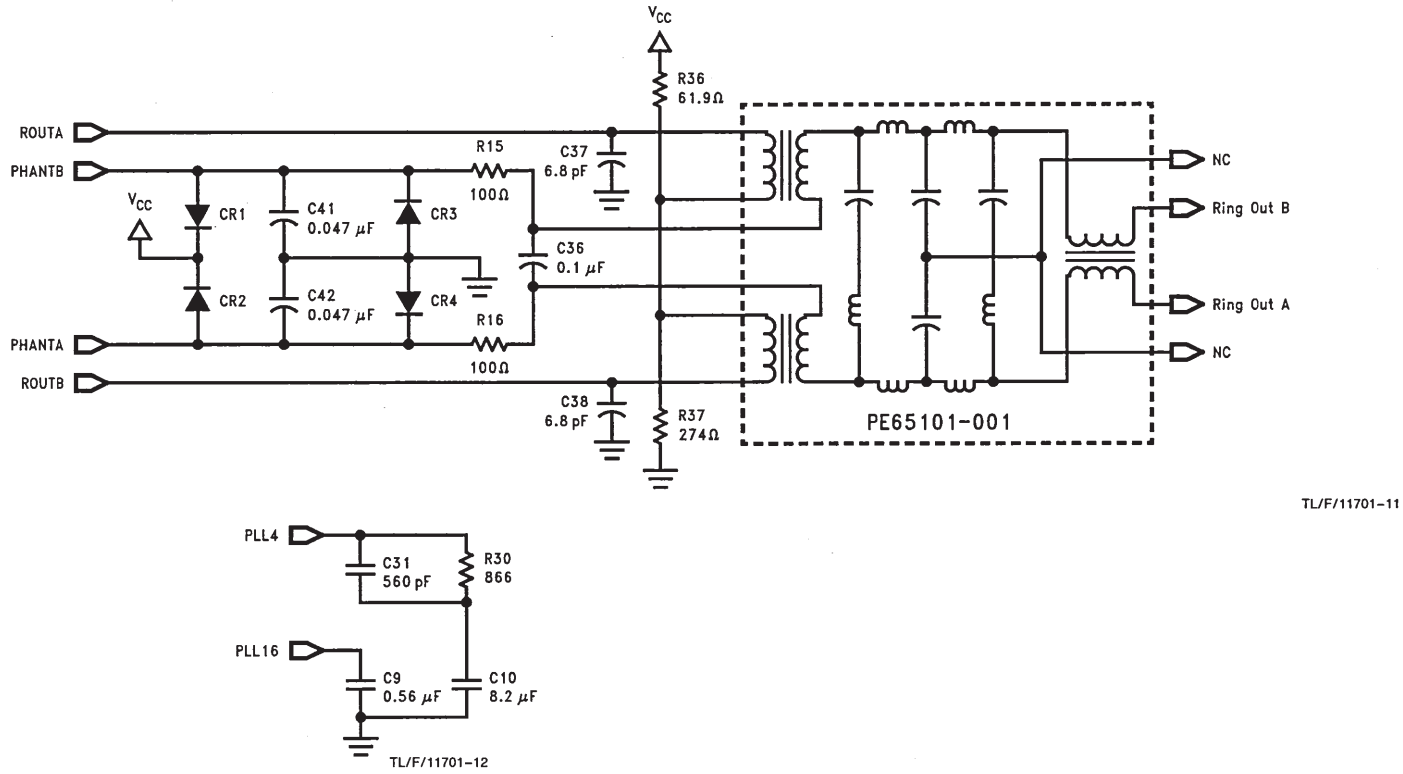

FIGURE 6b. Transmitter and PLL Filter External Components Schematic