# Layout Guideline for a Token Ring Adapter Using the DP8025 (TROPIC™)

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Application Note 816
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## 1.0 INTRODUCTION

When designing a Token Ring adapter using TROPIC, the PCB layout must be divided into two distinct regions: the digital section, and the analog front-end section.

The digital section will contain host interface logic, miscellaneous glue logic, all memory devices, and the majority of the TROPIC pins. The layout of this section should follow standard common-sense digital layout techniques such as minimizing trace lengths, daisy-chaining bus signals, etc.

The analog front-end section, however, is extremely sensitive to physical layout in two areas: logic switching noise immunity, and electromagnetic interference. An improperly designed front-end layout can add excessive jitter to data repeated on the ring. Therefore, the layout of the analog section must be optimized to obtain correct operation.

**If possible, copy an existing analog layout which has been proven,** such as that used in National DP8025EB-AT 16-bit Adapter. Make an attempt to copy the layout exactly, without being tempted to make minor changes. The more closely the final layout matches the original, the greater the probability of success on the first pass.

Assuming that it is not possible to copy an existing analog layout, the following guidelines have been provided to assist a board designer in placing components, connections, and prioritizing the position of wiring nets. These guidelines have been developed through experience and theoretical analysis, most of which will be recognized simply as good design practice applied to this application. Unfortunately, these guidelines cannot, by themselves, guarantee correct operation. This can only be accomplished through thorough testing of the final design.

## 2.0 GENERAL COMPONENT AND SIGNAL PLACEMENT

The receive transformer module should be placed adjacent to the ring connector, followed by the equalization components and the TROPIC. All receiver components should be located near the edge or corner of the board to facilitate the isolation of the power and ground planes. The receive path components should be grouped together, and should be located between the receive transformer and TROPIC.

The transmit transformer module should be located between the TROPIC and the ring connector. The transmit path should be separated from the receive path, even if it means longer routing of the traces. It is still necessary to attempt to minimize transmit trace length to avoid radiation problems.

The 32 MHz oscillator should be located close to TROPIC but away from the analog section.

## 3.0 POWER AND GROUND PLANE AREAS

The power and ground planes need to be separated into three areas: Digital power/ground, Analog power/ground, and Chassis ground. This plane isolation helps to prevent digital logic noise from interfering with the analog circuit operation, and prevents all circuit noise from coupling onto the chassis. The separation between plane areas should be accomplished with a 0.100″ gap or void in the plane copper. The electrical connection between the digital and analog planes should be made through a single connection point approximately 0.300″ wide (a bridge). A low-frequency (22 $\mu$F) and a high-frequency (0.1 $\mu$F) decoupling capacitor should be placed in the bridge area. *Figure 1* illustrates the isolation of the plane areas.

A higher level of noise isolation can be achieved if the digital and analog plane areas are completely separated (no bridge), and electrically connected via 0Ω resistors placed where the bridge would be located. In this type of implementation, the decoupling capacitors would go on the smaller plane area (analog) near the resistor to plane connection. This case would also allow ferrite beads to be used instead of the 0Ω resistors to provide better high frequency rejection.

The analog plane area should include all receive path components, all receive data signals, and the PLL filter components. The transmit and phantom drive components and signals should be placed in the digital plane under the analog plane as shown on *Figure 1*.

The chassis ground plane isolation is designed to limit the amount of high-frequency (> 100 MHz) radiated energy. This plane area should include all space underneath the chassis connection (i.e., the mounting brackets and/or screws), the ring connector, and the transmit and receive traces which run from the ring connector to their respective filter module. The power layer in this area should be voided.

All other logic components not previously mentioned should be included in the digital plane area.

**Note:** Care should be taken so differential lines (either analog or digital) are not routed in the channel adjacent to the edge of a plane. This could cause an imbalance to ground between the closer and further traces of the pair.

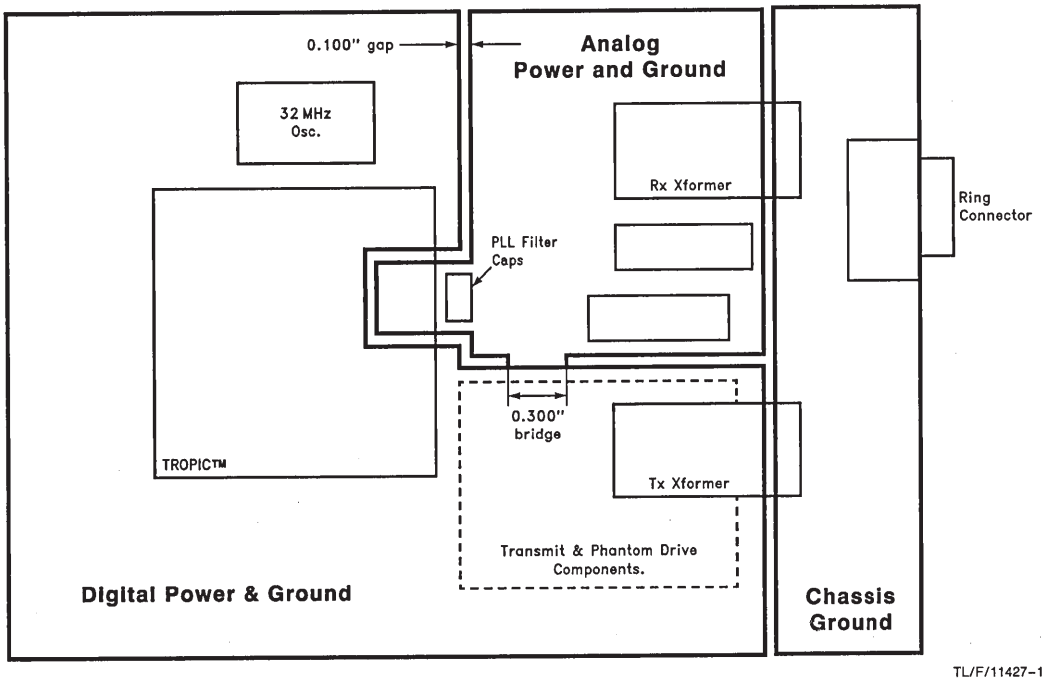


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**FIGURE 1. Power and Ground Plane Isolation**

### 4.0 DISCHETE COMPONENT PLACEMENT AND ROUTING PRIORITY

All discrete components should be placed as close to their associated TROPIC/equalizer/transformer module pins as possible. The next section should provide a better feel for how to place the discretes, once their general location has been determined. The priority in placement is as follows:

**Note:** The component references given correspond to the NSC DP8025EB-AT 16-bit Adapter schematics.

1. C9
2. C10, C31, R30
3. R27, R29, C14, C15
4. R24, R5, C7
5. R32, R33, C16
6. R17, R18, R19, R20, R1, R2
7. C32, C33
8. C37, C38
9. R15, R16, C36, CR1–CR4

The priorities assigned must be used with a little common sense. For example (with the exception of C9) a high-priority component may be moved slightly to provide a better placement for several low-priority components. (Refer to Schematic Diagram on *Figure 3*.)

### 5.0 ANALOG TRACE ROUTING

The cardinal rule of analog trace routing is to keep the area enclosed by a circuit loop as small as possible to minimize the potential of magnetic coupling. This can conflict, however, with the general rule of keeping trace lengths short. For example, if circuit components are positioned along three sides of a square, the best return route is back along the same three sides of the square, NOT directly back along the fourth side. This rule must be carried to extremes. Furthermore, there should never be an unnecessary via or feedthrough inside the circuit loop. This also implies that the circuit loop should never encircle the power/ground planes (i.e., part of the circuit loop above and part below these planes). The concept is illustrated in *Figure 2*.

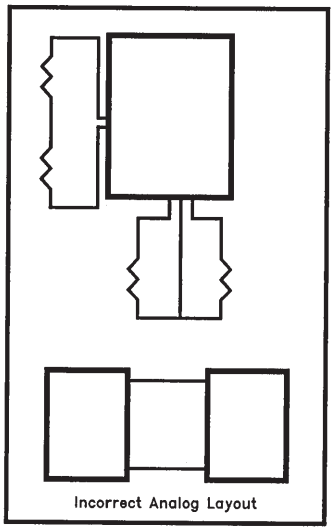
A simple case of this guideline applies to differential signal pairs. The two traces of the pair should always be routed in adjacent channels. Five sets of differential pairs exist in the TROPIC front-end section:

- Pre-filtered transmit data (TROPIC to transformer)
- Filtered transmit data (transformer to ring connector—ring data out)
- Pre-filtered receive data (ring connector to transformer—ring data in)
- Filtered receive data (transformer to equalizer circuits)
- Equalized receive data (equalizer to TROPIC)

The Phantom Drive signals are not a differential pair and are not extremely sensitive. However, these signals are still capable of picking up enough noise to create false wire faults if placed too close to the transmit path.

**Note:** To limit radiation potential, it is advisable to keep the differential transmit and receive traces in the signal layer adjacent to the ground layer.

To reduce capacitive coupling, each circuit loop should be separated from the others. Circuit loops can be separated

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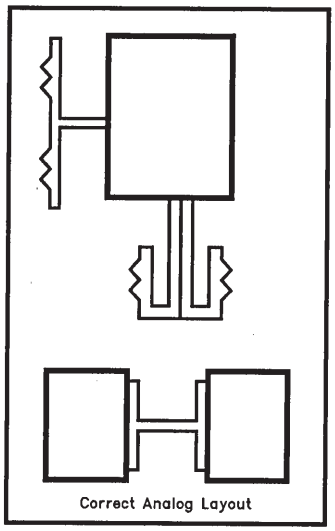


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**FIGURE 2. Analog Trace Layout Examples**

either by physical space (if located on the same signal layer), or by placement on signal layers on opposite sides of the power/ground planes. Items in the following list should be isolated from each other.

- Receiver and equalizer path
- Transmit path
- PLL filter components
- Phantom Drive path

### 6.0 DIGITAL TRACE ROUTING

Placement of digital components and routing of digital traces should follow standard common-sense digital layout techniques such as minimizing trace lengths, daisy-chaining bus signals, etc. Except for the 32 MHz clock signal, the Transmit path, and the Phantom Drive path, auto-routing of traces in this section is permissible.

Care should be taken when routing the 32 MHz clock signal from the oscillator to TROPIC. This trace should be kept as short as possible and should contain no vias. The Transmit and Phantom Drive traces should be routed away from any digital signals.

### 7.0 DECOUPLING CAPACITORS

As a general rule-of-thumb for a multi-layer PCB, using one 0.1 $\mu$F bypass capacitor for each digital component provides adequate high-frequency decoupling. For most components, locating the capacitor near the $V_{CC}$ pin and tying into the power and ground planes is sufficient. For high-speed switching components, such as a crystal oscillator, the capacitor should be tied directly across the component power pins via traces.

Depending on the size of the PCB a number of low-frequency capacitors (10 $\mu$F–22 $\mu$F) should be placed around the periphery of the PCB. Two of these should be located near the host bus edge connector power entry pins.

As indicated in the discussion on plane isolation, a low-frequency (22 $\mu$F) and a high-frequency (0.1 $\mu$F) decoupling capacitor should be placed directly in the bridge area between the analog and digital plane sections. Additionally, the TROPIC analog supply pins should be directly decoupled. This should be accomplished by connecting 0.1 $\mu$F capacitors via traces directly across TROPIC pins M06–M07 and L06–N07.

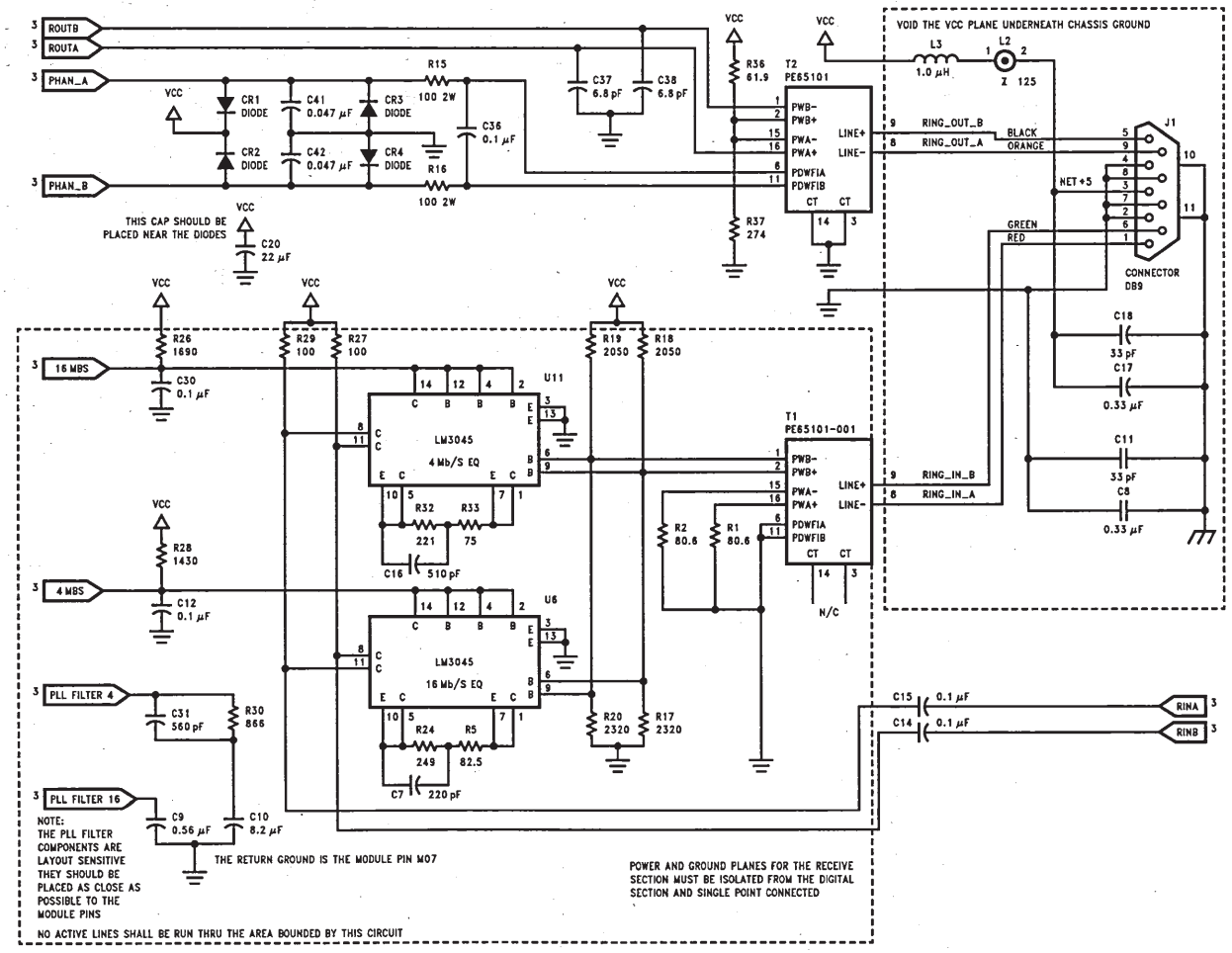


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**FIGURE 3. Front End Schematic**