Integrated Circuit Systems, Inc.

ICS1394

T-52-33-49

Video Dot Clock Generator

Features

- Low cost - eliminates need for multiple crystal clock oscillators in video display subsystems
- Strobed /transparent frequency select options
- Mask-programmable frequencies
- Glitch-free frequency transitions
- Compatible with Industry STD VGA Controllers
- Provision for two external frequency inputs
- Low power CMOS device technology
- Small footprint - 20 pin DIP or SO

Applications

- 85 MHz Guaranteed Performance
- EGA - VGA - Super VGA XGA video adapters
- High resolution MAC II displays
- Workstations
- LCD and other flat panel display systems
- 8514A - TMS 34010 - TMS 34020
- Motherboard - PS2™ display systems

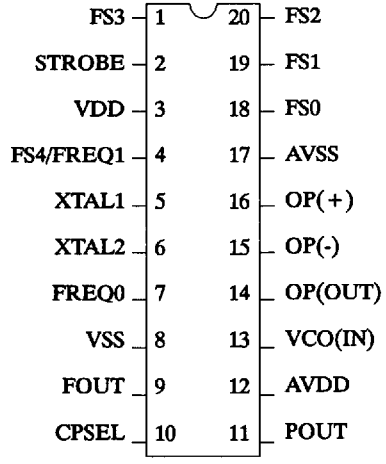
B

Introduction

The **ICS1394 Dot Clock Generator** is an integrated circuit capable of generating up to 32 video dot clock frequencies for use with high performance video display systems. Utilizing CMOS technology to implement all linear, digital and memory functions, the **ICS1394** provides a low power, small footprint, low cost solution to the generation of video dot clocks. Outputs are compatible with **XGA,VGA, EGA, MCGA, CGA, MDA,** as well as the higher frequencies needed for advanced applications in desktop publishing and workstation graphics. Provision is made via a single level custom mask to implement customer specific frequency sets. Phase locked loop circuitry permits rapid glitch-free transitions between clock frequencies.

Principal applications for these products include generating dot clock frequencies for EGA, VGA, Super VGA, and XGA graphics products in the IBM-compatible world, as well as for high resolution MAC II and workstations. Applications utilizing 8514A and TMS 34010 and TMS 34020 benefit as well, with significant performance improvements and cost reductions in all of these applications.

Pin Configuration



Ordering Information
ICS1394NXXX (DIP Package)
ICS1394MXXX (SO Package)
(XXX = Pattern number)

ICS1394

Circuit Description

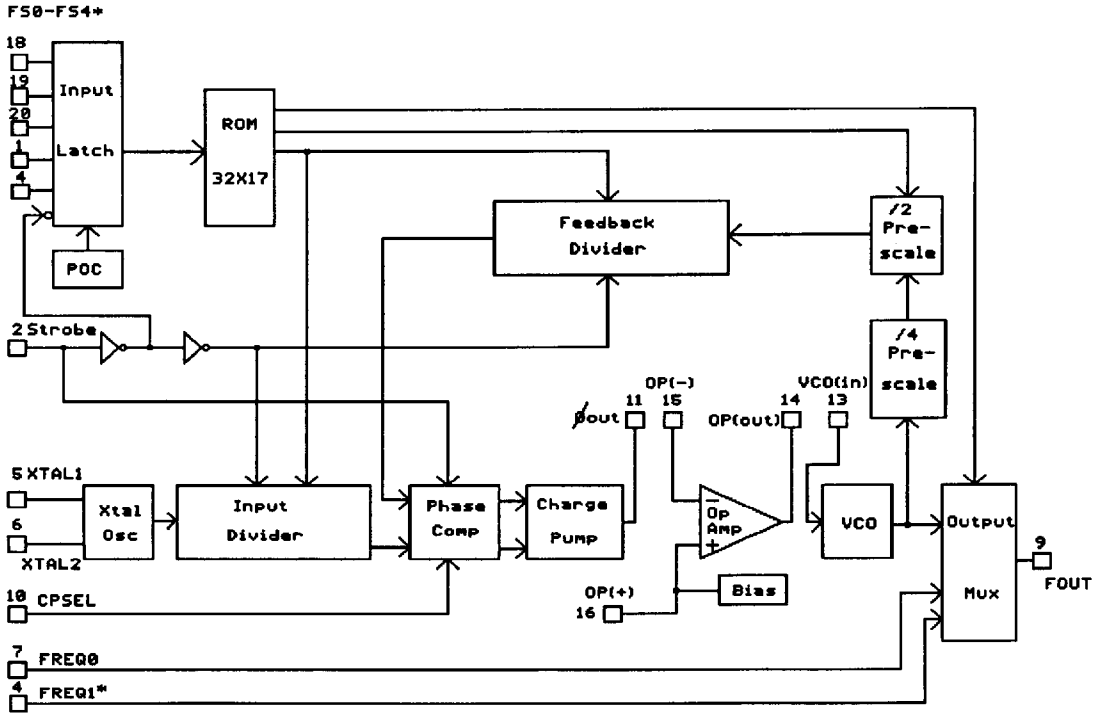
INPUT LATCH: If the latched data option is selected, a 4 (5) bit **INPUT LATCH** is loaded with one of 16 (32) selected frequencies by an active high transition of **STROBE**. While **STROBE** is high, the **PHASE COMPARATOR** is disabled, maintaining the **CHARGE PUMP** and **FILTER** in their high impedance state. The **PHASE COMPARATOR** output is forced to a zero phase error state to insure that the next input transition will force an output of the correct polarity to drive the **VCO** to lock at the new frequency. **STROBE** must remain high long enough to allow input lines **FS[0-4]** to propagate through the input latch, the **ROM**, and to be set up for at least one clock to the **DIVIDERS**. **STROBE** enables the **DIVIDERS** to be loaded with the current selected **ROM** value on the next clock pulse. When the **STROBE** pulse goes low, the data on the latch inputs is latched, the **PHASE COMPARATOR** is enabled to accept the next edge, and the **DIVIDERS** are enabled to count down on the next clock. Metal options permit the strobe creature to be disabled in systems where stable frequency select data is available.

ROM: The **ROM** is a mask programmable ROM containing the **FEED BACK DIVIDER** values, the **INPUT DIVIDER** values, and a bit to force the **PRESCALER** to divide by 8 instead of by 4. Additional bits select the signal which is passed as an output.

POC: An internal power-on clear (**POC**) clears the input latch to all zeros, enabling the **ROM** to output the frequency value stored in location 0. The **FEEDBACK DIVIDER** and **INPUT DIVIDER** are not cleared; they power up to a random count (maximum 127) and count down to zero before they are loaded with the proper value.

DIVIDERS: The **INPUT** and **FEEDBACK DIVIDERS** are 2^7 synchronous down counters which are loaded when they decrement to zero or when a **STROBE** occurs. The preload values for the **DIVIDERS** are stored in the **ROM**. Both the zero reload and the strobe reload require a clock pulse to store the data.

Block Diagram



Pin Descriptions

The following table provides the pin functions of the **ICS1394** in the 20 pin DIP or SO package.

PIN NUMBER	PIN SYMBOL	TYPE	DESCRIPTION
1	FS3	IN	Frequency select input, TTL compatible (MSB)*
2	STROBE	IN	Negative edge clock for select inputs, TTL compatible
3	VDD	-	5 Volt digital power pin
4	FS4/FREQ1*	IN	Frequency select input, TTL compatible (MSB)*, or externally generated frequency input 1
5	XTAL1	IN	Crystal interface / External oscillator input
6	XTAL2	OUT	Crystal interface
7	FREQ0	IN	Externally generated frequency input 0
8	VSS	-	Digital ground
9	FOUT	OUT	Clock output, TTL compatible
10	CPSEL	IN	Phase comparator polarity select (pulled up to Vdd if left open)
11	POUT	OUT	Phase comparator output
12	AVDD	-	5 Volt analog power pin
13	VCO(IN)	IN	Voltage controlled oscillator input
14	OP(OUT)	OUT	Op-amp output
15	OP(-)	IN	Op-amp negative input
16	OP(+)	IN	Op-amp positive input
17	AVSS	-	Analog ground
18	FS0	IN	Frequency select input, TTL compatible (LSB)
19	FS1	IN	Frequency select input, TTL compatible
20	FS2	IN	Frequency select input, TTL compatible

* Note: Devices which provide more than 16 frequencies utilize pin 4 as the MSB address bit (FS4), thus permitting only one external source of video dot rates (FREQ0). If only 16 frequencies are required, then pin 4 may function as a second external source of video dot rates (FREQ1).

ICS1394

Applications

Layout Considerations

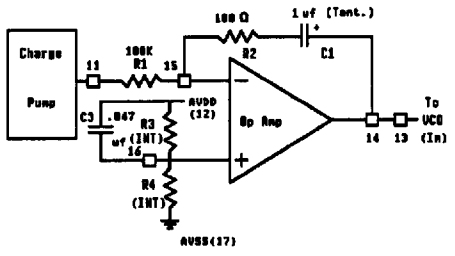
Utilizing the ICS1394 in video graphics adapter cards or on PS2™ motherboards is simple but does require precautions in board layout if satisfactory jitter-free performance is to be realized. A low series inductance bypass capacitor of .047mF should be utilized between digital Vss (8) and V_{DD} (3). AVss (17) should be connected to ground at the card edge connector, and care should be exercised in ensuring that components not related to the ICS1394 do not use this ground. In applications utilizing a multi-layer board, both AVss and Vss should be directly connected to the ground plane.

Power Considerations

The ICS1394 product requires an AV_{DD} supply free of fast rise time transients. This requirement may be met in several ways and is highly dependent on the characteristics of the host system. A VGA adapter card is unique in that it must function in an unknown environment. +5 Volt power quality is dependent not only on the quality of the power supply resident in the host system but also on the other cards plugged into the host's backplane. Power supply noise ranges from fair to terrible. As the VGA adapter manufacturer has no control over this, he must assume the worst. The best solution is to create a clean +5 Volts by deriving it from the +12 Volt supply by using a zener diode and dropping resistor. A 470 ohm resistor and 5.1 Volt Zener diode are the least costly way to accomplish this. A .047 to .1mF bypass capacitor tied from AV_{DD} (12) insures good high-frequency decoupling of this point.

Laptop and notebook computers have entirely different problems with power. Typically, they have no +12 Volt supply; however, they are much quieter electrically. Because the designer has complete control of the system architecture, he can place sensitive components and systems such as the RAMDAC and dot clock away from DRAM and other noise-generating components. Most systems provide power that is clean enough to allow for jitter-free dot clock performance if the +5 Volt supply is decoupled with a 47 ohm resistor and 33 mF Tantalum capacitor. AV_{dd} is not particularly sensitive to supply voltage and will work fine at 4.1 Volts over the full frequency range of the ICS1394, so drop across the decoupling resistor is not a problem.

Typical Loop Filter Configuration



Loop Filter

Normal applications of the ICS1394 should utilize the internal op-amp to implement the loop filter. VCO frequency is determined by the voltage that exists between AV_{DD} and **VCOin (13)** with frequency increasing as **VCOin** approaches AV_{SS}. The positive input to the internal op-amp, **OP+ (16)** is internally biased and bypassed to AV_{DD}. An additional .047mF ceramic capacitor should be connected between **OP+** and AV_{DD} to provide adequate low frequency decoupling. Normally, a 100K ohm resistor should connect **Fout (11)** and **OP- (15)**. A 1 mF Tantalum capacitor in series with a 100 ohm resistor should be connected between **OP-OUT (14)** and **OP- (15)** with the positive lead of the capacitor tied to **OP-OUT**. **OP OUT (14)** should be directly connected to **VCO-in (13)**. This configuration provides high noise immunity and results in low phase-jitter in the output frequency spectrum. All passive loop filter components should be laid out tightly to minimize noise pickup. Digital signals should be spaced well away from these components.

CSPEL(10) determines the polarity of the charge pump output. It is internally pulled high, but should be connected directly to V_{DD} for improved noise immunity if the op-amp or any other external active filter which inverts the signal is used. Connect **CSPEL (10)** to V_{SS} when passive filter configurations are used.

Frequency Reference

The internal reference oscillator contains all of the passive components required. An appropriate series resonant crystal should be connected between **XTAL1 (5)** and **XTAL2 (6)**. In IBM™-compatible applications this will typically be a 14.31818 MHz crystal, but crystals between 10MHz and 25MHz have been tested and work fine. Maintain short lead lengths between the crystal and the ICS1394, and solder the crystal can to the ground plane to minimize noise pickup. In graphics adapter board applications, it may be desirable to utilize the bus clock. To do this, connect the clock through a .047mF capacitor to **XTAL1 (5)**, and keep the lead length of the capacitor to **XTAL1 (5)** to a minimum to reduce noise susceptibility. This input is internally biased at $V_{DD/2}$ since TTL compatible clocks typically exhibit a V_{OH} of 3.5V.

Capacitively coupling the input restores noise immunity. The ICS1394 is not sensitive to the duty cycle of the bus clock; however, the quality of this signal varies considerably with different motherboard designs. As the quality of this signal is typically outside of the control of the graphics adapter card manufacturer, it is suggested that this signal be buffered on the graphics adapter board. **XTAL2 (6)** should be left open in this configuration. In PS2™ applications it may be desirable to have the **ICS1394** provide the bus clock for the rest of the system. To do this, the **XTAL2 (6)** output should be buffered with a CMOS driver. The ICS1350 would be ideal for this application since it is a CMOS device capable of driving high capacitance loads with minimum clock skew.

Output Circuit Considerations

As the dot clock is usually the highest frequency present in a video graphics system, consideration should be given to EMI. To minimize problems with meeting FCC EMI requirements, the trace which connects **FOUT (9)** and other components in the system should be kept as short as possible. It may be helpful to place a ferrite bead in this signal path to limit the propagation of high order harmonics of this signal. A suitable device would be a Ferroxcube ™ 56-590-65/4B or equivalent. This device should be placed physically close to the **ICS1394**. A 33 to 47 ohm series resistor in this path may be necessary to reduce capacitive loading of the signal and may reduce phase-jitter as well as EMI.

External Frequency Sources

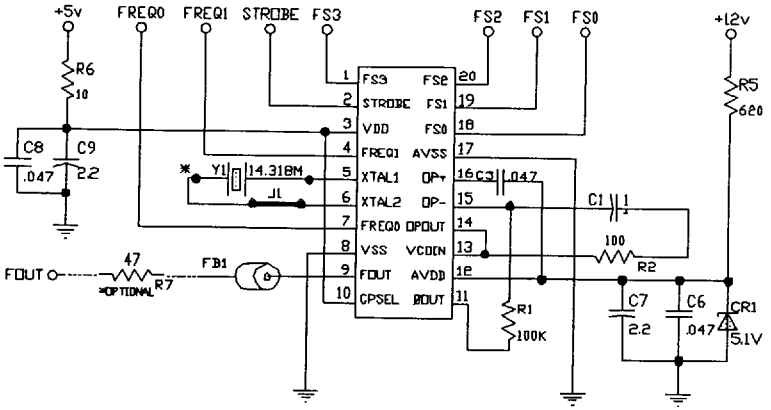
FREQ0 (7) and **FREQ1 (4)**, when enabled, are inputs to an analog multiplexer. When either of these inputs is enabled, signals driving the input will appear at **FOUT (9)** instead of the dot clock output. Internally, the dot clock will remain in lock at the frequency selected by the ROM code. The on-resistance of this multiplexer is typically 100 ohm. **ICS1394** devices with extended frequency capabilities utilize **FREQ1** as the MSB of the frequency select code, and only permit one external input.

Digital Inputs

FS0 (18), FS1 (19), FS2 (20), FS3 (1), and **FS4 /FREQ1 (4),** are the TTL compatible frequency select inputs for the binary code corresponding to the frequency desired. **STROBE** is a factory-programmed option which permits the **ICS1394** to be used in systems which utilize a bus to output frequency select data. **STROBE (2)** transfers these inputs on its positive edge. In addition, **STROBE** causes the output of the charge pump to assume its high impedance state and forces the feedback and reference dividers to a zero count while **STROBE** is high. When **STROBE** is returned low, both feedback and reference dividers are enabled along with the charge pump. The phase comparator will respond correctly to whichever divider clocks out first with a correction pulse in the appropriate direction. The internal power-on-clear signal will force an initial frequency code corresponding to an all zeros input state.

The rate of change in output frequency is dependent on loop filter values and VCO gain. When suggested loop filter values are used, the **ICS1394** will change to a selected new frequency at a rate of approximately 1 MHz/Millisecond.

System Schematic



*** - Replace Y1 with .047 Mfd capacitor and omit J1 for busclock input.**
All capacitor values in microfarads.
All resistor values in ohms.

NOTE: IBM and PS2 are trademarks of International Business Machines Corporation.
Ferroxcube is a trademark of Ferroxcube

ICS1394

Absolute Maximum Ratings

Supply Voltage .....V_{DD} .....-0.5V to +7V
Input Voltage .....V_{IN} .....-0.5V to V_{DD} +0.5V
Output Voltage .....V_{OUT} .....-0.5V to V_{DD} +0.5V
Clamp Diode Current .....I_{IK} & I_{OK} ..... +/-30mA
Output Current per Pin .....I_{OUT} ..... +/-50mA
Storage Temperature .....T_S .....-85 °C to +150 °C
Power Dissipation .....P_D 500mW

Values beyond these ratings may damage the device. This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to > = V_{SS} and < = V_{DD}.

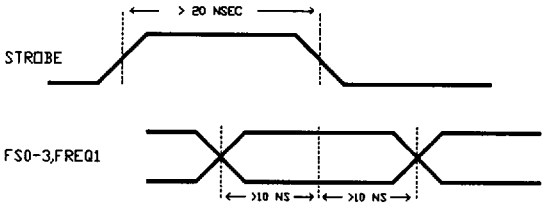
Typical Operating Characteristics

Operating Temperature Range 0 °C to 70 °C

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	DV_{DD}, AV_{DD}	4.5	5.0	5.5	Volts
Digital Supply Current (Fout = 50 MHz, internal xtal oscillator used for Fref.)	DI_{DD}		11	25	Milliamps
Analog Supply Current (F_{out} = 50 MHz)	AI_{DD}		3.2	4.5	Milliamps
Output Impedance	Z_{OUT}		33	100	Ohms
Output Drive Current	I_{SOURCE}, I_{SINK}		4		Milliamps
Op Amp Characteristics					
Output Voltage Swing (Open Circuit)		AV_{SS}		AV_{DD}	Volts
Gain-Bandwidth Product	V_{GBW}		6		MHz
Phase Comparator Characteristics					
Gain Constant	$K\phi$		0.4		Volts/Radian
Bus Timing Setup Time FS0-FS4 relative to STROBE	T_{SETUP}	10			ns
Hold Time **FS0-FS4 relative to STROBE**	T_{HOLD}				ns

ICS1394

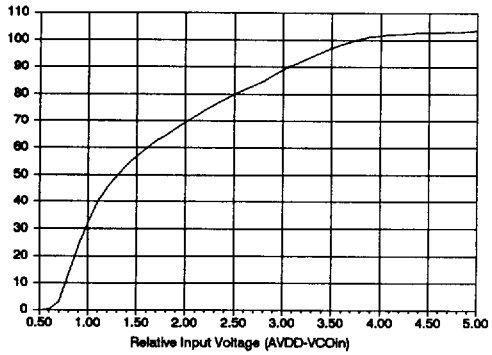
Bus Timing



Typical VCO Characteristics

(High frequency limit is tailored for the Specific Application)

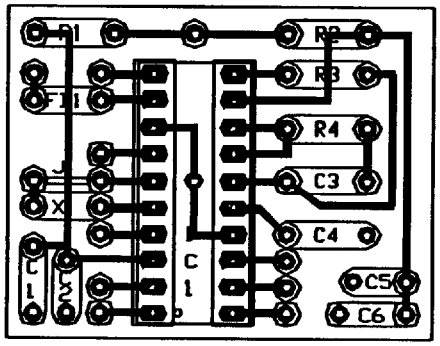
Frequency vs. Voltage



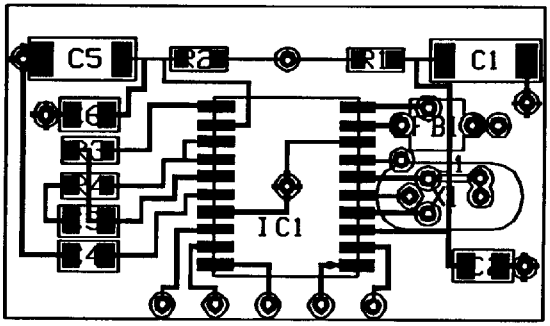
B

Suggested PCB Layouts

DIP Package

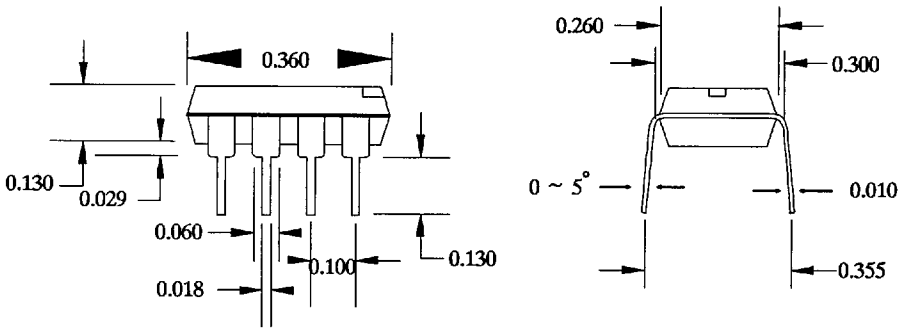


SO Package

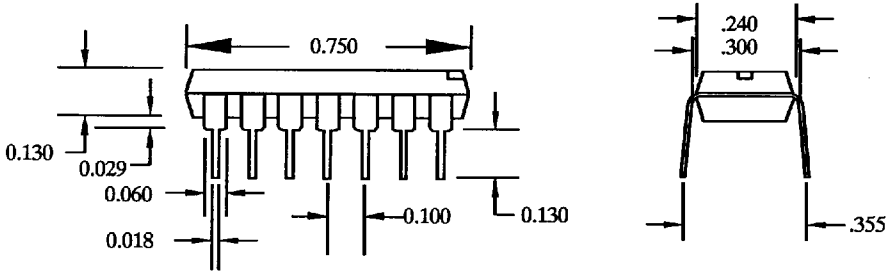


T-90-20

DIP Packages



8 Pin DIP Package



14 Pin DIP Package

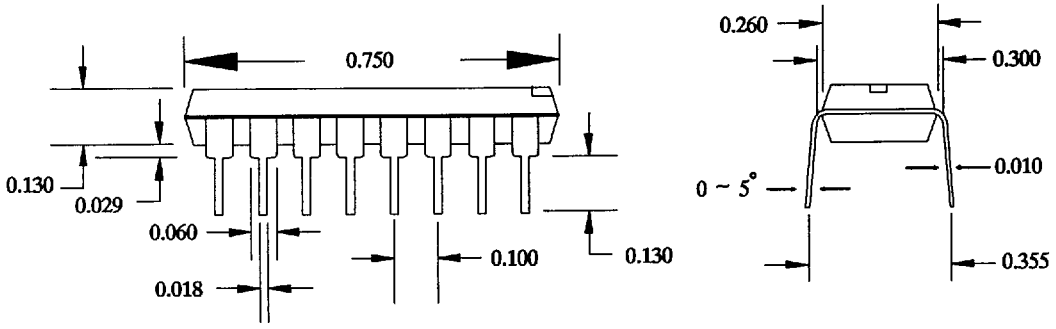
Ordering Information:

All ICS devices in DIP packages carry an "N" designation. See individual data sheets for more specific information.

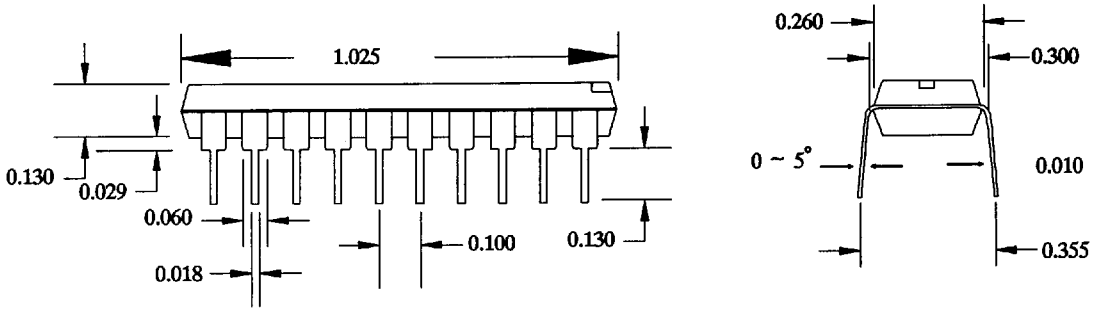
Example: ICSXXXXN

H

DIP Packages



16 Pin DIP Package



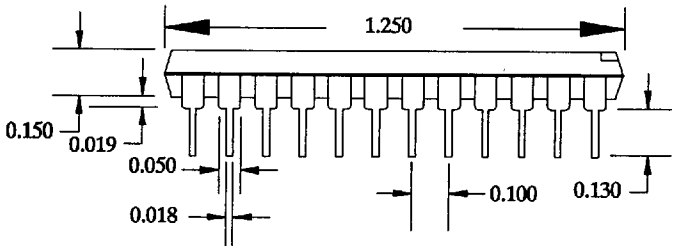
20 Pin DIP Package

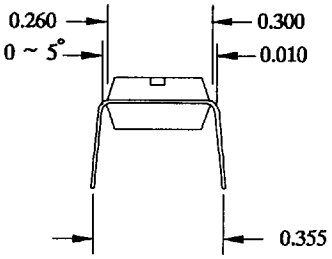
Ordering Information:

All ICS devices in DIP packages carry an "N" designation. See individual data sheets for more specific information.

Example: ICSXXXXN

DIP Packages





24 Pin DIP Package

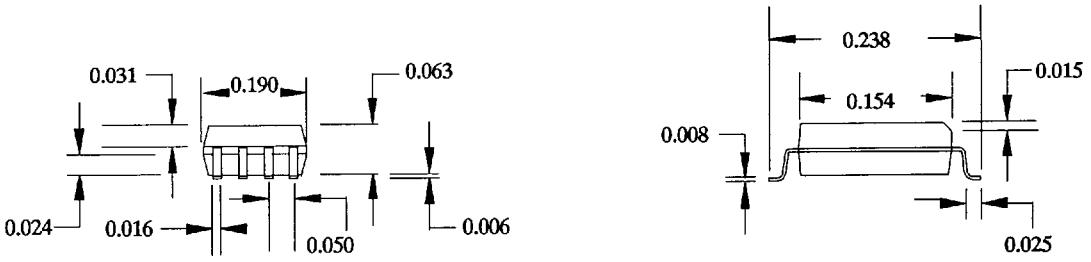
Ordering Information:

All ICS devices in DIP packages carry an "N" designation. See individual data sheets for more specific information.

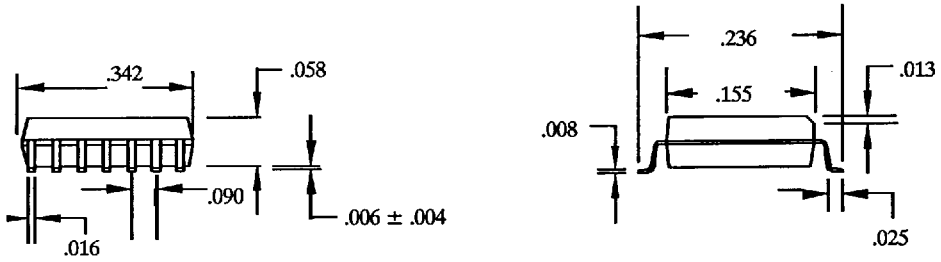
Example: ICSXXXXN

H

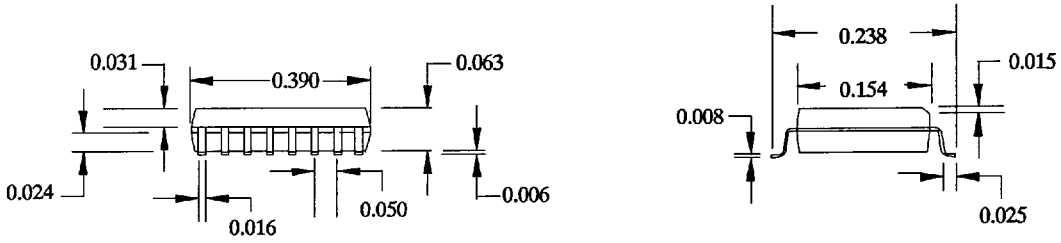
SO Packages



8 Pin SO Package



14 Pin SO Package



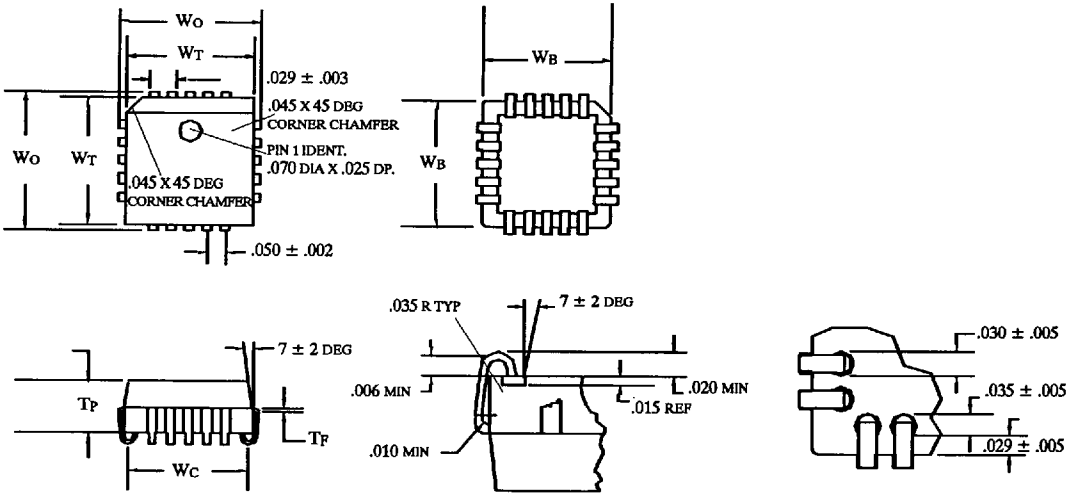
16 Pin SO Package

Ordering Information:

All ICS devices in SO packages carry an "M" designation. See individual data sheets for more specific information.

Example: ICSXXXXM

PLCC Packages



LEAD COUNT	FRAME THICKNESS T_F +/-.0003	PKG. THICKNESS T_P +/-.004	PKG. WIDTH TOP W_T +/-.004	PKG. WIDTH BOTTOM W_B +/-.066	OVERALL PKG. WIDTH W_O +/-.005	CONTACT WIDTH W_O +.010/-.030
20L	0.010	0.152	0.350	0.323	0.390	0.320
28L	0.010	0.152	0.450	0.423	0.490	0.420
44L	0.010	0.152	0.650	0.623	0.690	0.620
52L	0.010	0.152	0.750	0.723	0.790	0.720
68L	0.008	0.150	0.950	0.923	0.990	0.920
84L	0.008	0.150	1.160	1.123	1.190	1.120

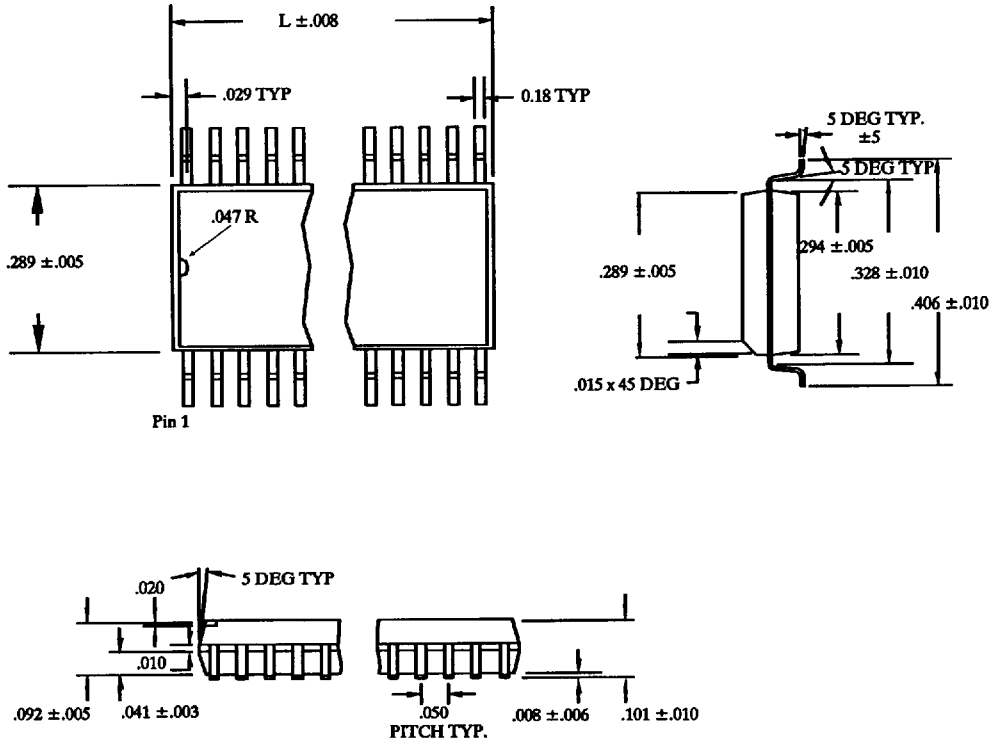
Ordering Information:

All ICS devices in PLCC packages carry a "V" designation. See individual data sheets for more specific information.

Example: ICSXXXXV

H

SOIC Packages



SOIC Packages (wide body)

LEAD COUNT	14L	16L	18L	20L	24L	28L	32L
DIMENSION L	.354	.404	.454	.504	.604	.704	.704

Ordering Information:

All ICS devices in SOIC packages carry an "M" designation. See individual data sheets for more specific information.

Example: ICSXXXXM