CY7C168
CY7C169

CYPRESS SEMICONDUCTOR

4096 x 4 Static R/W RAM

Features

- **Automatic power-down when deselected (7C168)**
- **CMOS for optimum speed/power**
- **High Speed**
  - **— 25 ns t_{AA}**
  - **— 15 ns t_{ACE} (7C169)**
- **Low active power**
  - **— 385 mW (commercial)**
  - **— 385 mW (military)**
- **Low standby power (7C168)**
  - **— 110 mW**
- **TTL compatible inputs and outputs**
- **Capable of withstanding greater than 2000V electrostatic discharge**

Functional Description

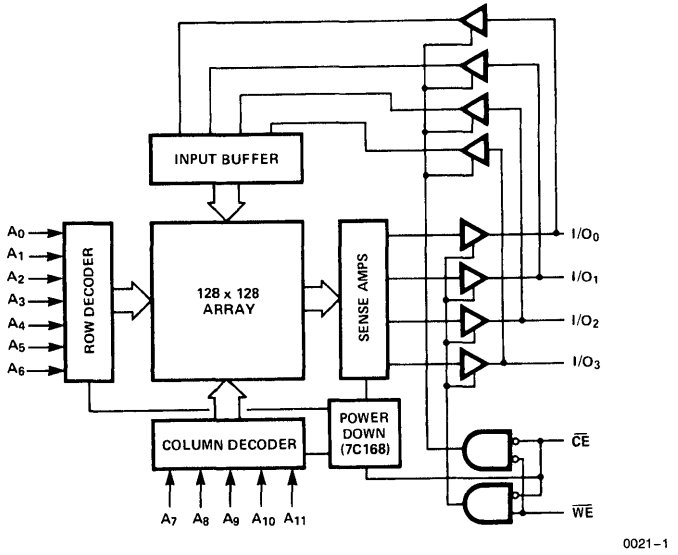
The CY7C168 and CY7C169 are high performance CMOS static RAMs organized as 4096 x 4 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C168 has an automatic power-down feature, reducing the power consumption by 85% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input/output pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{11}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

The I/O pins stay in high impedance state when chip enable ($\overline{CE}$) is HIGH, or write enable ($\overline{WE}$) is LOW.

Logic Block Diagram



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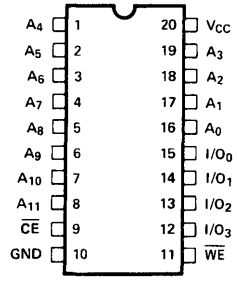
Pin Configurations



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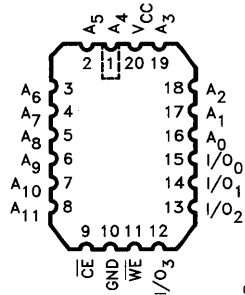

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Selection Guide

		7C168-25	7C168-35	7C168-45	7C169-25	7C169-35	7C169-40
Maximum Access Time (ns)		25	35	45	25	35	40
Maximum Operating Current (mA)	Commercial	90	90	70	90	90	70
	Military		90	70		90	70
Maximum Standby Current (mA)	Commercial	20	20	15			
	Military		20	20			

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 20 to Pin 10)..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... >2001V (Per MIL-STD-883 Method 3015.2)

Latch-up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[1]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		7C168-25, -35 7C169-25, -35		7C168-45 7C169-40		Units
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	−10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−50	+50	−50	−50	μA
I_{OS}	Output Short Circuit Current[2]	V_{CC} = Max., V_{OUT} = GND			−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Commercial		90		70	mA
			Military*		90		70	
I_{SB_1}	Automatic $\overline{CE}$ Power Down Current	Max. V_{CC}, CE ≥ V_{IH}	Commercial		20		15	mA
			Military*		20		20	
I_{SB_2}	Automatic $\overline{CE}$ Power Down Current	Max. V_{CC}, CE ≥ V_{CC} − 0.3V	Commercial		11		11	mA
			Military*		20		20	

*−35 and −45 only

Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	4	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF

Notes:

1. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
2. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
3. Tested on a sample basis.

AC Test Loads and Waveforms

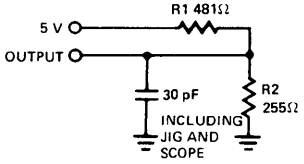


Figure 1a

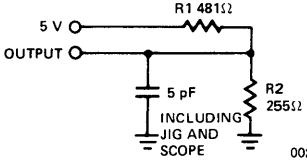


Figure 1b

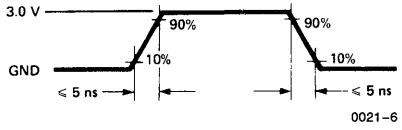
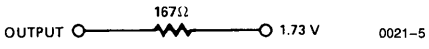


Figure 2

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over Operating Range[4]

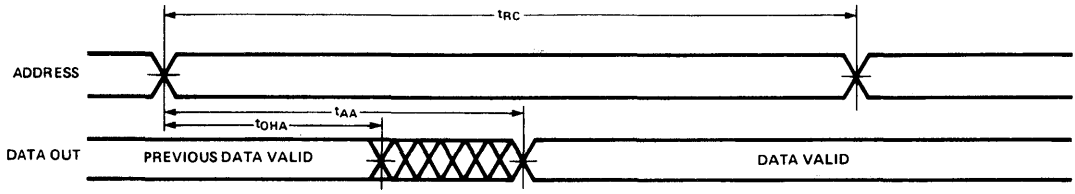
Parameters	Description		7C168-25 7C169-25		7C168-35 7C169-35		7C169-40		7C168-45		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE											
t_{RC}	Read Cycle Time		25		35		40		45		ns
t_{AA}	Address to Data Valid			25		35		40		45	ns
t_{OHA}	Output Hold from Address Change		3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid	7C168		25		35				45	ns
		7C169		15		25		25			ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]		5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[5, 6]			15		20		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power Up (7C168)		0		0				0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down (7C168)			25		25				30	ns
t_{RCS}	Read Command Set-up		0		0		0		0		ns
t_{RCH}	Read Command Hold		0		0		0		0		ns
WRITE CYCLE[7]											
t_{WC}	Write Cycle Time		25		35		40		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End		25		35		30		35		ns
t_{AW}	Address Set-up to Write End		20		30		40		35		ns
t_{HA}	Address Hold from Write End		0		0		0		0		ns
t_{SA}	Address Set-up to Write Start		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width		20		30		35		35		ns
t_{SD}	Data Set-up to Write End		10		15		15		15		ns
t_{HD}	Data Hold from Write End		0		0		3		3		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]		6		6		6		6		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5, 6]			10		15		20		20	ns

Notes:

4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
5. t_{HZCE} and t_{HZWE} are tested with C_L = 5 pF as in *Figure 1b*. Transition is measured ± 500 mV from steady state voltage.
6. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices. These parameters are sampled and not 100% tested.
7. The internal write time of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. $\overline{WE}$ is high for read cycle.
9. Device is continuously selected, $\overline{CE}$ = V_{IL}.
10. Address valid prior to or coincident with $\overline{CE}$ transition low.

Switching Waveforms

Read Cycle No. 1 (Notes 8, 9)



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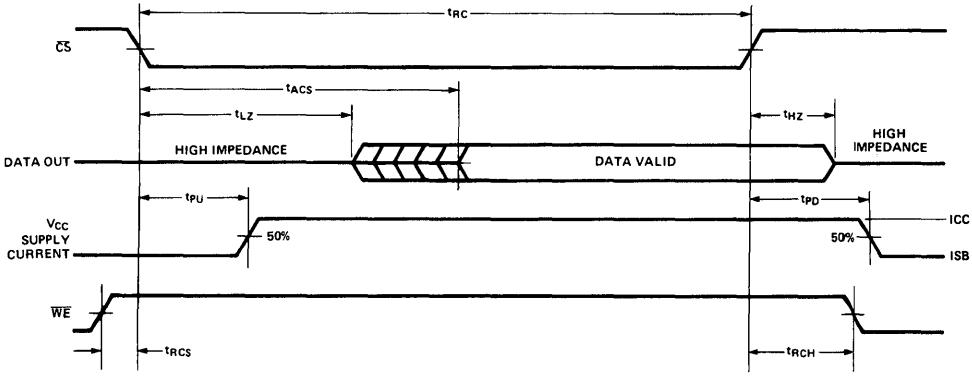
Switching Waveforms (Continued)

Read Cycle (Notes 8, 10)



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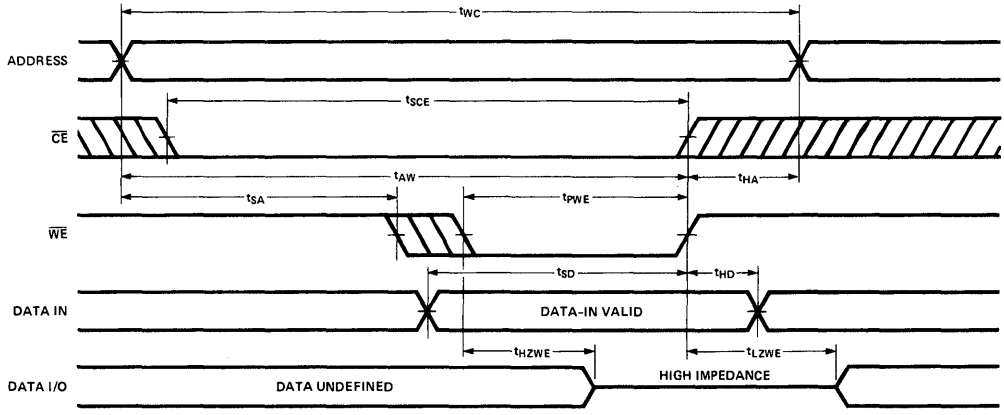
Write Cycle No. 1 ($\overline{WE}$ Controlled) (Note 7)



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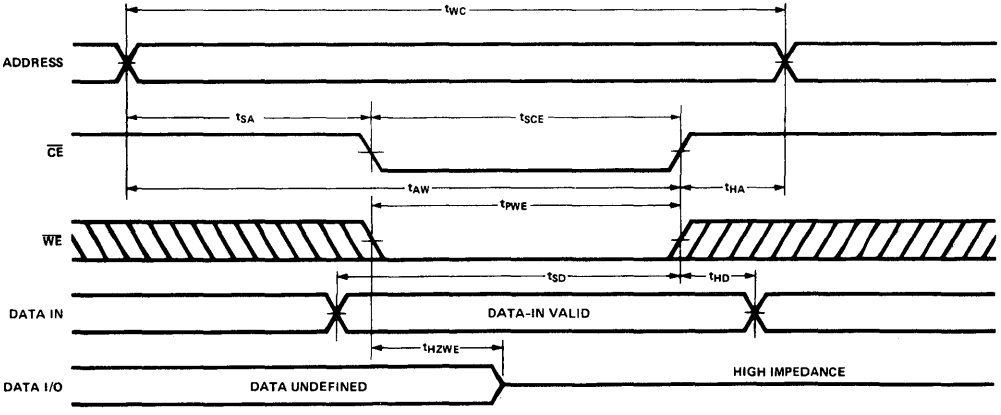
Write Cycle No. 2 ($\overline{CE}$ Controlled) (Note 7)



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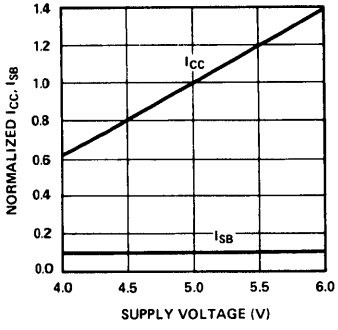
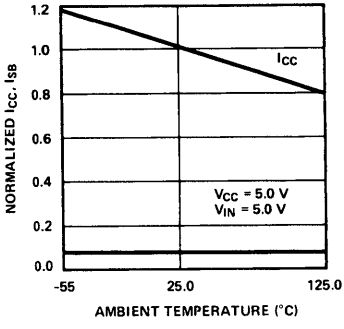
Note: If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

Typical DC and AC Characteristics

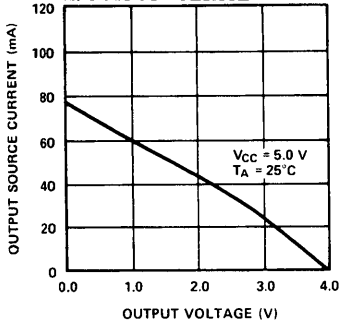
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



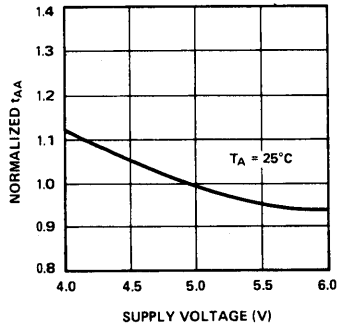
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



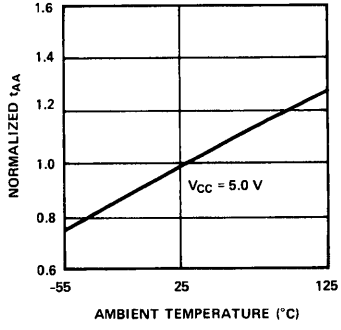
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



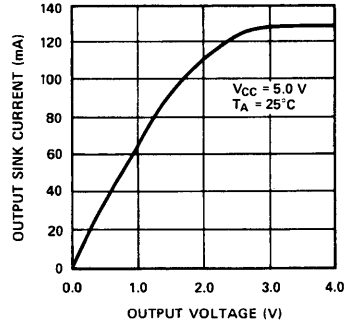
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



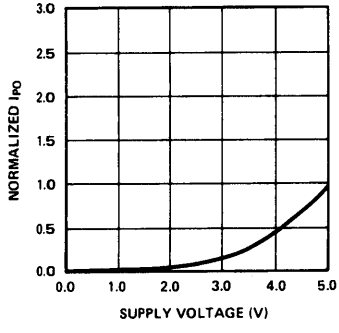
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



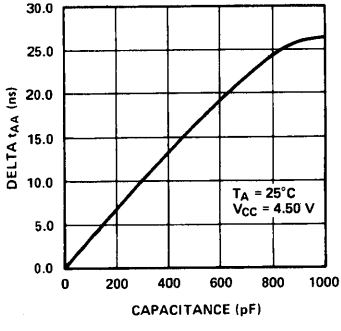
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



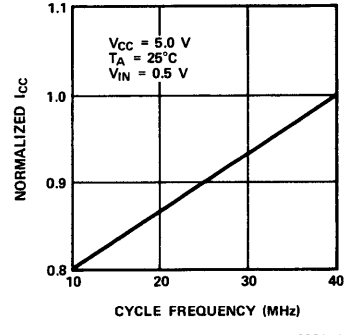
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED ICC vs. CYCLE TIME



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Ordering Information

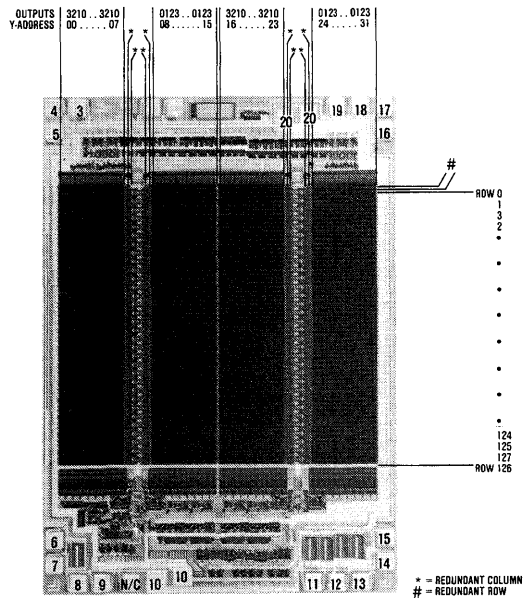
Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C168-25PC	P5	Commercial
	CY7C168-25DC	D6	
	CY7C168-25LC	L51	
35	CY7C168-35PC	P5	Commercial
	CY7C168-35DC	D6	
	CY7C168-35LC	L51	
	CY7C168-35DMB	D6	Military
	CY7C168-35LMB	L51	
45	CY7C168-45PC	P5	Commercial
	CY7C168-45DC	D6	
	CY7C168-45LC	L51	
	CY7C168-45DMB	D6	Military
	CY7C168-45LMB	L51	

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C169-25PC	P5	Commercial
	CY7C169-25DC	D6	
	CY7C169-25LC	L51	
35	CY7C169-35PC	P5	Commercial
	CY7C169-35DC	D6	
	CY7C169-35LC	L51	
	CY7C169-35DMB	D6	Military
	CY7C169-35LMB	L51	
40	CY7C169-40PC	P5	Commercial
	CY7C169-40DC	D6	
	CY7C169-40LC	L51	
	CY7C169-40DMB	D6	Military
	CY7C169-40LMB	L51	

Address Designators

Address Name	Address Function	Pin Number
A_0	X_0	16
A_1	X_3	17
A_2	X_4	18
A_3	X_1	19
A_4	X_2	1
A_5	X_5	2
A_6	X_6	3
A_7	Y_3	4
A_8	Y_4	5
A_9	Y_0	6
A_{10}	Y_1	7
A_{11}	Y_2	8

Bit Map



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