



CYPRESS SEMICONDUCTOR

T-46-23-12

CY7C128

2048 x 8 Static R/W RAM

Features

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed
— 35 ns
- Low active power
— 660 mW (commercial)
— 825 mW (military)
- Low standby power
— 110 mW
- TTL-compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

Functional Description

The CY7C128 is a high-performance CMOS static RAM organized as 2048 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable (CE), and active LOW output enable (OE) and three-state drivers. The CY7C128 has an automatic power-down feature, reducing the power consumption by 83% when deselected.

Writing to the device is accomplished when the chip enable (CE) and write enable (WE) inputs are both LOW. Data on the eight I/O pins (I/O₀ through I/O₇) is written into the memory location specified on the address pins (A₀ through A₁₀).

Reading the device is accomplished by taking chip enable (CE) and output enable (OE) LOW while write enable (WE) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the eight I/O pins.

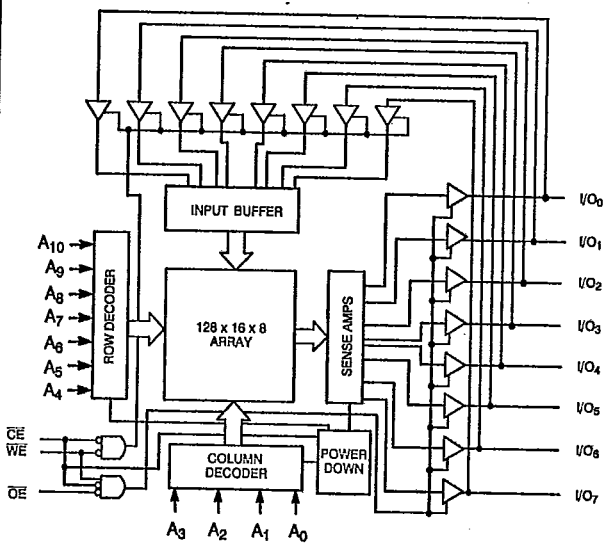
The I/O pins remain in high-impedance state when chip enable (CE) or output enable (OE) is HIGH or write enable (WE) is low.

The 7C128 utilizes a die coat to ensure alpha immunity.

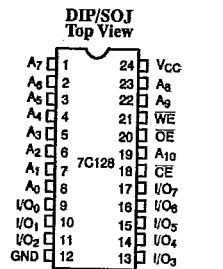


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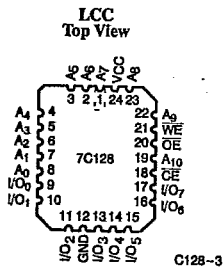
Logic Block Diagram



Pin Configurations



C128-2



C128-3

C128-1

Selection Guide

		7C128-35	7C128-45	7C128-55
Maximum Access Time (ns)		35	45	55
Maximum Operating Current (mA)	Commercial	120	120	90
	Military		130	100
Maximum Standby Current (mA)	Commercial	20	20	20
	Military		20	20



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature - 65°C to + 150°C
- Ambient Temperature with Power Applied - 55°C to + 125°C
- Supply Voltage to Ground Potential (Pin 24 to Pin 12) - 0.5V to + 7.0V
- DC Voltage Applied to Outputs in High Z State - 0.5V to + 7.0V
- DC Input Voltage - 3.0V to + 7.0V
- Output Current into Outputs (LOW) 20 mA

- Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)
- Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military ^[1]	- 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[2]

Parameters	Description	Test Conditions	7C128		Units	
			Min.	Max.		
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 4.0 mA	2.4		V	
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4	V	
V _{IH}	Input HIGH Voltage		2.0	V _{CC}	V	
V _{IL}	Input LOW Voltage		-3.0	0.8	V	
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	µA	
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-40	+40	µA	
I _{OS}	Output Short Circuit Current ^[3]	V _{CC} = Max., V _{OUT} = GND		-300	mA	
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA	Com'l	35, 45	120	mA
				55	90	
			Mil	45	130	
				55	100	
I _{SB}	Automatic CE Power-Down Current	Max. V _{CC} , CE ≥ V _{IH}	Com'l		20	mA
			Mil		20	

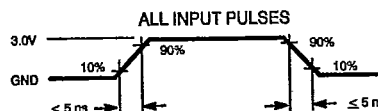
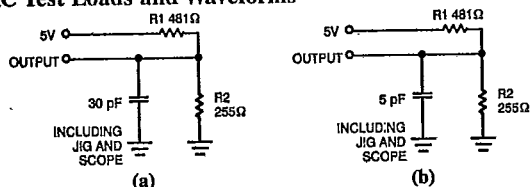
Capacitance^[4]

Parameters	Description	Test Conditions	Max.	Units
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THEVENIN EQUIVALENT
 OUTPUT — 167Ω — 1.73V

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C128-5



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Switching Characteristics Over the Operating Range^{2, 5]}

Parameters	Description	7C128-35		7C128-45		7C128-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	35		45		55		ns
t _{AA}	Address to Data Valid		35		45		55	ns
t _{OHA}	Data Hold from Address Change	5		5		5		ns
t _{ACE}	\overline{CE} LOW to Data Valid		35		45		55	ns
t _{DOE}	\overline{OE} LOW to Data Valid		15		20		25	ns
t _{LZOE}	\overline{OE} LOW to Low Z	0		0		0		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[6]		15		15		20	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[7]	5		5		5		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[6, 7]		15		20		20	ns
t _{PU}	\overline{CE} LOW to Power-Up	0		0		0		ns
t _{PD}	\overline{CE} HIGH to Power-Down		20		25		25	ns
WRITE CYCLE^[8]								
t _{WC}	Write Cycle Time	35		45		55		ns
t _{SCE}	\overline{CE} LOW to Write End	30		40		50		ns
t _{AW}	Address Set-Up to Write End	30		40		50		ns
t _{HA}	Address Hold from Write End	0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		ns
t _{PWE}	\overline{WE} Pulse Width	20		20		25		ns
t _{SD}	Data Set-Up to Write End	15		20		25		ns
t _{HD}	Data Hold from Write End	0		0		0		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[6]		15		15		20	ns
t _{LZWE}	\overline{WE} HIGH to Low Z	0		0		0		ns



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Notes:

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

- \overline{WE} is HIGH for read cycle.
- Device is continuously selected. \overline{OE} , \overline{CE} = V_{IL}.
- Address valid prior to or coincident with \overline{CE} transition LOW.
- Data I/O pins enter high-impedance state, as shown, when \overline{OE} is held LOW during write.
- If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.

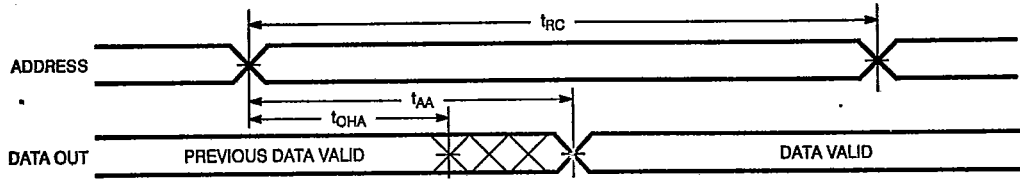


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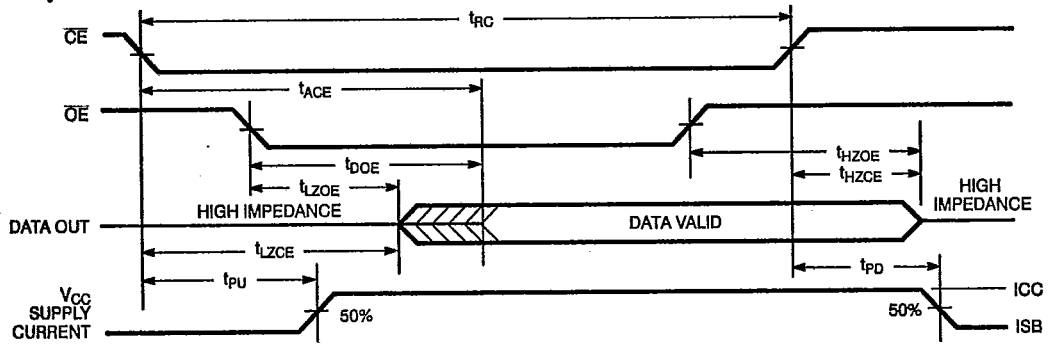
Switching Waveforms

Read Cycle No. 1^[9, 10]



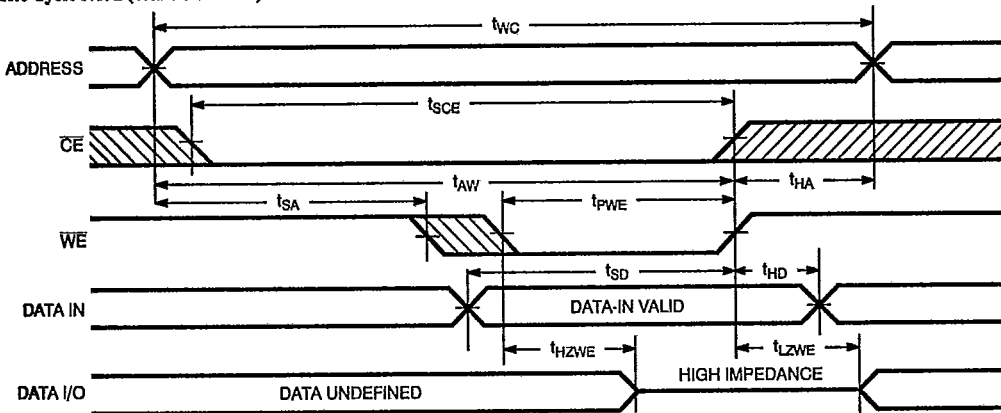
C128-6

Read Cycle No. 2^[9, 11]



C128-7

Write Cycle No. 1 (\overline{WE} Controlled)^[9, 12]



C128-8

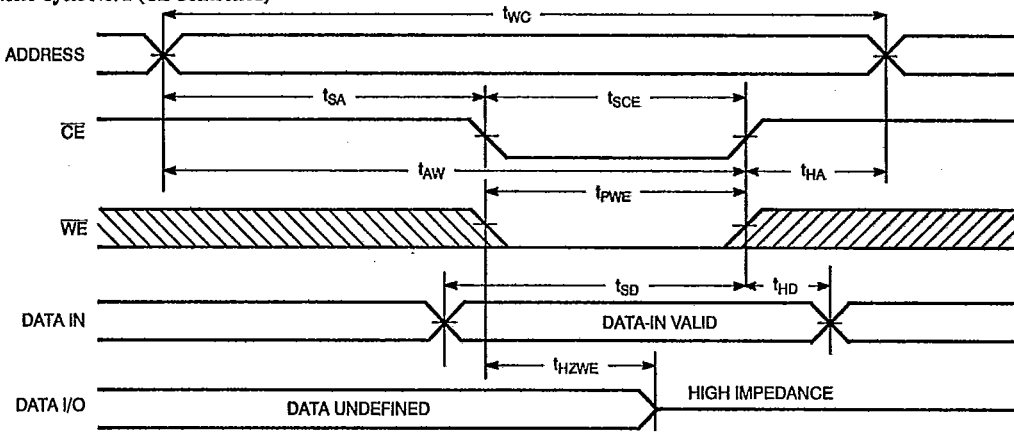


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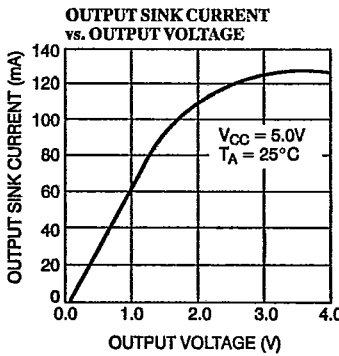
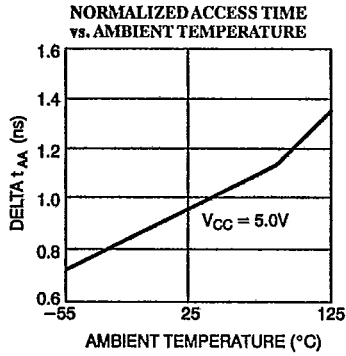
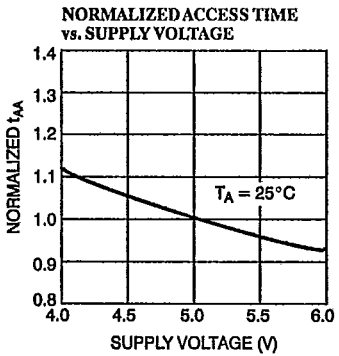
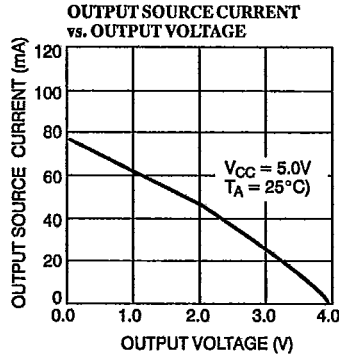
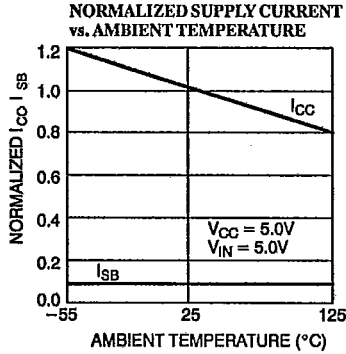
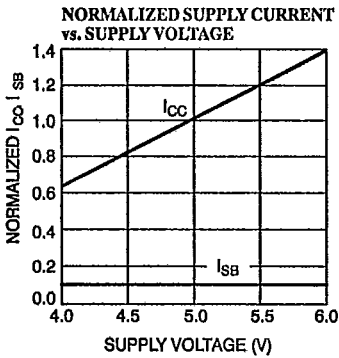
Switching Waveforms (continued)

Write Cycle No. 2 (CE Controlled) [9, 12, 13]



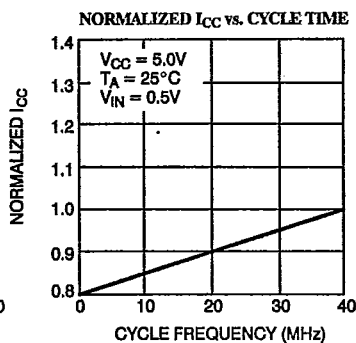
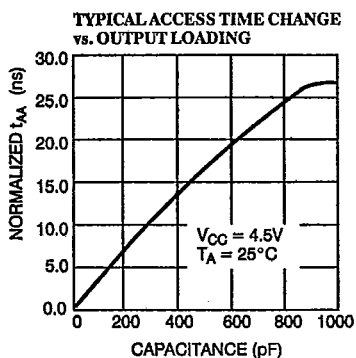
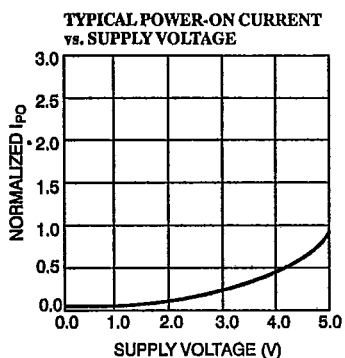
C128-9

Typical DC and AC Characteristics





Typical DC and AC Characteristics (continued)



Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY7C128-35PC	P13	Commercial
	CY7C128-35VC	V13	
	CY7C128-35DC	D14	
	CY7C128-35LC	L53	
45	CY7C128-45PC	P13	Commercial
	CY7C128-45VC	V13	
	CY7C128-45DC	D14	
	CY7C128-45LC	L53	
	CY7C128-45DMB	D14	Military
	CY7C128-45LMB	L53	
	CY7C128-45KMB	K73	
55	CY7C128-55PC	P13	Commercial
	CY7C128-55VC	V13	
	CY7C128-55DC	D14	
	CY7C128-55LC	L53	
	CY7C128-55DMB	D14	Military
	CY7C128-55LMB	L53	
	CY7C128-55KMB	K73	



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MILITARY SPECIFICATIONS**Group A Subgroup Testing****DC Characteristics**

Parameters	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL Max.}	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB}	1, 2, 3



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Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{OHA}	7, 8, 9, 10, 11
t _{ACE}	7, 8, 9, 10, 11
t _{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCE}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11

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