



8,192 x 8 Static RAM

Features

- BiCMOS for optimum speed/power
- High speed
– 12 ns
- Low active power
– 600 mW
- Low standby power
– 200 mW
- TTL-compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

Functional Description

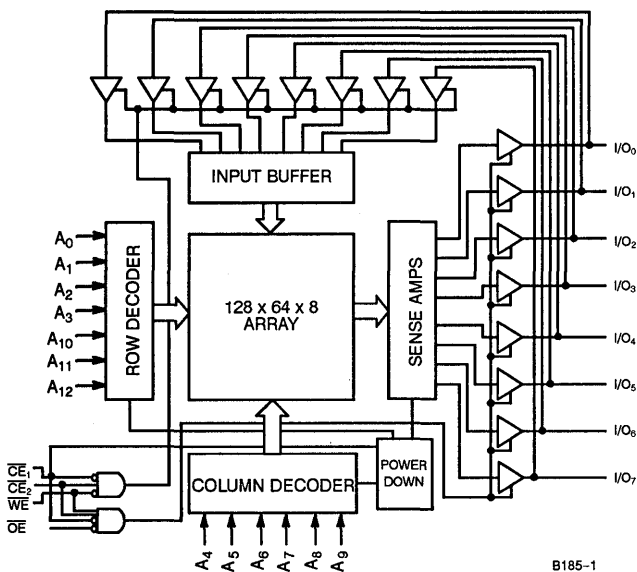
The CY7B185 and CY7B186 are high-performance BiCMOS static RAMs organized as 8,192 words by 8 bits. These RAMs are developed by Aspen Semiconductor Corporation, a subsidiary of Cypress Semiconductor. Easy memory expansion is provided by an active LOW chip enable (\overline{CE}_1), an active HIGH chip enable (CE_2), and active LOW output enable (\overline{OE}) and three-state drivers. Both devices have a power-down feature (\overline{CE}_1) that reduces the power consumption by 67% when deselected. The CY7B185 is in the space saving 300-mil-wide DIP package and leadless chip carrier. The CY7B186 is in the standard 600-mil-wide package.

An active LOW write enable signal (\overline{WE}) controls the writing/reading operation of the memory. When \overline{CE}_1 and \overline{WE} inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by (A_0 through A_{12}). Reading the device is accomplished by selecting the device and enabling the outputs, \overline{CE}_1 and \overline{OE} active LOW, CE_2 active HIGH, while \overline{WE} remains HIGH. Under these conditions, the contents of the location addressed by the information on the address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable (\overline{WE}) is HIGH.

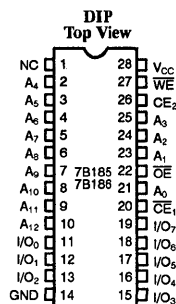
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Logic Block Diagram

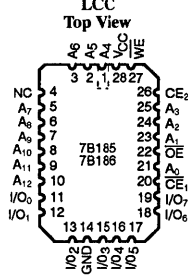


B185-1

Pin Configurations



B185-2



B185-3

Selection Guide

	7B185-12 7B186-12	7B185-15 7B186-15
Maximum Access Time (ns)	12	15
Maximum Operating Current (mA)	Commercial	140
	Military	145
Maximum Standby Current (mA)	Commercial	40
	Military	50

Maximum Rating

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	-0.5V to +7.0V
Input Voltage ^[1]	-3.0V to +7.0V
Output Current into Outputs (Low)	20 mA

Static Discharge Voltage	> 2001V (Per MIL-STD-883 Method 3015)
Latch-Up Current	> 200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Military ^[2]	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range ^[3]

Parameters	Description	Test Conditions	7B185-12 7B186-12		7B185-15 7B186-15		Units	
			Min.	Max.	Min.	Max.		
V _{OH}	Output HIGH Voltage	V _{CC} = Min.	I _{OH} = -4.0 mA	Com'l	2.4		2.4	V
			I _{OH} = -2.0 mA	Mil	2.4		2.4	
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA			0.4		0.4	V
V _{IH}	Input HIGH Level		2.2	V _{CC}	2.2	V _{CC}	V _{CC}	V
V _{IL}	Input LOW Voltage ^[1]		-0.5	0.8	-0.5	0.8	V	
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	-10	+10	μA	
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-10	+10	-10	+10	μA	
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA f = f max.	Com'l		140		135	mA
			Mil				145	mA
I _{SB}	\overline{CE}_1 Power-Down Current	$\overline{CE}_1 \geq V_{IH}$	Com'l		40		40	mA
			Mil				50	mA

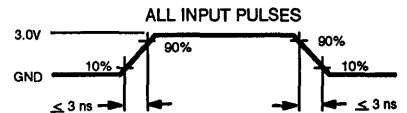
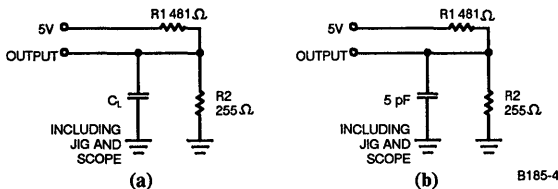
Capacitance^[4]

Parameters	Description	Test Conditions	Max. ^[5]	Units
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz	5	pF
C _{OUT}	Output Capacitance	V _{CC} = 5.0V	7	pF

Notes:

- V_{IL} (min.) = -3.0V for pulse width < 20 ns.
- T_A is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Tested initially and after any design or process changes that may affect these parameters.
- For all packages except Cerdip (D16, D22), which has maximums of C_{IN} = 8 pF, C_{OUT} = 9 pF.

AC Test Loads and Waveforms



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Switching Characteristics Over the Operating Range ^[3, 6]

Parameters	Description	7B185-12 7B186-12		7B185-15 7B186-15		Units
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	12		15		ns
t_{AA}	Address to Data Valid		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		ns
t_{ACE1}	\overline{CE}_1 LOW to Data Valid		12		15	ns
t_{ACE2}	CE_2 HIGH to Data Valid		12		15	ns
t_{DOE}	\overline{OE} LOW to Data Valid		8		10	ns
t_{LZOE}	\overline{OE} LOW to Low Z	2		3		ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[7]		8		8	ns
t_{LZCE1}	\overline{CE}_1 LOW to Low Z ^[8]	3		3		ns
t_{LZCE2}	CE_2 HIGH to Low Z ^[8]	3		3		ns
t_{HZCE}	\overline{CE}_1 HIGH to High Z ^[6, 7] CE_2 LOW to High Z		7		8	ns
WRITE CYCLE ^[9]						
t_{WC}	Write Cycle Time	12		15		ns
t_{SCE1}	\overline{CE}_1 LOW to Write End	8		10		ns
t_{SCE2}	CE_2 HIGH to Write End	8		10		ns
t_{AW}	Address Set-Up to Write End	8		10		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	\overline{WE} Pulse Width	8		10		ns
t_{SD}	Data Set-Up to Write End	6.5		8		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	\overline{WE} LOW to High Z ^[6]		7		7	ns
t_{LZWE}	\overline{WE} HIGH to Low Z	3		3		ns

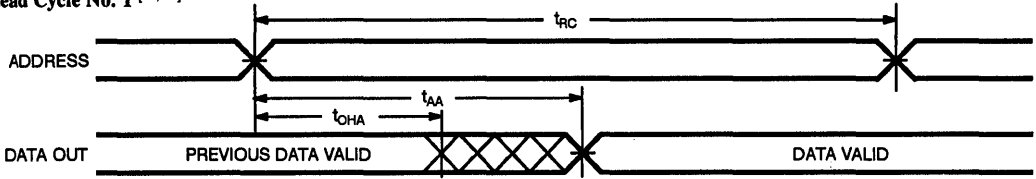
Notes:

- Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} , and $C_L = 20$ pF.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
- The internal write time of the memory is defined by the overlap of \overline{CE}_1 LOW, CE_2 HIGH, and \overline{WE} LOW. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write. All three signals must be active to initiate a write, and either signal can terminate a write by going inactive.

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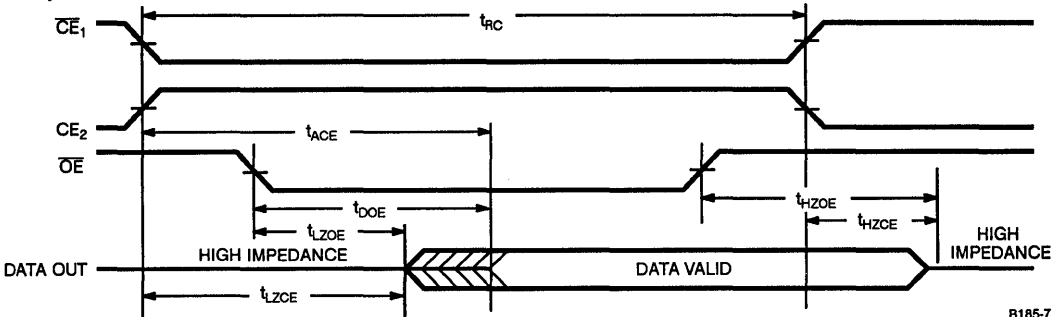
Switching Waveforms

Read Cycle No. 1 [10, 11]



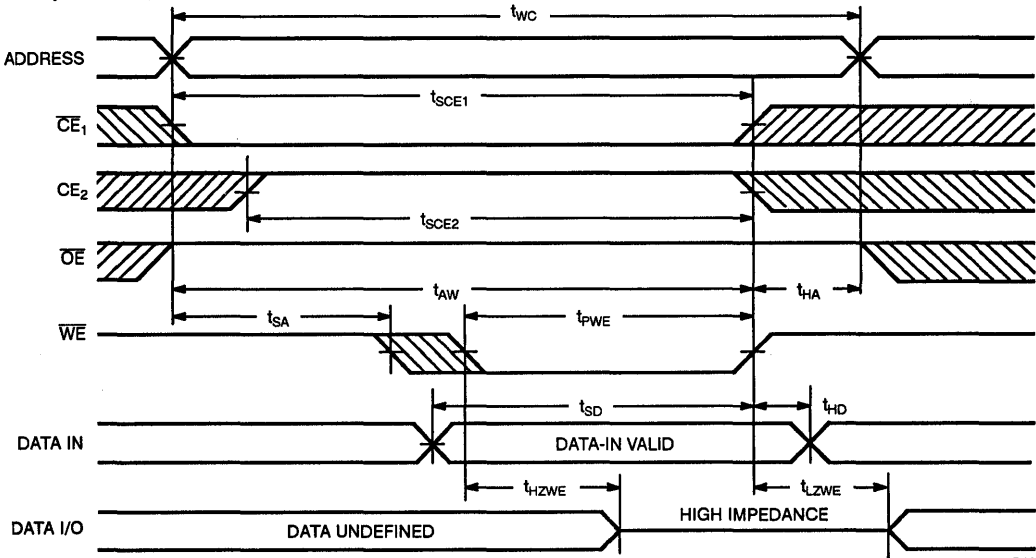
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Read Cycle No. 2 [10, 12]



B185-7

Write Cycle No. 1 (\overline{WE} Controlled) [8, 13]



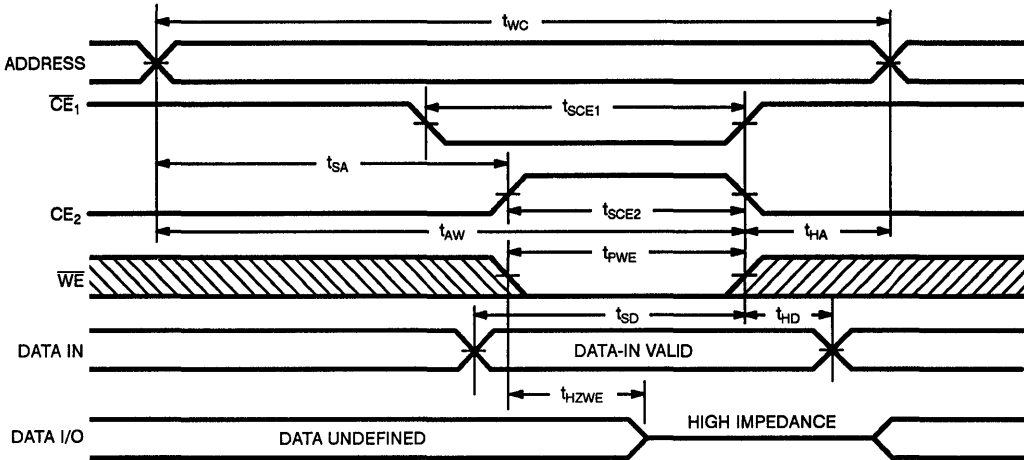
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Notes:

10. Device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$. $CE_2 = V_{IH}$.
11. Address valid prior to or coincident with \overline{CE} transition LOW.
12. \overline{WE} is HIGH for read cycle.

13. Data I/O is HIGH impedance if $\overline{OE} = V_{IH}$.

14. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)
Write Cycle No. 2 (\overline{CE} Controlled) ^[8, 12, 14]


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Truth Table

\overline{CE}_1	\overline{CE}_2	\overline{WE}	\overline{OE}	Inputs/Outputs	Mode
H	X	X	X	High Z	Deselect/Power-Down
L	L	X	X	High Z	Deselect
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
12	CY7B185-12PC	P21	Commercial
	CY7B185-12VC	V21	
	CY7B185-12DC	D22	
15	CY7B185-15PC	P21	Commercial
	CY7B185-15VC	V21	
	CY7B185-15DC	D22	
	CY7B185-15DMB	D22	Military
	CY7B185-15LMB	L54	

Speed (ns)	Ordering Code	Package Type	Operating Range
12	CY7B186-12PC	P15	Commercial
15	CY7B186-15PC	P15	Commercial
	CY7B186-15DMB	D16	Military