Bt471
Bt476
Bt478

80 MHz
256-Word Color Palette
Personal System/2®
RAMDAC™

4

Distinguishing Features

- Personal System/2® Compatibility
- 80, 66, 50, 35 MHz Operation
- Triple 6-bit or 8-bit D/A Converters
- 256-Word Color Palette RAM
- RS-343A-Compatible Outputs
- 15 Overlay Registers (Bt471/478)
- Sync on All Three Channels (Bt471/478)
- Programmable Pedestal (Bt471/478)
- External Voltage or Current Reference
- Standard MPU Interface
- +5 V CMOS Monolithic Construction
- 44-pin PLCC or 28-pin DIP Package

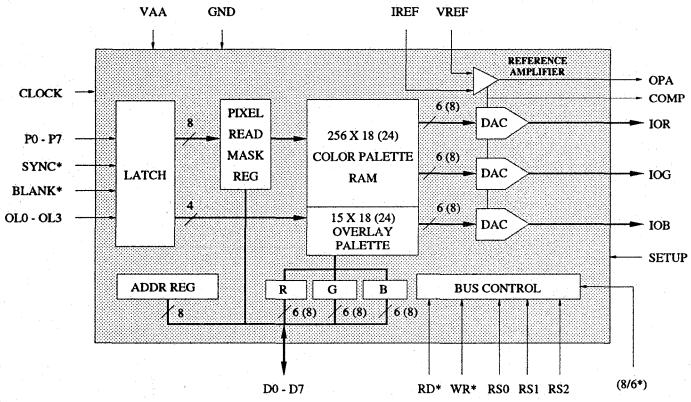
Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Instrumentation
- Desktop Publishing

Related Products

- Bt473, Bt477, Bt479
- Bt474, Bt475

Functional Block Diagram



Product Description

The Bt471, 476, and 478 are pin-compatible and software-compatible RAMDACs designed specifically for Personal System/2®-compatible color graphics. The Bt476 is also available in a 28-pin DIP package that is pin compatible with the IMS® G176.

The Bt471 has a 256 x 18 color lookup table with triple 6-bit video D/A converters. The Bt478 has a 256 x 24 color lookup table with triple 8-bit video D/A converters. It may be configured for either 6-bit or 8-bit D/A converter operation. The Bt476 is similar to the Bt471 but has no overlays, no programmable setup, and no sync information on the analog outputs.

Additional features on the Bt471 and Bt478 include 15 overlay registers that provide, for example, overlaying cursors, grids, menus, and EGA emulation. Also supported is sync generation on all three channels, a programmable pedestal (0 or 7.5 IRE), and use of either an external voltage or current reference.

The Bt471/476/478 generates RS-343A-compatible video signals into a doubly-terminated 75 Ω load.

Note: "Personal System/2®" and "PS/2®" are registered trademarks of IBM. "IMS®" is a registered trademark of Inmos Limited.

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MPU Interface

As illustrated in the functional block diagram, the Bt471/476/478 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers.

The RS0–RS2 select inputs specify whether the MPU is accessing the address register, color palette RAM, overlay registers, or read mask register, as shown in Table 1. The 8-bit address register is used to address the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

Writing Color Palette RAM Data

To write color data, the MPU loads the address register (RAM write mode) with the address of the color palette RAM location to be modified. The MPU performs three successive write cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM. After the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word (18-bit word for the Bt471/476) and written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R, G, B write cycles until the entire block has been written. (See Figure 7 in the Timing Waveforms section.)

Reading Color Palette RAM Data

To read color palette RAM data, the MPU loads the address register (RAM read mode) with the address of the color palette RAM location to be read. The contents of the color palette RAM at the specified address are copied into the RGB registers, and the address register is incremented to the next RAM location. The MPU performs three successive read cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM. Following the blue read cycle, the contents of the color palette RAM at the address specified by the address register are copied into the RGB registers, and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R,G,B read cycles until the entire block has been read.

Writing Overlay Color Data

To write overlay color data, the MPU loads the address register (overlay write mode) with the address of the overlay location to be modified. The MPU performs three successive write cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select the overlay registers. After the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word (18-bit word for the Bt471/476) and written to the overlay location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R, G, B write cycles until the entire block has been written.

RS2	RS1	RS0	Addressed by MPU
0	0	0	address register (RAM write mode)
0	1	1	address register (RAM read mode)
0	0	1	color palette RAM
0	1	0	pixel read mask register
1	0	0	address register (overlay write mode)
1	1	1	address register (overlay read mode)
1	0	1	overlay registers
1	1	0	reserved

Table 1. Control Input Truth Table.

Reading Overlay Color Data

To read overlay color data, the MPU loads the address register (overlay read mode) with the address of the overlay location to be read. The contents of the overlay register at the specified address are copied into the RGB registers, and the address register is incremented to the next overlay location. The MPU performs three successive read cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select the overlay registers. Following the blue read cycle, the contents of the overlay location at the address specified by the address register are copied into the RGB registers, and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R, G, B read cycles until the entire block has been read.

Additional Information

When the MPU is accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF. While accessing the overlay color registers, the 4 most significant bits of the address register (ADDR4–7) are ignored.

The MPU interface operates asynchronously to the pixel clock. Data transfers that occur between the color palette RAM/overlay registers and the color registers (R, G, and B in the block diagram) are synchronized by internal logic and take place in the period between MPU accesses. Occasional accesses to the color palette RAM can be made without noticeable disturbance on the display screen; however, operations requiring frequent access to the color palette (such as block fills of the color palette) should take place during the blanking interval.

To keep track of the red, green, and blue read/write cycles, the address register has 2 additional bits(ADDRa and ADDRb) that count modulo three, as shown in Table 2. They are reset to zero when the MPU writes to the address register and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other 8 bits of the address register are incremented following a blue read or write cycle. (ADDR0–7) are accessible to the MPU and are used to address color palette RAM locations and overlay registers, as indicated in Table 2. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

	Value	RS2	RS1	RS0	Addressed by MPU
ADDRa, b (counts modulo 3)	00 01 10				red value green value blue value
ADDR0–7 (counts binary)	$00 - $FF xxxx 0000 xxxx 0001 : xxxx 1111	0 1 1 : 1	0 0 0 : 0	1 1 1 : 1	color palette RAM reserved overlay color 1 : overlay color 15

Table 2. Address Register (ADDR) Operation.

Bt471/476 Data Bus Interface

Color data is contained on the lower 6 bits of the data bus. D0 is the LSB and D5 is the MSB of color data. When color data is written, D6 and D7 are ignored. During color read cycles, D6 and D7 will be logical zeros.

Bt478 Data Bus Interface

On the Bt478, the 8/6* control input is used to specify whether the MPU is reading and writing 8 bits (8/6* = logical one) or 6 bits (8/6* = logical zero) of color information each cycle.

For 8-bit operation, D0 is the LSB and D7 is the MSB of color data.

For 6-bit operation (and when the Bt471/476 is used), color data is contained on the lower 6 bits of the data bus. D0 is the LSB and D5 is the MSB of color data. When color data is written, D6 and D7 are ignored. During color read cycles, D6 and D7 will be logical zeros.

When the Bt478 is in the 6-bit mode, its full-scale output current will be about 1.5-percent lower than when it is in the 8-bit mode. This is because the 2 LSBs of each 8-bit DAC are logical zeros in the 6-bit mode.

Frame Buffer Interface

The P0–P7 and OL0–OL3 inputs are used to address the color palette RAM and overlay registers, as shown in Table 3.

The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bitwise logically ANDed with the P0–P7 inputs. Bit D0 of the pixel read mask register corresponds to pixel input P0. The addressed location provides 24 bits (18 bits for the Bt471/476) of color information to the three D/A converters. For proper operation, the pixel read mask register must be initialized by the user after power-up.

The SYNC* and BLANK* inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs. This produces the specific output levels required for video applications, as illustrated in Figures 1, 2, and 3. Tables 4, 5, and 6 detail how the SYNC* and BLANK* inputs modify the output levels.

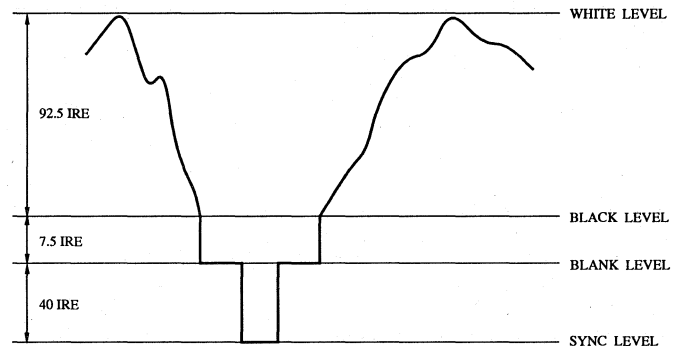
The SETUP input is used to specify whether a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = VAA) blanking pedestal is to be used. The Bt476 generates only a 0 IRE blanking pedestal (Figures 2 and 3).

The analog outputs of the Bt471/476/478 can directly drive a 37.5 Ω load, such as a doubly-terminated 75 Ω coaxial cable.

OL0–OL3	P0–P7	Addressed by frame buffer
$0	$00	color palette RAM location $00
$0	$01	color palette RAM location $01
:	:	:
$0	$FF	color palette RAM location $FF
$1	$xx	overlay color 1
:	$xx	:
$F	$xx	overlay color 15

Table 3. Pixel and Overlay Control Truth Table (Pixel Read Mask Register = $FF).

BT471 / 478 W/O SYNC		BT471 / 478 WITH SYNC	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly-terminated load and SETUP = 7.5 IRE. VREF = 1.235 V and RSET = 147 Ω. RS-343A levels and tolerances are assumed on all levels.

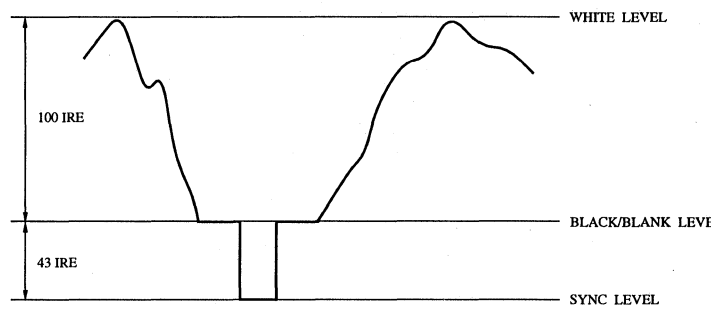
Figure 1. RS-343A Composite Video Output Waveforms (SETUP = 7.5 IRE).

Description	Bt471/478 Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	1	1	$FF
DATA	data + 9.05	1	1	data
DATA - SYNC	data + 1.44	0	1	data
BLACK	9.05	1	1	$00
BLACK - SYNC	1.44	0	1	$00
BLANK	7.62	1	0	$xx
SYNC	0	0	0	$xx

Note: 75 Ω doubly-terminated load and SETUP = 7.5 IRE. VREF = 1.235 V and RSET = 147 Ω.

Table 4. RS-343A Video Output Truth Table (SETUP = 7.5 IRE).

BT476 OR BT471 / 478 W/O SYNC		BT471 / 478 WITH SYNC	
MA	V	MA	V
17.62	0.660	25.24	0.950
0.00	0.000	7.62	0.286
0.00	0.000	0.00	0.000



Note: 75 Ω doubly-terminated load and SETUP = 0 IRE. VREF = 1.235 V and RSET = 147 Ω. RS-343A levels and tolerances are assumed on all levels.

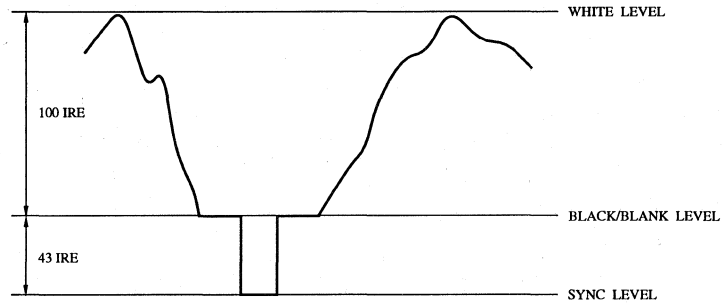
Figure 2. RS-343A Composite Video Output Waveforms. (SETUP = 0 IRE)

Description	Bt476 Iout (mA)	Bt471/478 Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	17.62	25.24	1	1	$FF
DATA	data	data + 7.62	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	0	7.62	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	0	7.62	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 75 Ω doubly-terminated load and SETUP = 0 IRE. VREF = 1.235 V and RSET = 147 Ω.

Table 5. RS-343A Video Output Truth Table (SETUP = 0 IRE).

NO SYNC		SYNC	
MA	V	MA	V
14.25	0.713	20.36	1.018
0.00	0.000	6.11	0.305
0.00	0.000	0.00	0.000



Note: 50 Ω load and SETUP = 0 IRE. VREF = 1.235 V and RSET = 182 Ω. PS/2 levels and tolerances are assumed on all levels.

Figure 3. PS/2 Composite Video Output Waveforms (SETUP = 0 IRE).

Description	Sync Disabled	Sync Enabled	SYNC*	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	14.25	20.36	1	1	$FF
DATA	data	data + 6.11	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	0	6.11	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	0	6.11	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 50 Ω load and SETUP = 0 IRE. VREF = 1.235 V and RSET = 182 Ω.

Table 6. PS/2 Video Output Truth Table (SETUP = 0 IRE).

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the analog outputs to the blanking level, as specified in Tables 4, 5 and 6. BLANK* is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SETUP	Setup control input (TTL compatible). SETUP is used to specify either a 0 IRE (logical zero) or 7.5 IRE (logical one) blanking pedestal. This pin should not be left floating.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the analog outputs (see Figures 1, 2, and 3). SYNC* does not override any other control or data input, as shown in Tables 4, 5, and 6; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK. If sync information is not required on the video outputs, SYNC* should be connected to GND.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0–P7, OL0–OL3, SYNC*, and BLANK* inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer to avoid reflection-induced jitter. Clock Interfacing in the PC Board Layout Considerations section contains detailed layout suggestions.
P0–P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which 1 of the 256 entries in the color palette RAM is to be used to provide color information. P0–P7 are latched on the rising edge of CLOCK. P0 is the LSB. Unused inputs should be connected to GND.
OL0–OL3	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information, as shown in Table 3. When the overlay palette is accessed, the P0–P7 inputs are ignored. They are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
COMP	Compensation pin. If an external voltage reference is used (Figure 4 in the PC Board Layout Considerations section), this pin should be connected to OPA. If an external current reference is used (Figure 5 in the PC Board Layout Considerations section), this pin should be connected to IREF. A 0.1 µF ceramic capacitor must be used to bypass this pin to VAA. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. *The PC Board Layout Considerations section contains critical layout criteria.*
VREF	Voltage reference input. If an external voltage reference is used (Figure 4), it must supply this input with a 1.2 V (typical) reference. IF an external current reference is used (Figure 5), this pin should be left floating; however, the bypass capacitor must still be connected. A 0.1 µF ceramic capacitor is used to decouple this input to GND, as shown in Figure 4. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
OPA	Reference amplifier output. If an external voltage reference is used (Figure 4), this pin must be connected to COMP. When an external current reference is used (Figure 5), this pin should be left floating.
IOR, IOG, IOB	Red, green, and blue current outputs. These high-impedance current sources can directly drive a doubly-terminated 75 Ω coaxial cable (Figures 4, 5, and 6 in the PC Board Layout Considerations section).
VAA	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup.
GND	Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup.

Pin Descriptions *(continued)*

<table>
<tr><th>Pin Name</th><th>Description</th></tr>
<tr><td>IREF</td><td>Full-scale adjust control. The IRE relationships in Figures 1, 2, and 3 are maintained, regardless of the full-scale output current.

When an external voltage reference is used (Figure 4), a resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal. The relationship between RSET and the full-scale output current on each output is:

RSET (Ω) = K * 1,000 * VREF (V) / Iout (mA)

K is defined in the table below. It is recommended that a 147 Ω RSET resistor be used for doubly-terminated 75 Ω loads (i.e., RS-343A applications). For PS/2® applications (i.e., 0.7 V into 50 Ω with no sync), a 182 Ω RSET resistor is recommended.

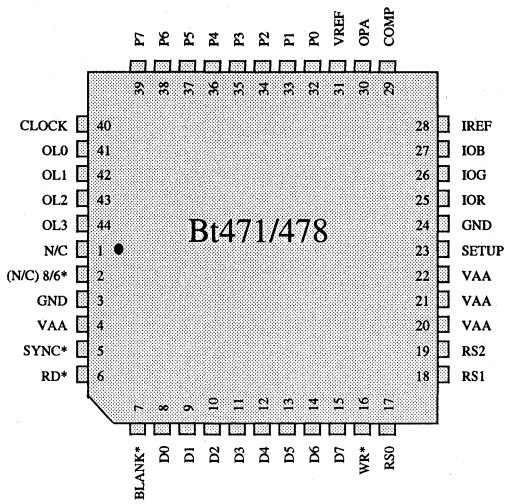
When an external current reference is used (Figures 5 and 6), the relationship between IREF and the full-scale output current on each output is:

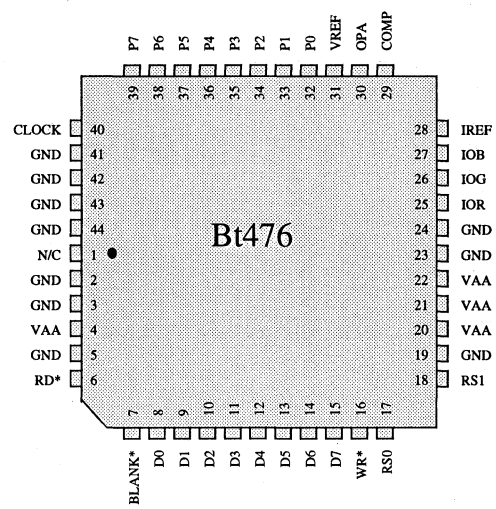
IREF (mA) = Iout (mA) / K

<table>
<tr><th>Part</th><th>Mode</th><th>Pedestal</th><th>K (with sync)</th><th>K (without sync)</th></tr>
<tr><td>Bt478</td><td>6-bit</td><td>7.5 IRE</td><td>3.170</td><td>2.26</td></tr>
<tr><td></td><td>8-bit</td><td>7.5 IRE</td><td>3.195</td><td>2.28</td></tr>
<tr><td></td><td>6-bit</td><td>0 IRE</td><td>3.000</td><td>2.10</td></tr>
<tr><td></td><td>8-bit</td><td>0 IRE</td><td>3.025</td><td>2.12</td></tr>
<tr><td>Bt471</td><td>(6-bit)</td><td>7.5 IRE</td><td>3.170</td><td>2.26</td></tr>
<tr><td></td><td></td><td>0 IRE</td><td>3.000</td><td>2.10</td></tr>
<tr><td>Bt476</td><td>(6-bit)</td><td>0 IRE</td><td>3.000</td><td>2.10</td></tr>
</table>
</td></tr>
<tr><td>WR*</td><td>Write control input (TTL compatible). D0–D7 data is latched on the rising edge of WR*, and RS0–RS2 are latched on the falling edge of WR* during MPU write operations. RD* and WR* should not be asserted simultaneously. MPU Control Signal Interfacing in the PC Board Layout Considerations section contains detailed layout suggestions.</td></tr>
<tr><td>RD*</td><td>Read control input (TTL compatible). To read data from the device, RD* must be a logical zero. RS0–RS2 are latched on the falling edge of RD* during MPU read operations. RD* and WR* should not be asserted simultaneously. MPU Control Signal Interfacing contains detailed layout suggestions.</td></tr>
<tr><td>RS0, RS1, RS2</td><td>Register select inputs (TTL compatible). RS0–RS2 specify the type of read or write operation being performed, as detailed in Tables 1 and 2. MPU Control Signal Interfacing contains detailed layout suggestions.</td></tr>
<tr><td>D0 - D7</td><td>Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.</td></tr>
<tr><td>8/6*</td><td>8-bit/6-bit select input (TTL compatible). This bit specifies whether the MPU is reading and writing 8 bits (logical one) or 6 bits (logical zero) of color information each cycle. For 8-bit operation, D7 is the most significant data bit during color read/write cycles. For 6-bit operation, D5 is the most significant data bit during color read/write cycles. (D6 and D7 are ignored during color write cycles and logical zeros during color read cycles.) This pin should be connected to GND when the Bt476 is used.</td></tr>
</table>

Pin Descriptions *(continued)*

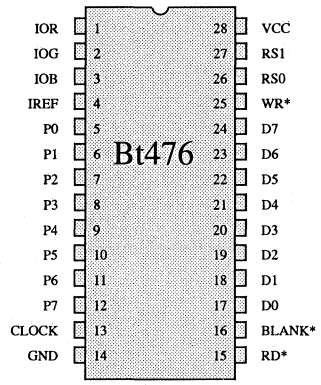
44-Pin Plastic J-Lead (PLCC)





Note 1: Names in parentheses are pin names for the Bt471.
Note 2: N/C pins may be left unconnected with no effect on the performance of the Bt471/476/478.

28-Pin DIP



PC Board Layout Considerations

PC Board Considerations

For optimum performance of the Bt471, Bt476, and Bt478, proper CMOS RAMDAC layout techniques should be studied in the Bt451/7/8 Evaluation Module Operation and Measurements, Application Note (AN-16), before PC board layout is begun. This application note can be found in Brooktree's *Applications Handbook.*

The layout should be optimized for lowest noise on the Bt471, Bt476, and Bt478 power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended, with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for power and ground.

Component Placement

Components should be placed as close as possible to the associated RAMDAC pin. Whenever possible, components should be placed so traces can be connected point to point.

The optimum layout enables the Bt471, Bt476, and Bt478 to be located as close as possible to the power supply connector and the video output connector.

Ground Planes

For optimum performance, a common digital and analog ground plane is recommended.

Power Planes

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt471, Bt476, and Bt478 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figures 4, 5, and 6. This bead should be located within 3 inches of the Bt471, Bt476, and Bt478. The bead provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, and the shortest possible leads (consistent with reliable operation) should be used to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor, decoupling each of the two groups of VAA pins to GND. For operation above 75 MHz, a 0.1 µF capacitor in parallel with a 0.01 µF chip capacitor is recommended. The capacitors should be placed as close as possible to the device VAA and GND pins and connected with short, wide traces.

The 10 µF capacitor shown in Figures 4, 5, and 6 is for low-frequency power supply ripple; the 0.1 µF capacitors are for high-frequency power supply noise rejection.

When a linear regulator is used, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used, and the switching frequency is close to the raster scan frequency. About 10 percent of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically with a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance. Lead inductance degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help.

VREF Decoupling

A 0.1 µF ceramic capacitor should be used to decouple this input to GND.

Digital Signal Interconnect

The digital inputs to the Bt471, Bt476, and Bt478 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane or analog output signals.

Most of the noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time (refer to Brooktree Application Notes AN-11 and AN-12). Line termination or line-length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without use of termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω). The RS-select inputs and RD*/WR* lines must be verified for proper levels with no ringing, undershoot, or overshoot. Ringing on these lines can cause improper operation.

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

Clock Interfacing

The Bt471, Bt476, and Bt478 require a pixel clock with monotonic clock edges for proper operation. Impedance mismatch on the pixel clock line will induce reflections on the pixel clock, which may cause erratic operation.

The Pixel Clock Pulse Width High Time and Pixel Clock Pulse Width Low Time minimum specifications (see the AC Characteristics section) must not be violated, or erratic operation can occur.

The pixel clock line must be terminated to prevent impedance mismatch. A series termination of 33–68 Ω placed at the pixel clock driver may be used, or a parallel termination may be used at the pixel clock input to the RAMDAC. A parallel termination of 220 Ω to VCC and 330 Ω to ground will provide a Thevenin equivalent of a 110 Ω termination, which is normally sufficient to absorb reflections. The series or parallel resistor values should be adjusted to provide the optimum clock signal fidelity.

MPU Control Signal Interfacing

The Bt471, Bt476, and Bt478 use the RD*, WR*, and RS lines to determine which MPU accesses will take place. Glitches or ringing on any of these lines may cause improper MPU operation. When a VGA controller with edge rate control is used on these lines, a series termination is not necessary. In non-VGA controller application or in applications where the MPU control signals are daisy chained, a series termination, pull-down resistors, or additional capacitance to ground should be used to prevent glitches that could cause improper MPU accesses.

Analog Signal Interconnect

The Bt471, Bt476, and Bt478 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should not overlay the analog power plane.

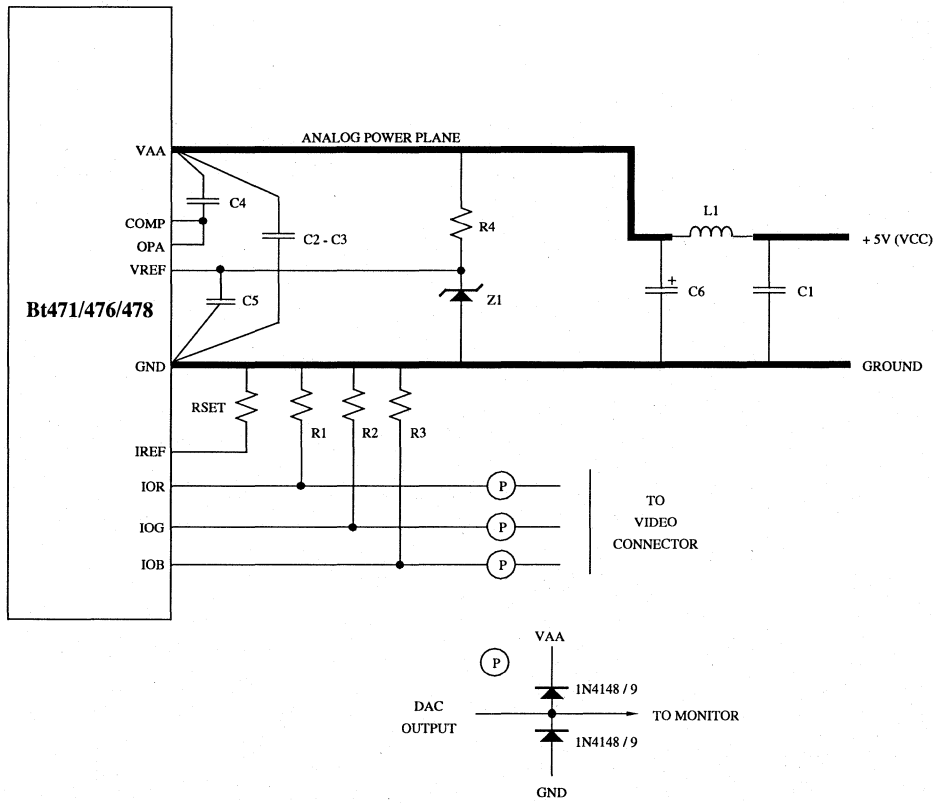
For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the Bt471, Bt476, and Bt478 to minimize reflections. Unused analog outputs should be connected to GND.

Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt471, Bt476, and Bt478 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching AC-coupled monitors.

The diode protection circuit shown in Figures 4, 5, and 6 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

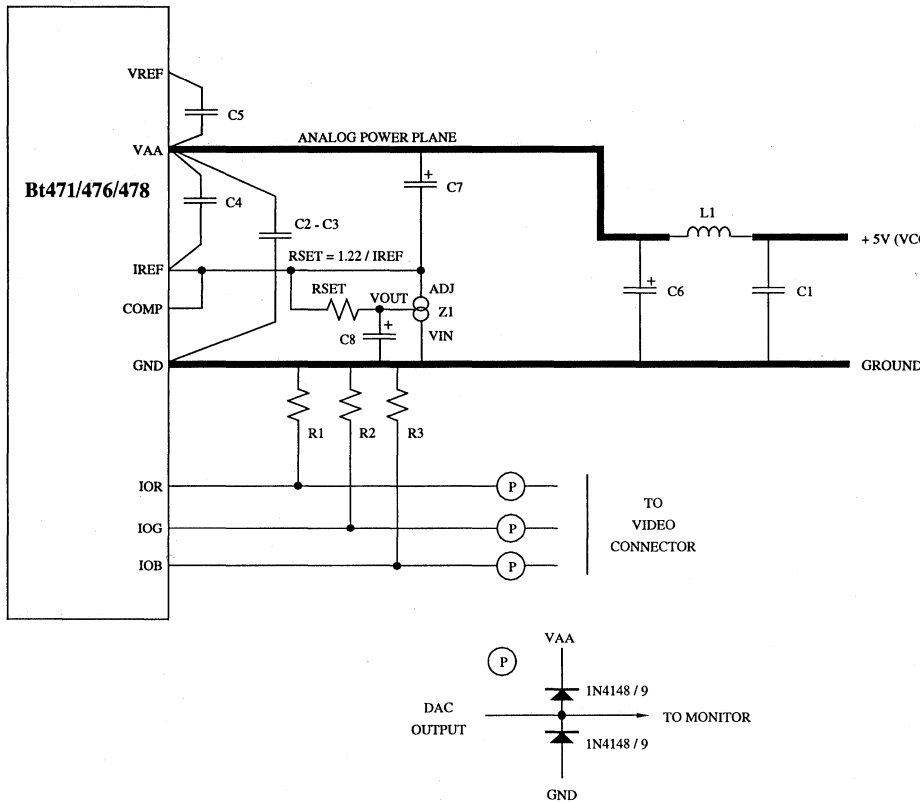


Note: Each set of VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1 kΩ 5% resistor	—
RSET	1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt471/476/478.

Figure 4. Typical Connection Diagram and Parts List for the 44-Pin PLCC (External Voltage Reference).



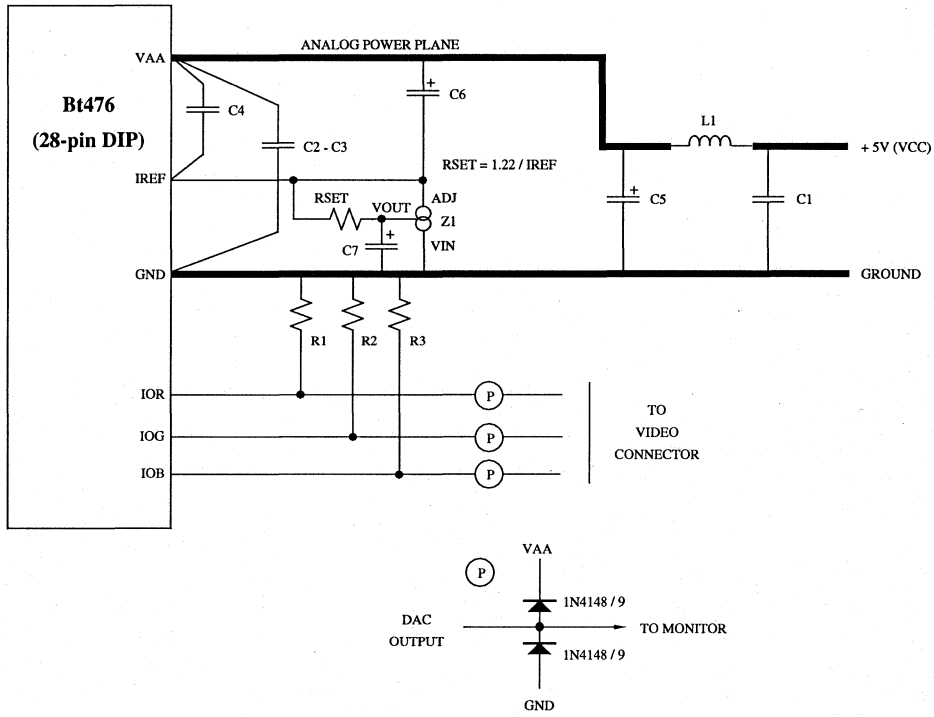
Note: Each set of VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1 - C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
C7, C8	1 µF capacitor	Mallory CSR13G105KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
Z1	adjustable regulator	National Semiconductor LM337LZ
RSET	1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt471/476/478.

Figure 5. Typical Connection Diagram and Parts List for the 44-Pin PLCC (External Current Reference).

PC Board Layout Considerations *(continued)*



Note: Each set of VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1–C4	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C5	10 µF capacitor	Mallory CSR13G106KM
C6, C7	1 µF capacitor	Mallory CSR13G105KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
Z1	adjustable regulator	National Semiconductor LM337LZ
RSET	1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt476.

Figure 6. Typical Connection Diagram and Parts List for the 28-Pin DIP (External Current Reference).

Application Information

Using Multiple Devices

When multiple RAMDACs are used, each RAMDAC should share a common power plane with one ferrite bead. In addition, a single reference may drive multiple devices. However, isolation resistors are recommended to reduce color channel crosstalk.

Higher performance is obtained if each RAMDAC has its own reference. This may further reduce the amount of color channel crosstalk and color palette interaction.

Each RAMDAC must still have its own RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and reference capacitors.

Reference Selection

An external voltage reference provides about 10 times the power supply rejection on the analog outputs than does an external current reference.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. DAC power decoupling networks with large time constants should be avoided. They could delay VAA power to the device. Ferrite beads must be used only for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA				
80, 66 MHz Parts		4.75	5.00	5.25	V
50, 35 MHz Parts		4.5	5.00	5.5	V
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ω
Voltage Reference Configuration					
Reference Voltage	VREF	1.14	1.235	1.26	V
Current Reference Configuration					
IREF Current	IREF				
Standard RS-343A		–3	–8.39	–10	mA
PS/2 Compatible		–3	–8.88	–10	mA

4

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	V
Voltage on any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)					
Bt478		8	8	8	Bits
Bt471/476		6	6	6	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL				
Bt478				±1	LSB
Bt476				±1/2	LSB
Bt471				±1/4	LSB
Differential Linearity Error	DL				
Bt478				±1	LSB
Bt476				±1/2	LSB
Bt471				±1/4	LSB
Gray-Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN			7	pF
Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
3-State Current	IOZ			50	µA
Output Capacitance	CDOUT			7	pF

See test conditions on next page.

DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Gray-Scale Current Range				20	mA
Output Current (Standard RS-343A)					
White Level Relative to Black (Note 1)		16.74	17.62	18.50	mA
Black Level Relative to Blank					
Bt471/478					
SETUP = 7.5 IRE		0.95	1.44	1.90	mA
SETUP = 0 IRE		0	5	50	µA
Bt476		0	0	0	µA
Blank Level					
Bt471/478		6.29	7.62	8.96	mA
Bt476		0	5	50	µA
Sync Level (Bt471/478 only)		0	5	50	µA
LSB Size					
Bt478 (8/6* = logical one)			69.1		µA
Bt471/476			279.68		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	–0.5		+1.5	V
Output Impedance	RAOUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT			30	pF
Voltage Reference Input Current	IVREF		10		µA
Power Supply Rejection Ratio (Note 2) (COMP = 0.1 µF, f = 1 kHz)	PSRR			0.5	% / % ΔVAA

Test conditions to generate RS-343A standard video signals (unless otherwise specified): "Recommended Operating Conditions" with external voltage reference, RSET = 147 Ω, VREF = 1.235 V, SETUP = 7.5 IRE, and 8/6* = logical one. For 28-pin DIP version of the Bt476, IREF = –8.39 mA. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Since the Bt471 and Bt476 have 6-bit DACs (and the Bt478 is in the 6-bit mode), the output levels are approximately 1.5-percent lower than these values.

Note 2: Guaranteed by characterization, not tested.

Analog Output Levels — PS/2® Compatibility

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Black		18.00	18.65	20.00	mA
Black Level Relative to Blank					
Bt471/478					
SETUP = 7.5 IRE		1.01	1.51	2.0	mA
SETUP = 0 IRE		0	5	50	µA
Bt476		0	5	50	µA
Blank Level					
Bt471/478		6.6	8	9.4	mA
Bt476		0	5	50	µA
Sync Level (Bt471/478 only)		0	5	50	µA

Test conditions to generate PS/2®-compatible video signals (unless otherwise specified): "Recommended Operating Conditions" with external voltage reference, RSET = 140 Ω, VREF = 1.235 V, SETUP = 7.5 IRE, and 8/6* = logical one. For 28-pin DIP version of the Bt476, IREF = –8.88 mA.

AC Characteristics

Parameter	Symbol	80 MHz Devices Min	80 MHz Devices Typ	80 MHz Devices Max	66 MHz Devices Min	66 MHz Devices Typ	66 MHz Devices Max	Units
Clock Rate	Fmax			80			66	MHz
RS0–RS2 Setup Time	1	10			10			ns
RS0–RS2 Hold Time	2	10			10			ns
RD* Asserted to Data Bus Driven	3	5			5			ns
RD* Asserted to Data Valid	4			40			40	ns
RD* Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup Time	7	10			10			ns
Write Data Hold Time	8	3			3			ns
RD*, WR* Pulse Width Low	9	50			50			ns
RD*, WR* Pulse Width High	10	6*p13			6*p13			ns
Pixel and Control Setup Time	11	3			3			ns
Pixel and Control Hold Time	12	3			3			ns
Clock Cycle Time (p13)	13	12.5			15.15			ns
Clock Pulse Width High Time	14	4			5			ns
Clock Pulse Width Low Time	15	4			5			ns
Analog Output Delay	16			30			30	ns
Analog Output Rise/Fall Time	17			3			3	ns
Analog Output Settling Time (Note 1)	18		13			13		ns
Clock and Data Feedthrough (Note 1)			–30			–30		dB
Glitch Impulse (Note 1)			75			75		pV - sec
DAC-to-DAC Crosstalk			–3			–23		dB
Analog Output Skew				2			2	ns
Pipeline Delay		4	4	4	4	4	4	Clocks
VAA Supply Current (Note 2)	IAA		180	240		180	240	mA

See test conditions and notes on next page.

AC Characteristics *(continued)*

		80 MHz Devices			66 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Clock Rate	Fmax			50			35	MHz
RS0–RS2 Setup Time	1	10			10			ns
RS0–RS2 Hold Time	2	10			10			ns
RD* Asserted to Data Bus Driven	3	5			5			ns
RD* Asserted to Data Valid	4			40			40	ns
RD* Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup Time	7	10			10			ns
Write Data Hold Time	8	3			3			ns
RD*, WR* Pulse Width Low	9	50			50			ns
RD*, WR* Pulse Width High	10	6*p13			6*p13			ns
Pixel and Control Setup Time	11	3			3			ns
Pixel and Control Hold Time	12	3			3			ns
Clock Cycle Time (p13)	13	20			28			ns
Clock Pulse Width High Time	14	6			7			ns
Clock Pulse Width Low Time	15	6			9			ns
Analog Output Delay	16			30			30	ns
Analog Output Rise/Fall Time	17			3			3	ns
Analog Output Settling Time (Note 1)	18		20			28		ns
Clock and Data Feedthrough (Note 1)			–30			–30		dB
Glitch Impulse (Note 1)			75			75		pV - sec
DAC-to-DAC Crosstalk			–23			–23		dB
Analog Output Skew				2			2	ns
Pipeline Delay		4	4	4	4	4	4	Clocks
VAA Supply Current (Note 2)	IAA		180	240		180	240	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with external voltage reference, RSET = 147 Ω, VREF = 1.235 V, SETUP = 7.5 IRE, and 8/6* = logical one. For 28-pin DIP version of the Bt476, IREF = –8.39 mA. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. Timing reference points at 50 percent for inputs and outputs. Analog output load ≤ 10 pF and D0–D7 output load ≤ 75 pF. See timing waveforms and notes in Figures 7 and 8. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Clock and data feedthrough is a function of the number of edge rates, and the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2x clock rate.

Note 2: at Fmax. IAA (typ) at VAA = 5.0 V. IAA (max) at VAA (max).

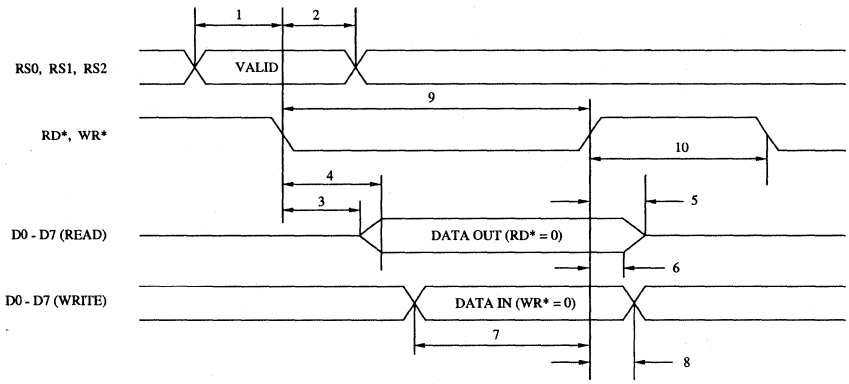
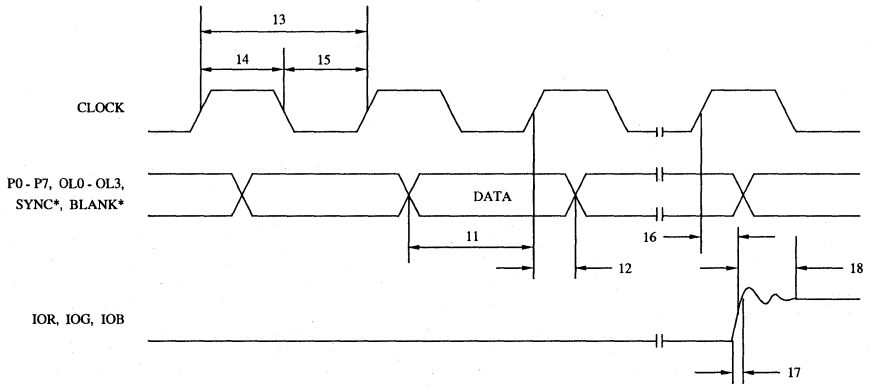


Figure 7. MPU Read/Write Timing Dimensions.



Note 1: Output delay is measured from the 50-percent point of the rising edge of CLOCK to the 50-percent point of full-scale transition.

Note 2: Settling time is measured from the 50-percent point of full-scale transition to the output remaining within ±1 LSB (Bt478), ±1/4 LSB (Bt471), or ±1/2 LSB (Bt476).

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 8. Video Input/Output Timing.

Ordering Information

Model Number	Color Palette RAM	Overlay Palette	Sync Generation	Speed	Package	Ambient Temperature Range
Bt471KPJ80	256 x 18	15 x 18	yes	80 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt471KPJ66	256 x 18	15 x 18	yes	66 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt471KPJ50	256 x 18	15 x 18	yes	50 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt471KPJ35	256 x 18	15 x 18	yes	35 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt476KPJ66	256 x 18	—	no	66 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt476KPJ50	256 x 18	—	no	50 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt476KPJ35	256 x 18	—	no	35 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt476KP66	256 x 18	—	no	66 MHz	28-pin 0.6" Plastic DIP	0° to +70° C
Bt476KP50	256 x 18	—	no	50 MHz	28-pin 0.6" Plastic DIP	0° to +70° C
Bt476KP35	256 x 18	—	no	35 MHz	28-pin 0.6" Plastic DIP	0° to +70° C
Bt478KPJ80	256 x 24	15 x 24	yes	80 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt478KPJ66	256 x 24	15 x 24	yes	66 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt478KPJ50	256 x 24	15 x 24	yes	50 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt478KPJ35	256 x 24	15 x 24	yes	35 MHz	44-pin Plastic J-Lead	0° to +70° C