ANALOG DEVICES

AD1848

Parallel-Port 16-Bit SoundPort® Stereo Codec

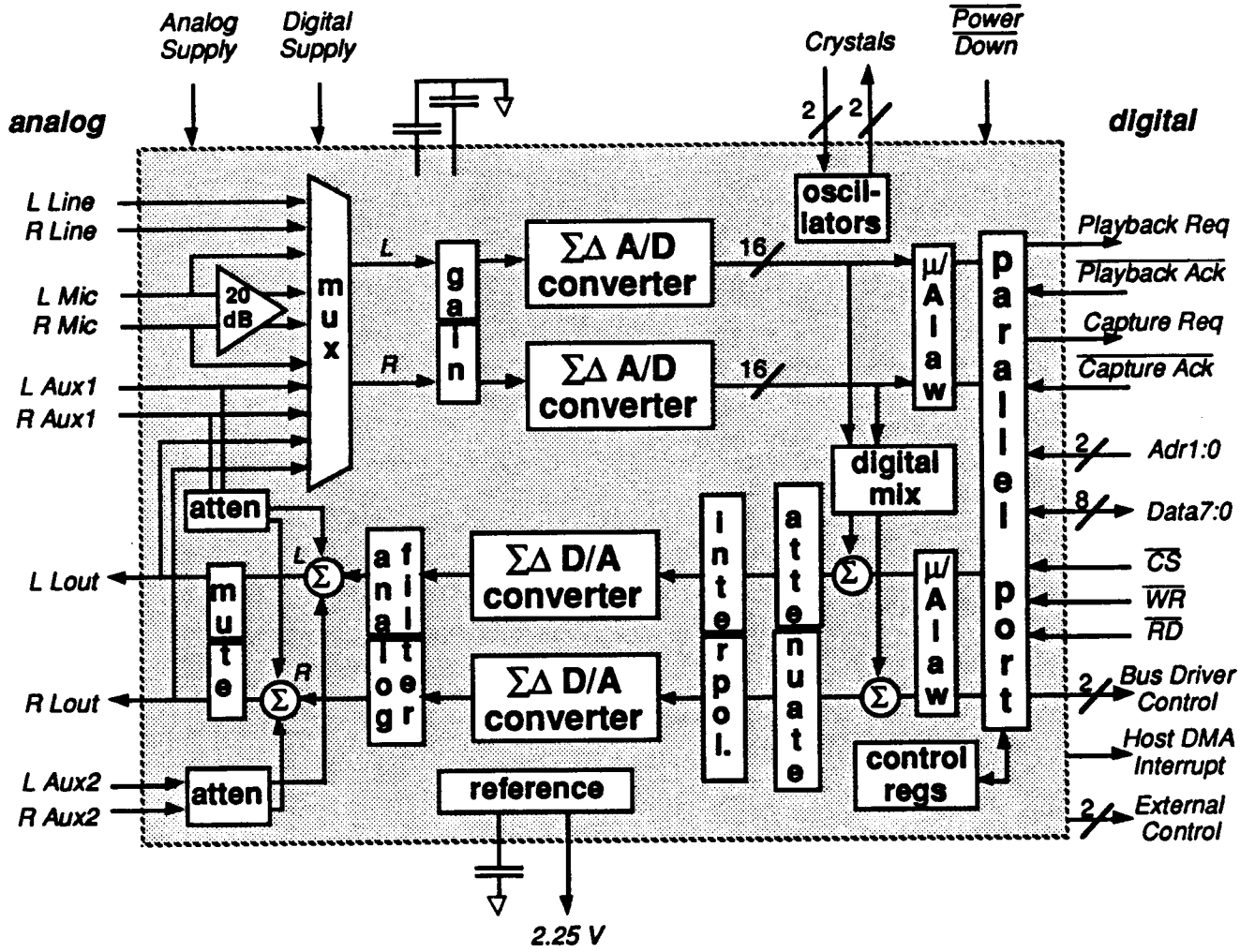
PRELIMINARY INFORMATION

Rev. 1.1 — 7/31/92

FEATURES

Single-Chip Integrated ΣΔ Digital Audio Stereo Codec
Multiple Channels of Stereo Input and Output
Analog and Digital Signal Mixing
Programmable Gain and Attenuation
On-Chip Signal Filters
- **Digital Interpolation**
- **Analog Output Low-Pass**

Sample Rates from 5.5 kHz to 48 kHz
68-Lead PLCC Package
Operation from +5V Supplies
Byte-Wide Parallel Interface to ISA and EISA buses
Supports One or Two DMA channels and Programmed I/O



Preliminary Technical Data: This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

PRODUCT OVERVIEW

The Parallel-Port AD1848 SoundPort® Stereo Codec integrates the key audio data conversion and control functions into a single integrated circuit. The AD1848 is intended to provide a complete, single-chip audio solution for business audio and multimedia applications requiring operation from a single +5V supply. It provides a direct, byte-wide interface to both ISA ("AT") and EISA computer buses for simplified implementation on a computer motherboard or add-in card. The AD1848 generates enable and direction controls for IC buffers such as 74_245.

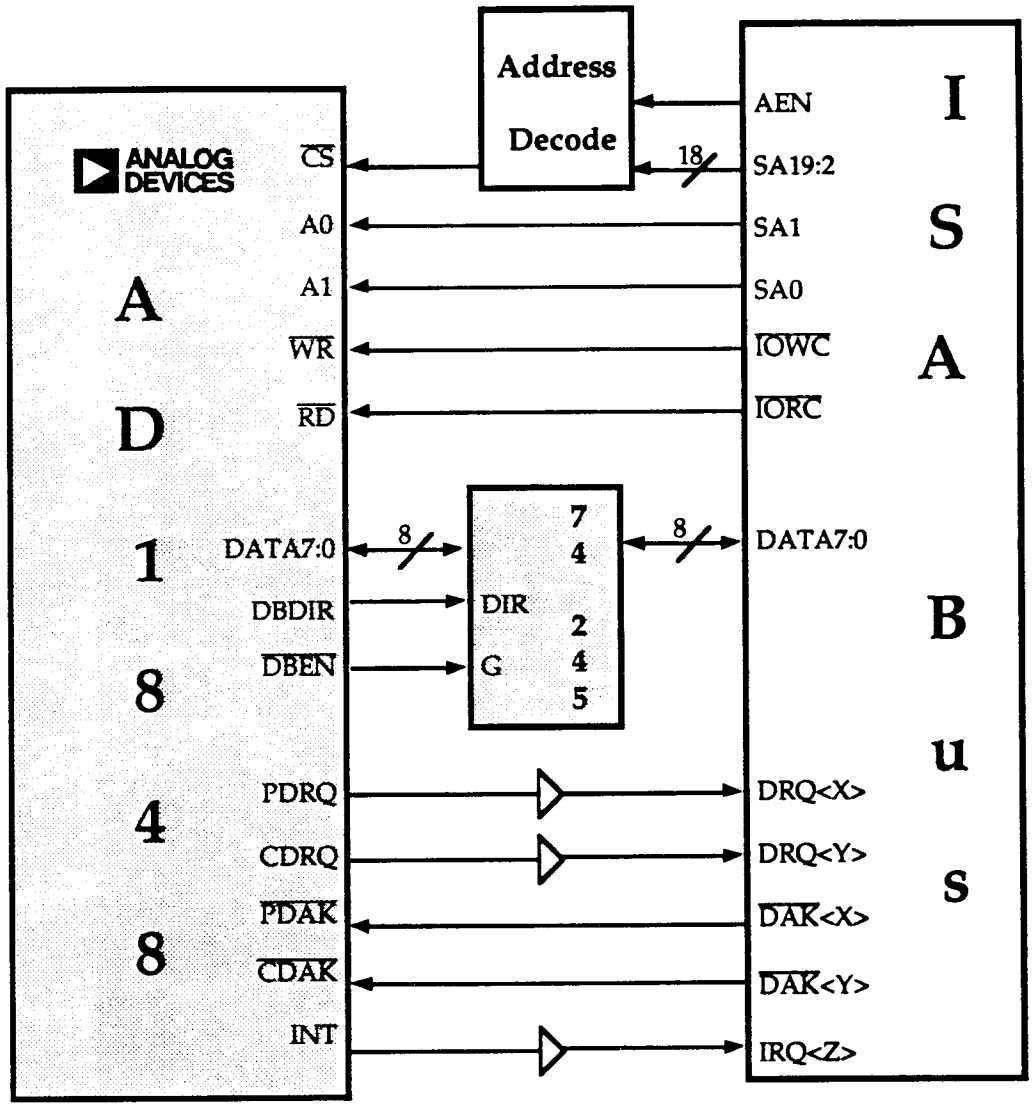


Figure 1. AD1848 Interface to ISA Bus

The AD1848 SoundPort Stereo Codec supports a DMA request/grant architecture for transferring data with

the host computer bus. One or two DMA channels can be supported. Programmed I/O (PIO) mode is also supported for control register accesses and for applications lacking DMA control. Two input control lines support mixed direct indirect addressing of twenty-one internal control registers over this asynchronous interface.

External circuit requirements are limited to a minimal number of low-cost support components. Anti-imaging DAC output filters are incorporated on-chip. Dynamic range exceeds 80 dB over the 20 kHz audio band. Sample rates from 5.5 kHz to 48 kHz are supported from external crystals.

The Codec includes a stereo pair of ΣΔ analog-to-digital converters and a stereo pair of ΣΔ digital-to-analog converters. Inputs to the ADC can be selected from four stereo pairs of analog signals: line, microphone, auxiliary line #1, and post-mixed DAC output. The microphone inputs can pass through optional 20 dB gain blocks. A software-controlled programmable gain stage allows independent gain for each channel going into the ADC. The ADCs' output can be digitally mixed with the DACs' input.

The pair of 16-bit outputs from the ADCs is available over a byte-wide bidirectional interface that also supports 16-bit digital input to the DACs and control information. The AD1848 can accept and generate 16-bit twos-complement PCM linear digital data, 8-bit unsigned magnitude PCM linear data, and 8-bit μ-law or A-law companded digital data.

The ΣΔ DACs are preceded by a digital interpolation filter. An attenuator provides independent user control over each DAC channel. Nyquist images are removed from the DACs' analog stereo output by on-chip switched-capacitor and continuous-time filters. Two stereo pairs of auxiliary line-level inputs can also be mixed in the analog domain with the DAC output.

ORDERING INFORMATION

Pre-production quantities of the AD1848 SoundPort Stereo Codec will be available through Analog Devices, its representatives, and its distributors. Quantities up to ten units can be booked as "AD1848XP." They will typically ship within seven days. Quantities greater than ten require the buyer to sign our AD1848 X-Grade Acceptance Agreement. This agreement acknowledges that the buyer understands that these are pre-production units and that they are non-returnable. The agreement can be obtained at the factory from Donna Molinari at 617-937-1480.

The price for one to ninety-nine units of AD1848XP is $54 per unit FOB Norwood, Massachusetts. Quantities greater than ninety-nine are not available prior to product release (October 31, 1992).

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AD1848 PINLIST

Parallel Interface

Pin Name	*Number*	*I/O*	*Description*
CDRQ	12	O	Capture Data Request. The assertion of this signal indicates that the Codec has a captured audio sample from the ADC ready for transfer. This signal will remain asserted until all the bytes from the capture buffer have been transferred.
$\overline{\text{CDAK}}$	11	I	Capture Data Acknowledge. The assertion of this active LO signal indicates that the $\overline{\text{RD}}$ cycle occurring is a DMA read from the capture buffer.
PDRQ	14	O	Playback Data Request. The assertion of this signal indicates that the Codec is ready for more DAC playback data. The signal will remain asserted until all the bytes needed for a playback sample have been transferred.
$\overline{\text{PDAK}}$	13	I	Playback Data Acknowledge. The assertion of this active LO signal indicates that the $\overline{\text{WR}}$ cycle occurring is a DMA write to the playback buffer.
ADR1:0	9&10	I	Codec Addresses. These address pins are asserted by the Codec interface logic during a control register / PIO access. The state of these address lines determine which register is accessed.
$\overline{\text{RD}}$	60	I	Read Command Strobe. This active LO signal defines a read cycle to the Codec. The cycle may be a read from the control / PIO registers, or the cycles could be a read from the Codec's DMA sample registers.
$\overline{\text{WR}}$	61	I	Write Command Strobe. This active LO signal indicates a write cycle to the Codec. The cycle may be a write to the control / PIO registers, or the cycle could be a write to the Codec's DMA sample registers.
$\overline{\text{CS}}$	59	I	AD1848 Chip Select. The Codec will not respond to any control / PIO cycle accesses unless this active LO signal is LO. This signal is ignored during DMA transfers.
DATA7:0	3-6 & 65-68	I/O	Data Bus. These pins transfer data and control to and from the AD1848.
$\overline{\text{DBEN}}$	64	O	Data Bus Enable. This pin enables the external bus drivers normally attached. This signal is normally HI. For control register / PIO cycles, $\overline{\text{DBEN}}$ = ($\overline{\text{WR}}$ *or* $\overline{\text{RD}}$) *and* $\overline{\text{CS}}$ For DMA cycles, $\overline{\text{DBEN}}$ = ($\overline{\text{WR}}$ *or* $\overline{\text{RD}}$) *and* ($\overline{\text{PDAK}}$ *or* $\overline{\text{CDAK}}$)
DBDIR	62	O	Data Bus Direction. This pin controls the direction of the data bus

transceiver. HI enables transfers from the host to the AD1848; LO enables transfers from the AD1848 to the host bus. This signal is normally HI.

For control register / PIO cycles,

DBDIR = $\overline{RD}$ *and* $\overline{CS}$

For DMA cycles,

DBDIR = $\overline{RD}$ *and* ($\overline{PDAK}$ *or* $\overline{CDAK}$)

Analog Signals

Pin Name	*Number*	*I/O*	*Description*
L_LINE	30	I	Left Line Input. Line level input for the left channel.
R_LINE	27	I	Right Line Input. Line level input for the right channel.
L_MIC	29	I	Left Microphone Input. Microphone input for the left channel. This signal can be either line level or –20 dB from line level.
R_MIC	28	I	Right Microphone Input. Microphone input for the right channel. This signal can be either line level or –20 dB from line level.
L_AUX1	39	I	Left Auxiliary #1 Line Input
R_AUX1	42	I	Right Auxiliary #1 Line Input
L_AUX2	38	I	Left Auxiliary #2 Line Input
R_AUX2	43	I	Right Auxiliary #2 Line Input
L_OUT	40	O	Left Line Level Output
R_OUT	41	O	Right Line Level Output

Miscellaneous

Pin Name	*Number*	*I/O*	*Description*
XTAL1I	17	I	25.567 MHz Crystal #1 Input
XTAL1O	18	O	25.567 MHz Crystal #1 Output
XTAL2I	21	I	16.934 MHz Crystal #2 Input
XTAL2O	22	O	16.934 MHz Crystal #2 Output
$\overline{PWRDWN}$	23	I	Power Down Signal. Active LO control places AD1848 in its lowest power consumption mode. All sections of the AD1848, including the digital

			interface, are shut down and consuming minimal power.
INT	57	O	Host Interrupt Pin. This signal is used to notify the host that the DMA Current Count Register has underflowed.
XCTL1:O	56&58	O	External Control. These signals reflect the current status of register bits inside the AD1848. They can be used for signaling or to control external logic.
VREF	32	O	Voltage Reference. Nominal 2.25 volt reference available externally as a datum for DC-coupling and level-shifting.
VREF_F	33	I	Voltage Reference Filter. Voltage reference filter point for external bypassing.
L_FILT	31	I	Left Channel Filter Input. This pin requires a 1000 pF[1] capacitor to analog ground.
R_FILT	26	I	Right Channel Filter Input. This pin requires a 1000 pF[2] capacitor to analog ground.
N/C	46-52,55		No-connect. Do not connect.

Power Supplies

Pin Name	*Number*	*I/O*	*Description*
VCC	35&36	I	Analog supply voltage
GNDA	37	I	Analog ground
VDD	1,7,15,19,24,45,54	I	Digital supply voltage
GNDD	2,8,16,20,25,44,53,64	I	Digital ground

AUDIO FUNCTIONAL DESCRIPTION

This section overviews the functionality of the AD1848 and is intended as a general introduction to the capabilities of the device. As much as possible, detailed reference information has been placed in "Control Registers" and other sections. The user is not expected to refer repeatedly to this section.

Analog Inputs

The AD1848 SoundPort Stereo Codec accepts stereo line-level and mic-level inputs. These inputs are internally buffered to protect the user from driving a switched-capacitor load. These buffers eliminate the need for active front-end conditioning circuitry. LINE, MIC, AUX1, and post-mixed DAC output analog

[1] The value of this capacitor will change with the next revision of silicon.

[2] The value of this capacitor will change with the next revision of silicon.

stereo signals are multiplexed to the internal programmable gain amplifier stage (PGA). Each channel of the mic inputs can be amplified by +20 dB prior to the PGA to compensate for the voltage swing difference between line levels and typical condenser microphones. Alternatively, mic inputs can bypass the +20 dB fixed gain block and go straight to the input multiplexer.

The PGA following the input multiplexer allows independent selectable gains for each channel from 0 to 22.5 dB in +1.5 dB steps. The Codec can operate either in a global stereo mode or in a global mono mode with left-channel inputs appearing at both channel outputs.

Analog Mixing

AUX1 and AUX2 analog stereo signals can be mixed in the analog domain with the DAC output. Each channel of each auxiliary analog input can be independently attenuated from 0 to –22.5 dB in –1.5 dB steps or completely muted. The post-mixed DAC output is available on LOUT externally and as an input to the ADCs.

Analog-to-Digital Datapath

The ΣΔ ADCs incorporate a proprietary fourth-order modulator similar to that used in the AD1879 18-Bit ΣΔ Stereo ADC. A single pole of passive filtering is all that is required for anti-aliasing the analog input because of the ADC's high 64 times oversampling ratio. The ADCs include linear-phase digital decimation filters that lowpass filters the input to $0.4 \bullet F_S$. ("F_S" is the word rate or "sampling frequency.") ADC input overrange conditions will cause bits to be set that can be read and cleared under software control.

Digital-to-Analog Datapath

The ΣΔ DACs are preceded by a programmable digital attenuator and a lowpass filters digital interpolation filter. The anti-imaging interpolation filter oversamples by 64 and digitally filters the higher frequency images. The attenuator allows independent control of each DAC channel from 0 dB to 93 dB in 1.5 dB steps plus full mute. The DACs' ΣΔ noise shapers also oversample by 64 and convert the signal to a single-bit stream. The DAC outputs are then filtered in the analog domain by a combination of switched-capacitor and continuous-time filters. They remove the very high frequency components of the DAC bitstream output. No external components are required. Exceptional phase linearity at the analog output is achieved by internally compensating for the group delay variation of the analog output filters.

Changes in DAC output volume take effect only on zero crossings of the digital signal, thereby eliminating "zipper" noise. Each channel has its own independent zero-crossing detector and attenuator change control circuitry. A timer guarantees that requested volume changes will occur even in the absence of an input signal that changes sign. The time-out period is 10.7 milliseconds at a 48 kHz sampling rate and 64 milliseconds at an 8 kHz sampling rate. (Time-out [ms] ≈ $512 \div F_S$ [kHz]).

Digital Mixing

A digital mix is also supported that digitally mixes a portion of the analog input (after digitization) with the digital input. Stereo digital output from the ADCs going out the data port is unaffected by monitor mix. Along the digital mix datapath, the 16-bit linear output from the ADCs is attenuated by an amount specified with control bits. Both channels of the monitor data are attenuated by the same amount. (Note that internally — digital mixing included — the AD1848 always works with 16-bit PCM linear data; format conversions take place at input and output.)

Sixty-four steps of –1.5 dB attenuation are supported. The digital mix datapath can also be completely muted, preventing any mixing of the analog input with the analog output. Note that the volume of the mixing signal

is also a function of the input PGA settings, since they affect the ADCs' output.

The attenuated digital mix data is digitally summed with the DAC input data prior to the DACs' datapath attenuators. Because both stereo signals are mixed before the output attenuators, mix data is attenuated a second time by the DACs' datapath attenuators. The digital sum of digital mix data and input DAC data is clipped at plus or minus full scale and does not wrap around.

Even if the AD1848 is not capturing data from its ADCs, the digital mix function can still be active.

In case the AD1848 is capturing data but output digital ADC data is not removed in time ("ADC overrun"), then the last sample captured before overrun will be used for the digital mix. In case the AD1848 is playing back data but input digital DAC data fails to arrive in time ("DAC underrun"), then a midscale zero will be added to the digital mix data.

Analog Outputs

A stereo line-level output is available at external pins. Each channel of this output can be independently muted. When muted, the outputs will settle to a dc value near VREF, the midscale reference value.

Digital Data Types

The AD1848 supports four global data types: 16-bit twos-complement linear PCM, 8-bit unsigned linear PCM, companded μ-law, and 8-bit companded A-law, as specified by control register bits. Data in all four formats is always transferred MSB first. 8-bit data is always left-justified in 16-bit fields; said in other words, the MSBs of all data types are always aligned; in yet other words, full-scale representations in all four formats correspond to equivalent full-scale signals. The eight least-significant bit positions of 8-bit data in 16-bit fields are ignored on input and zeroed on output.

The 16-bit PCM data format is capable of representing 96 dB of dynamic range. 8-bit PCM can represent 48 dB of dynamic range. Companded μ-law and A-law data formats use non-linear coding with less precision for large-amplitude signals. The loss of precision is compensated for by an increase in dynamic range to 64 dB and 72 dB, respectively.

On input, 8-bit companded data is expanded to an internal linear representation, according to whether μ-law or A-law was specified as the Codec's internal registers. Note that when μ-law compressed data is expanded to a linear format, it requires 14 bits. A-law data expanded requires 13 bits.

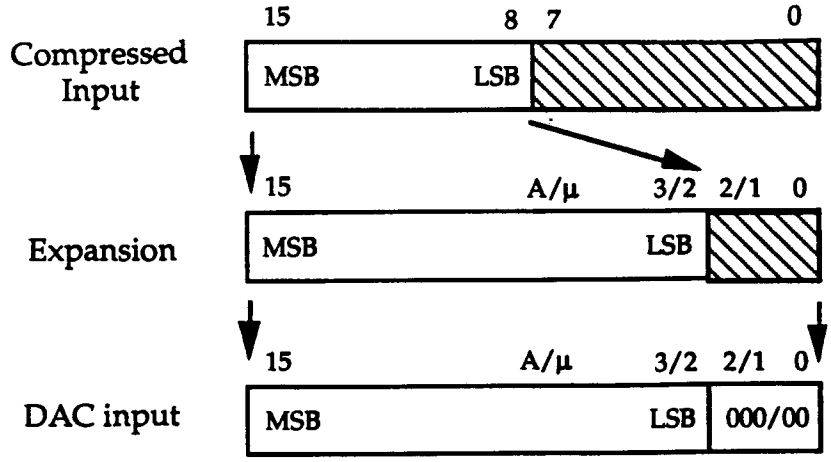

Figure 2. μ-Law or A-Law Expansion

When 8-bit companding is specified, the ADCs' linear output is compressed to the format specified prior to output.

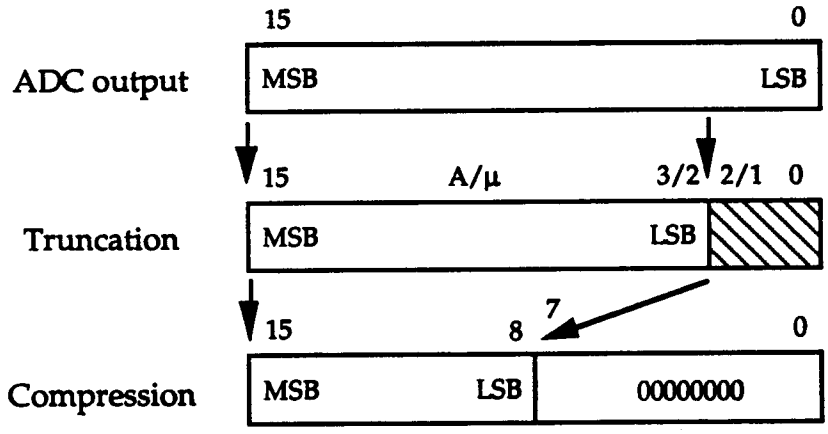

Figure 3. μ-Law or A-Law Compression

Note that all format conversions take place at input or output. Internally, the AD1848 uses 16-bit linear PCM representations to maintain maximum precision.

Power Supplies and Voltage Reference

The AD1848 operates from +5V power supplies. Independent analog and digital supplies are recommended for optimal performance though excellent results can be obtained in single-supply systems. A voltage reference is included on the Codec and its 2.25 V buffered output is available on an external pin (VREF). The

reference output can be used for biasing op amps used in dc coupling. The internal reference is externally bypassed to analog ground at the VREF_F pin.

Clocks and Sample Rates

The AD1848 operates internally from external crystals. Two crystal inputs are provided to generate a wide range of sample rates. The oscillators for these crystals are on the AD1848, as is a multiplexer for selecting between them. They can be overdriven with external clocks by the user, if so desired. The recommended crystal frequencies are 16.9344 MHz and 24.576 MHz. From them the following sample rates are divided down: 5.5125, 6.615, 8, 9.6, 11.025, 16, 18.9, 22.05, 27.42857, 32, 33.075, 37.8, 44.1, 48 kHz.

CONTROL REGISTERS

Control Register Architecture

The AD1848 SoundPort Stereo Codec accepts both data and control information through its byte-wide parallel port. Indirect addressing minimizes the external pins required to access all 21 of its byte-wide internal registers. Only two external address pins, ADR1:0, are required to accomplish all data and control transfers. These pins select one of five direct registers. (Adr1:0=3 addresses two registers, depending on whether the transfer is a playback or a capture.)

ADR1:0	*Register Name*
0	Index Address Register
1	Indexed Data Register
2	Status Register
3	PIO Data Registers

Figure 4. AD1848 Direct Register Map

A write to or read from the Indexed Data Register will be access the Indirect Register indexed by the value most recently written to the Index Address Register. The Status Register and the PIO Data Register are always accessible directly, without indexing. The 16 Indirect Registers are indexed as follows:

Index	*Register Name*
0	Left Input Control
1	Right Input Control
2	Left Aux #1 Input Control
3	Right Aux #1 Input Control
4	Left Aux #2 Input Control
5	Right Aux #2 Input Control
6	Left Output Control
7	Right Output Control
8	Clock and Data Format
9	Interface Configuration
10	Pin Control
11	Test and Initialization
12	Miscellaneous Information
13	Digital Mix
14	Upper Base Count
15	Lower Base Count

Figure 5. AD1848 Indirect Register Map

A detailed map of all direct and indirect register contents is summarized for reference as follows:

Direct Registers:

Adr1:0	*Data 7*	*Data 6*	*Data 5*	*Data 4*	*Data 3*	*Data 2*	*Data 1*	*Data 0*
0	INIT	MCE	TRD	res	IA3	IA2	IA1	IA0
1	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
2	CU/L	CL/R	CRDY	SOUR	PU/L	PL/R	PRDY	INT
3	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
3	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Indirect Registers:

IA3:0	*Data 7*	*Data 6*	*Data 5*	*Data 4*	*Data 3*	*Data 2*	*Data 1*	*Data 0*
0	LSS1	LSS0	LMGE	res	LIG3	LIG2	LIG1	LIG0
1	RSS1	RSS0	RMGE	res	RIG3	RIG2	RIG1	RIG0
2	LMX1	res	res	res	LX1A3	LX1A2	LX1A1	LX1A0
3	RMX1	res	res	res	RX1A3	RX1A2	RX1A1	RX1A0
4	LMX2	res	res	res	LX2A3	LX2A2	LX2A1	LX2A0
5	RMX2	res	res	res	RX2A3	RX2A2	RX2A1	RX2A0
6	LOM	res	LOA5	LOA4	LOA3	LOA2	LOA1	LOA0
7	ROM	res	ROA5	ROA4	ROA3	ROA2	ROA1	ROA0
8	res	FMT	L/C	S/M	CFS2	CFS1	CFS0	CSS
9	CPIO	PPIO	res	res	ACAL	SDC	CEN	PEN
10	XCTL1	XCTL0	res	res	res	res	IEN	res
11	COR	PUR	ACI	DRS	ORR1	ORR0	ORL1	ORL0
12	res	res	res	res	ID3	ID2	ID1	ID0
13	DMA5	DMA4	DMA3	DMA2	DMA1	DMA0	res	DME
14	UB7	UB6	UB5	UB4	UB3	UB2	UB1	UB0
15	LB7	LB6	LB5	LB4	LB3	LB2	LB1	LB0

Figure 6. AD1848 Register Summary

Note that the only sticky bit in any of the AD1848 control registers is the interrupt (INT) bit. All other bits change with every sample period.

Direct Control Register Definitions

Index Register (ADR1:0 = 0)

Adr1:0	*Data 7*	*Data 6*	*Data 5*	*Data 4*	*Data 3*	*Data 2*	*Data 1*	*Data 0*
0	INIT	MCE	TRD	res	IA3	IA2	IA1	IA0

IA3:0 — Index Address. These bits define the address of the AD1848 register accessed by the Indexed Data Register. These bits are read/write.

res — Reserved for future expansion. Always write zeros to these bits.

TRD — Transfer Request Disable. This bit, when set, causes DMA transfers to cease when the Interrupt Status (INT) bit of the Status Register is set.

0 Transfers Enabled During Interrupt (PDRQ and CDRQ occur uninhibited by interrupts)
1 Transfers Disabled By Interrupt (PDRQ and CDRQ only occur if INT bit is 0)

MCE Mode Change Enable. This bit must be set whenever the current functional mode of the AD1848 is changed. Specifically, the Clock and Data Format and Interface Configuration registers cannot be changed unless this bit is set. The exceptions are CEN and PEN in the Interface Configuration which can be changed "on-the-fly." MCE should be cleared at the completion of the desired register changes.

DAC outputs are automatically muted when the MCE bit is set. After MCE is cleared, DAC outputs will be restored to the state specified by the LOM and ROM mute bits. DAC outputs should be muted after the MCE bit is cleared for at least 64 sample cycles, i.e., ~12 ms @ 5.5 kHz F_S.[3]

Special sequences must be followed if autocalibrate (ACAL) is set or sample rates are changed (CFS2:0 and or CSS) during mode change enable. See the "Autocalibration" and "Changing Sample Rates" sections below.

INIT AD1848 Initialization. This bit is set when the AD1848 is in a state which is can not respond to parallel interface cycles. This bit is read-only.

Immediately after reset and once the AD1848 has left the INIT state, the initial value of this register will be "01000000 (40h)." During AD1848 initialization, this register cannot be written and is always read "10000000 (80h)."

Indexed Data Register (ADR1:0 = 1)

Adr1:0	*Data 7*	*Data 6*	*Data 5*	*Data 4*	*Data 3*	*Data 2*	*Data 1*	*Data 0*
1	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

ID7:0 Indexed Register Data. These bits contain the contents of the AD1848 register referenced by the Indexed Data Register.

During AD1848 initialization, this register cannot be written and is always read "10000000 (80h)."

Status Register (ADR1:0 = 2)

Adr1:0	*Data 7*	*Data 6*	*Data 5*	*Data 4*	*Data 3*	*Data 2*	*Data 1*	*Data 0*
2	CU/L	CL/R	CRDY	SOUR	PU/L	PL/R	PRDY	INT

INT Interrupt Status. This sticky bit (the only one) indicates the status of the interrupt logic of the AD1848. This bit is cleared by any host write of any value to this register. The IEN bit of the Pin Control Register determines whether the state of this bit is reflected on the INT pin of the AD1848.

[3] LOM and ROM can be set at the time MCE is cleared, if desired. This requirement will be eliminated in future silicon.

The only interrupt condition supported by the AD1848 is generated by the underflow of the DMA Current Count Register.

0 Interrupt pin inactive
1 Interrupt pin active

PRDY — Playback Data Register Ready. The PIO Playback Data Register is ready for more data. This bit should only be used when direct programmed I/O data transfers are desired. This bit is read-only.

0 DAC data is still valid. Do not overwrite.
1 DAC data is stale. Ready for next host data write value.

PL/R — Playback Right/Left Sample. This bit indicates whether the PIO playback data needed is for the right channel DAC or left channel DAC. This bit is read-only.

0 Right channel data needed
1 Left channel data or mono

PU/L — Playback Upper/Lower Byte. This bit indicates whether the PIO playback data needed is for the upper or lower byte of the channel. This bit is read-only.

0 Lower byte needed
1 Upper byte needed or any 8-bit mode

SOUR — Sample Over/Underrun. This bit indicates that the most recent sample was not serviced in time and therefore either an overrun (SOR) or underrun (PUR) has occurred. The bit indicates an overrun for ADC capture and underrun for DAC playback. If both capture and playback are enabled, the source which set this bit can be determined by reading SOR and PUR. This bit is read-only.

CRDY — Capture Data Ready. The PIO Capture Data Register contains data ready for reading by the host. This bit should only be used when direct programmed I/O data transfers are desired. This bit is read-only.

0 ADC data is stale. Do not reread the information.
1 ADC data is fresh. Ready for next host data read.

CL/R — Capture Right/Left Sample. This bit indicates whether the PIO capture data waiting is for the right channel ADC or left channel ADC. This bit is read-only.

0 Right channel data
1 Left channel data or mono

CU/L — Capture Upper/Lower Byte. This bit indicates whether the PIO capture data ready is for the upper and lower byte of the channel. This bit is read-only.

0 Lower byte ready
1 Upper byte ready or any 8-bit mode

The PRDY, CRDY, and INT bits of this status register can change asynchronously to host accesses. The host may access this register while the bits are transitioning. The host read may return a zero value and a one value will not be read until the next host access, for example.

PIO Data Registers (ADR1:0 = 3)

Adr1:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
3	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
3	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

The PIO Data Registers are two registers mapped to the same address. Writes send data to the PIO Playback Data Register (PD7:0). Reads will receive data from the PIO Capture Data Register (CD7:0).

During AD1848 initialization, the PIO Playback Data Register cannot be written and the Capture Data Register is always read "10000000 (80h)."

CD7:0 PIO Capture Data Register. This is the control register where capture data is read during programmed I/O data transfers.

The reading of this register will increment the state machine so that the following read will be from the next appropriate byte in the sample. The exact byte which is next to be read can be determined by reading the Status Register. Once all relevant bytes have been read, the state machine will stay pointed to the last byte of the sample until a new sample is received from the ADCs. Once this has occurred, the state machine and status register will point to the first byte of the sample. Until a new sample is received, reads from this register will return the most significant byte of the sample.

PD7:0 PIO Playback Data Register. This is the control register where playback data is written during programmed I/O data transfers.

Writing data to this register will increment the playback byte tracking state machine so that the following write will be to the correct byte of the sample. Once all bytes of a sample have been written, subsequent byte writes to this port are ignored. The state machine is reset when the current sample is sent to the DACs.

Indirect Control Register Definitions

The following control registers are accessed by writing index values to IA3:0 in the Index Address Register (ADR1:0 = 0) followed by a read/write to the Indexed Data Register (ADR1:0 = 1).

Left Input Control (IA3:0 = 0)

IA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0	LSS1	LSS0	LMGE	res	LIG3	LIG2	LIG1	LIG0

LIG3:0 Left input gain select. The least significant bit of this gain select represents +1.5 dB. Maximum gain is +22.5 dB. An autocalibration should be performed before capture is enabled if these gain bits have changed since the previous autocalibration.[4]

res Reserved for future expansion. Always write zeros to these bits.

LMGE Left Input Microphone Gain Enable. This bit will enable the +20 dB gain of the left mic input signal.

LSS1:0 Left Input Source Select. These bits select the input source for the left gain stage going to the left

[4] This requirement will be eliminated in future silicon.

ADC.

0 Left Line Source Selected
1 Left Auxiliary 1 Source Selected
2 Left Microphone Source Selected
3 Left Line Post-Mixed DAC Output Source Selected

This register's initial state after reset is "00000000."

Right Input Control (IA3:0 = 1)

IA3:0	*Data 7*	*Data 6*	*Data 5*	*Data 4*	*Data 3*	*Data 2*	*Data 1*	*Data 0*
1	RSS1	RSS0	RMGE	res	RIG3	RIG2	RIG1	RIG0

RIG3:0 Right Input Gain Select. The least significant bit of this gain select represents +1.5 dB. Maximum gain is +22.5 dB. An autocalibration should be performed before capture is enabled if these gain bits have changed since the previous autocalibration.[5]

res Reserved for future expansion. Always write zeros to these bits.

RMGE Right Input Mic Gain Enable. This bit will enable the +20 dB gain of the right mic input signal.

RSS1:0 Right Input Source Select. These bits select the input source for the right channel gain stage going to the right ADC.

0 Right Line Source Selected
1 Right Auxiliary 1 Source Selected
2 Right Microphone Source Selected
3 Right Post-Mixed DAC Output Source Selected

This register's initial state after reset is "00000000."

Left Auxiliary #1 Input Control (IA3:0 = 2)

IA3:0	*Data 7*	*Data 6*	*Data 5*	*Data 4*	*Data 3*	*Data 2*	*Data 1*	*Data 0*
2	LMX1	res	res	res	LX1A3	LX1A2	LX1A1	LX1A0

LX1A3:0 Left Auxiliary Input #1 Attenuate Select. The least significant bit of this attenuate select represents –1.5 dB. Maximum attenuation is –22.5 dB.

res Reserved for future expansion. Always write zeros to these bits.

LMX1 Left Auxiliary #1 Mute. This bit, when set, will mute the left channel of the Auxiliary #1 input source. This bit powers up active.

This register's initial state after reset is "10000000 (80h)."

Right Auxiliary #1 Input Control (IA3:0 = 3)

[5] This requirement will be eliminated in future silicon.

IA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
3	RMX1	res	res	res	RX1A3	RX1A2	RX1A1	RX1A0

RX1A3:0 Right Auxiliary Input #1 Attenuate Select. The least significant bit of this attenuate select represents –1.5 dB. Maximum attenuation is –22.5 dB.

res Reserved for future expansion. Always write zeros to these bits.

RMX1 Right Auxiliary #1 Mute. This bit, when set, will mute the right channel of the Auxiliary #1 input source. This bit powers up active.

This register's initial state after reset is "10000000 (80h)."

Left Auxiliary #2 Input Control (IA3:0 = 4)

IA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
4	LMX2	res	res	res	LX2A3	LX2A2	LX2A1	LX2A0

LX2A3:0 Left Auxiliary Input #2 Attenuate Select. The least significant bit of this attenuate select represents –1.5 dB. Maximum attenuation is –22.5 dB.

LMX2 Left Auxiliary #2 Mute. This bit, when set to 1, will mute the left channel of the Auxiliary #2 input source. This bit powers up active.

This register's initial state after reset is "10000000 (80h)."

Right Auxiliary #2 Input Control (IA3:0 = 5)

IA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
5	RMX2	res	res	res	RX2A3	RX2A2	RX2A1	RX2A0

RX2A3:0 Right Auxiliary Input #2 Attenuate Select. The least significant bit of this attenuate select represents –1.5 dB. Maximum attenuation is –22.5 dB.

res Reserved for future expansion. Always write zeros to these bits.

RMX2 Right Auxiliary #2 Mute. This bit, when set to 1, will mute the right channel of the Auxiliary #2 input source. This bit powers up active.

This register's initial state after reset is "10000000 (80h)."

Left Output Control (IA3:0 = 6)

IA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
6	LOM	res	LOA5	LOA4	LOA3	LOA2	LOA1	LOA0

LOA5:0 Left Output Attenuate Select. The least significant bit of this attenuate select represents –1.5 dB. Maximum attenuation is –94.5 dB.

res Reserved for future expansion. Always write zeros to these bits.

LOM Left Output Mute. This bit, when set to 1, will mute the left channel output. This bit powers bit active.

This register's initial state after reset is "1x000000."

Right Output Control (IA3:0 = 7)

IA3:0	*Data 7*	*Data 6*	*Data 5*	*Data 4*	*Data 3*	*Data 2*	*Data 1*	*Data 0*
7	ROM	res	ROA5	ROA4	ROA3	ROA2	ROA1	ROA0

ROA5:0 Right Output Attenuate Select. The least significant bit of this attenuate select represents –1.5 dB. Maximum attenuation is –94.5 dB.

res Reserved for future expansion. Always write zeros to these bits.

ROM Right Output Mute. This bit, when set to 1, will mute the right channel output. This bit powers up active.

This register's initial state after reset is "1x000000."

Clock and Data Format Register (IA3:0 = 8)

IA3:0	*Data 7*	*Data 6*	*Data 5*	*Data 4*	*Data 3*	*Data 2*	*Data 1*	*Data 0*
8	res	FMT	L/C	S/M	CFS2	CFS1	CFS0	CSS

The contents of the Clock and Data Format Register cannot be changed except when the AD1848 is in Mode Change Enable (MCE). Write attempts to this register when the AD1848 is not in MCE will not be successful.

CSS Clock Source Select. These bits select the crystal clock source which will ultimately be used for the audio sample rates.

0 XTAL1 (24.576 MHz)
1 XTAL2 (16.9344 MHz)

CFS2:0 Clock Frequency Divide Select. These bits select the audio sample rate frequency. The actual audio sample rate depends on which crystal clock source is selected and the frequency of that source.

	Divide Factor	*XTAL1 24.576 MHz*	*XTAL2 16.9344 MHz*
0	3072	8.0 kHz	5.5125 kHz
1	1536	16.0 kHz	11.025 kHz

2	896	27.42857 kHz	18.9 kHz
3	768	32.0 kHz	22.05 kHz
4	448	N/A	37.8 kHz
5	384	N/A	44.1 kHz
6	512	48.0 kHz	33.075 kHz
7	2560	9.6 kHz	6.615 kHz

Note that the AD1848's internal oscillators can be overdriven by external clock sources at the crystal input pins. If an externally clock source is applied, it will be divided down by the selected Divide Factor. It need not be at the recommended crystal frequencies.

S/M — Stereo/Mono Select. This bit determines how the audio data streams are formatted. Selecting stereo will result with alternating samples representing left and right audio channels. Mono playback plays the same audio sample on both channels. Mono capture only captures data from the left audio channel.

0 Mono
1 Stereo

L/C — Linear/Companded Select. This bit selects between a linear digital representation of the audio signal or a non-linear, companded format for all input and output data. The type of companded format is defined by the FMT bits.

0 Linear
1 Companded

FMT — Format Select. This bit defines the format for all digital audio input and outputs based on the state of the L/C bit.

	Linear PCM (L/C = 0)	*Companded (L/C = 1)*
0	8-bit Unsigned PCM	8-bit μ-law Companded
1	16-bit Twos-Complement PCM	8-bit A-law Companded

res — Reserved for future expansion. Always write zeros to these bits.

This register's initial state after reset is "x0000000."

Interface Configuration Register (IA3:0 = 9)

IA3:0	*Data 7*	*Data 6*	*Data 5*	*Data 4*	*Data 3*	*Data 2*	*Data 1*	*Data 0*
9	CPIO	PPIO	res	res	ACAL	SDC	CEN	PEN

The contents of the Interface Configuration Register cannot be changed except when the AD1848 is in Mode Change Enable (MCE). Write attempts to this register when the AD1848 is not in MCE will not be successful. PEN and CEN are exceptions; these bits may always be written.

PEN — Playback Enable. This bit will enable the playback of data in the format selected. The AD1848 will generate PDRQ and respond to $\overline{PDAK}$ signals when this bit is enabled and PPIO=0. If PPIO=1, this bit enables PIO playback mode. PEN may be set and reset without setting the MCE bit.

0 Playback disabled (PDRQ and PIO Playback Data Register inactive)
1 Playback enabled

CEN — Capture Enable. This bit will enable the capture of data in the format selected. The AD1848 will generate CDRQ and respond to $\overline{\text{CDAK}}$ signals when this bit is enabled and CPIO=0. If CPIO=1, this bit enabled PIO capture mode. CEN may be set and reset without setting the MCE bit.

- 0 Capture disable (CDRQ and PIO Capture Data Register inactive)
- 1 Capture enabled

SDC — Single DMA Channel. This bit will force both capture and playback DMA requests to occur on the Playback DMA channel. The Capture DMA CDRQ pin will be zero. This bit will allow the AD1848 to be used with only one DMA channel. Simultaneous capture and playback cannot occur in this mode. Should both cpature and playback be enabled (CEN=PEN=1) in the mode, only playback will occur. See "Data and Control Transfers" for further explanation.

- 0 Dual DMA channel mode
- 1 Single DMA channel mode

ACAL — Autocalibrate Enable. This bit determines whether the AD1848 performs an autocalibrate whenever returning from the $\overline{\text{PWRDWN}}$ pin being asserted or from the Mode Change Enable (MEC) bit being asserted. If the ACAL bit is not set, any previous autocalibrate is cleared when returning from mode-change (MCE) and no autocalibrate takes place. Therefore, ACAL is normally set. See "Autocalibration" below for a description of a complete autocalibration sequence.

- 0 No autocalibration
- 1 Autocalibration after reset or mode change

res — Reserved for future expansion. Always write zeros to these bits.

PPIO — Playback PIO Enable. This bit determined whether the playback data is transferred via DMA or PIO.

- 0 DMA transfers only
- 1 PIO transfers only

CPIO — Capture PIO Enable. This bit determines whether the capture data is transferred via DMA or PIO.

- 0 DMA transfers only
- 1 PIO transfers only

This register's initial state after reset is "00xx1000 (x8h)."

Pin Control Register (IA3:0 = 10)

IA3:0	*Data 7*	*Data 6*	*Data 5*	*Data 4*	*Data 3*	*Data 2*	*Data 1*	*Data 0*
10	XCTL1	XCTL0	res	res	res	res	IEN	res

IEN — Interrupt Enable. This bit enables the interrupt pin. That Interrupt Pin will go active HI when the number of samples programmed in the Base Count Register is reached.

- 0 Interrupt disabled
- 1 Interrupt enabled

res — Reserved for future expansion. Always write zeros to these bits.

XCTL1:0 External Control. The state of these bits is reflected on the XCTL1:0 pins of the AD1848.

0 TTL Logic LO on XCTL1:0 pins
1 TTL Logic HI on XCTL1:0 pins

This register's initial state after reset is "00x000x0x."

Test and Initialization Register (IA3:0 = 11)

IA3:0	*Data 7*	*Data 6*	*Data 5*	*Data 4*	*Data 3*	*Data 2*	*Data 1*	*Data 0*
11	COR	PUR	ACI	DRS	ORR1	ORR0	ORL1	ORL0

ORL1:0 Overrange Left Detect. These bits determine the overrange on the left input channel. This bit is read-only.

0 Less than –1 dB underrange
1 Between –1 dB and 0 dB underrange
2 Between 0 dB and +1 dB overrange
3 Greater +1 dB overrange

ORR1:0 Overrange Right Detect. These bits determine the overrange on the right input channel. This bit is read-only.

0 Less than –1 dB underrange
1 Between –1 dB and 0 dB underrange
2 Between 0 dB and +1 dB overrange
3 Greater +1 dB overrange

DRS Data Request Status. This bit indicates the current status of the PDRQ and CDRQ pins of the AD1848.

0 CDRQ and PDRQ are presently inactive
1 CDRQ or PDRQ are presently active

ACI Autocalibrate-In-Progress. This bit indicates the state of autocalibration. This bit is read-only.

0 Autocalibration not in progress
1 Autocalibration is in progress

PUR Playback Underrun. This bit is set when playback data has not arrived from the host in time to be played. As a result, the previous sample is sent again a midscale value will be sent to the DACs. This bit changes on a sample by sample basis.

COR Capture Overrun. This bit is set when the capture data has not been read by the host before the next sample arrives. The sample being read will not be overwritten by the new sample. The new sample will be ignored. This bit changes on a sample by sample basis.

The occurrence of a PUR and/or COR is designated in the Status Register's Sample Overrun/Underrun (SOUR) bit. The SOUR bit is the logical OR of the COR and PUR bits. This enables a polling host CPU to detect an overrun/underrun condition while checking other status bits.

This register's initial state after reset is "00000000."

Miscellaneous Control Register (IA3:0 = 12)

IA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
12	res	res	res	res	ID3	ID2	ID1	ID0

res — Reserved for future expansion. Always write zeros to these bits.

ID3:0 — AD1848 Revision ID. These four bits define the revision level of the AD1848. The first AD1848 will be designated ID = 1000. These bits are read-only.

This register's initial state after reset is "xxxx1001 (x9h)."

Digital Mix Control Register (IA3:0 = 13)

IA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
13	DMA5	DMA4	DMA3	DMA2	DMA1	DMA0	res	DME

DME — Digital Mix Enable. This bit will enable the digital mix of the AD1848 from the ADCs output to the DACs. When enabled, the data from the ADCs are digitally mixed with other data being delivered to the DACs (regardless of whether or not playback [PEN] is enabled). If capture is enabled (CEN) and there is a capture overrun (COR), then the last sample captured before overrun will be used for the digital mix. If playback is enabled (PEN) and there is a playback underrun (PUR), then a midscale zero will be added to the digital mix data.

0 Digital mix disabled (muted)
1 Digital mix enabled

res — Reserved for future expansion. Always write zeros to these bits.

DMA5:0 — Digital Mix Attenuation. These bits determine the attenuation of the ADC data in mixing with the DAC input. Each attenuate step is –1.5 dB.

This register's initial state after reset is "000000x0."

DMA Base Count Registers (IA3:0 = 13 & 14)

The DMA Base Count Registers in the AD1848 simplify integration of the AD1848 in ISA systems. The ISA DMA controller requires an external count mechanism to notify the host CPU of a full DMA buffer via interrupt. The programmable DMA Base Count Registers will allow such interrupts to occur.

The Base Count Registers contain the number of samples which will occur before an interrupt is generated on the interrupt (INT) pin. First write a value to the Lower Base Count Register. The act of writing a value to the Upper Base Register will cause both Base Count Registers to load into the Current Count Register. Once AD1848 transfers are enabled, each sample will decrement the Current Count Register until zero count is reached. The next sample after zero will generate the interrupt and reload the Current Count Register with the values in the Base Count Registers. The interrupt is cleared by a write to the Status Register.

The Current Count Register is only decremented when a sample is transferred and either the PEN or CEN bit is

enabled.

Upper Base Count Register (IA3:0 = 14)

IA3:0	*Data 7*	*Data 6*	*Data 5*	*Data 4*	*Data 3*	*Data 2*	*Data 1*	*Data 0*
14	UB7	UB6	UB5	UB4	UB3	UB2	UB1	UB0

UB7:0 Upper Base Count. This byte is the upper byte of the base count register. They are the 8 most significant bits of the 16-bit base register. Reads from this register return the same value which was written. The current count contained in the counters can not be read.

This register's initial state after reset is " 00000000."

Lower Upper Base Count Register (IA3:0 = 15)

IA3:0	*Data 7*	*Data 6*	*Data 5*	*Data 4*	*Data 3*	*Data 2*	*Data 1*	*Data 0*
15	LB7	LB6	LB5	LB4	LB3	LB2	LB1	LB0

LB7:0 Lower Base Count. This byte is the lower byte of the base count register. They are the 8 least significant bits of the 16-bit base register. Reads from this register return the same value which was written. The current count contained in the counters cannot be read.

This register's initial state after reset is "00000000."

DATA AND CONTROL TRANSFERS

The AD1848 SoundPort Stereo Codec supports a DMA request/grant architecture for transferring data with the host computer bus. One or two DMA channels can be supported. Programmed I/O (PIO) mode is also supported for control register accesses and for applications lacking DMA control. PIO transfers can be made on one channel while the other is supporting DMA. Transfers to and from the AD1848 SoundPort Codec are asynchronous relative the the internal data conversation clock. Transfers are buffered, but the AD1848 supports no internal FIFOs. The host is responsible for providing playback data before the next digital-to-analog conversion and removing capture data before the next analog-to-digital conversion.

Data Ordering

The number of byte-wide transfers required depends on the data format selected. The AD1848 is designed for "little endian" formats in which the least significant byte (i.e., occupying the lowest memory address) gets transferred first. So 16-bit data transfers require first transferring the least significant bits 7:0 and then transferring the most significant bits 15:8, where bit 15 is the most significant bit in the word.

In addition, left channel data is always transferred before right channel data with the AD1848. The following figures should make these requirements clear.

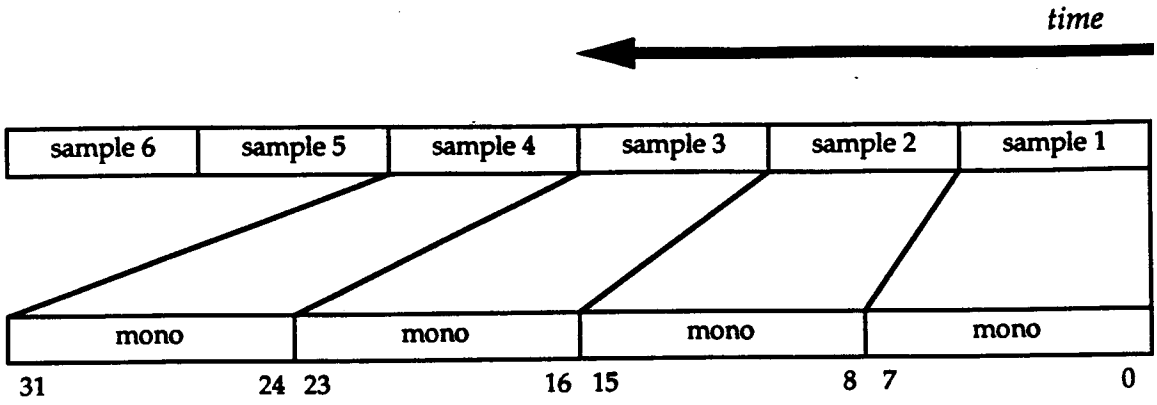

Figure 7. AD1848 8-Bit Mono Data Stream Sequencing

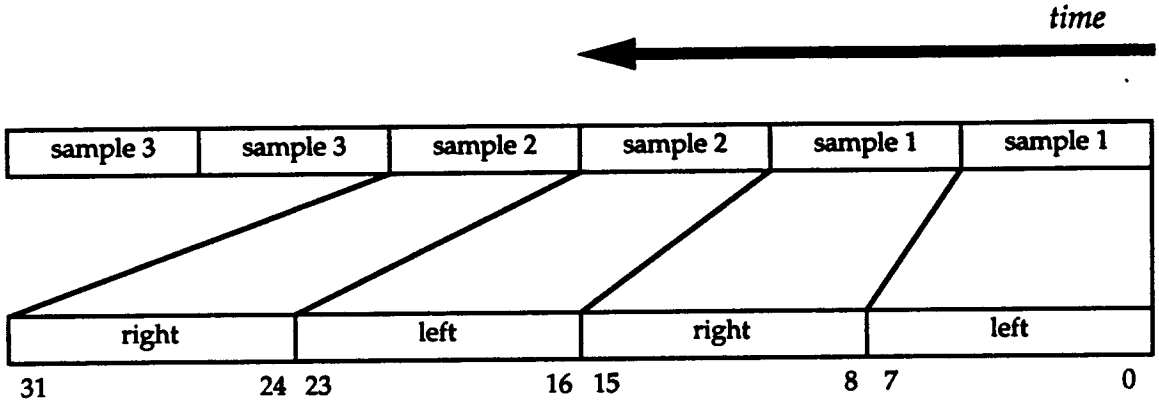

Figure 8. AD1848 8-Bit Stereo Data Stream Sequencing

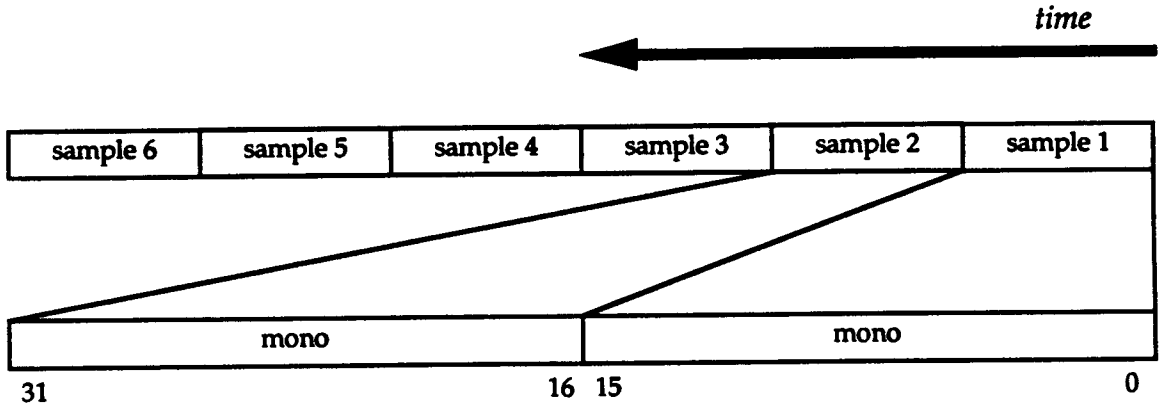

Figure 9. AD1848 16-Bit Mono Data Stream Sequencing

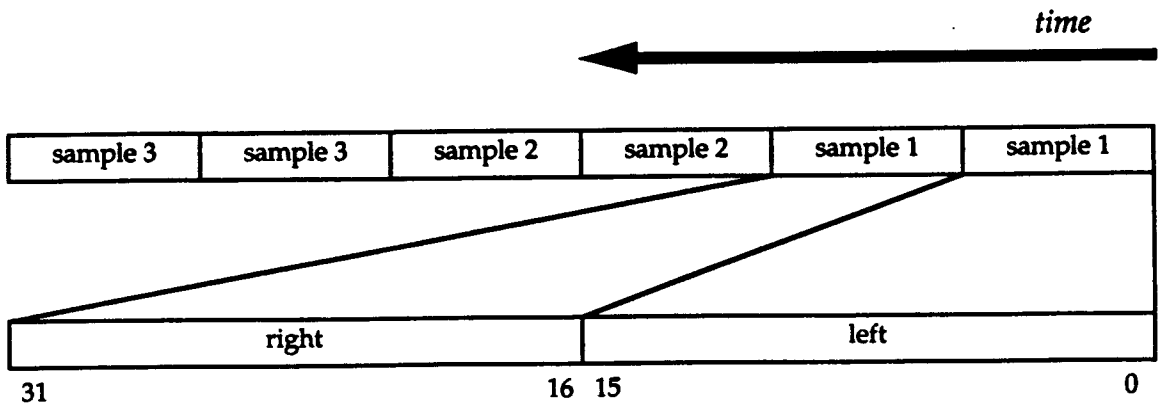

Figure 10. AD1848 16-Bit Stereo Data Stream Sequencing

Control and Programmed I/O (PIO) Transfers

This simpler mode of transfers is used both for control register accesses and programmed I/O. The 21 control and PIO data registers cannot be accessed via DMA transfers. Playback PIO is activated when both playback enable (PEN) is set and Playback PIO (PPIO) is set. Capture PIO is activated when both capture enable (CEN) is set and Capture PIO (CPIO) is set. See Figures 11 and 12 for the detailed timing of the control register / PIO transfers. The $\overline{RD}$ and $\overline{WR}$ signals are used to define the actual read and write cycles, respectively. The host holds $\overline{CS}$ LO during these transfers. The DMA Capture Data Acknowledge ($\overline{CDAK}$) and Playback Data Acknowledge ($\overline{PDAK}$) must be held inactive, i.e., HI.

For read/capture cycles, the AD1848 will assert data on the DATA7:0 lines while the host is asserting the read strobe, $\overline{RD}$, by holding it LO. For write/playback, the host must assert data at the DATA7:0 pins while strobing the $\overline{WR}$ signal. The AD1848 latches the write/playback data on the rising edge of the $\overline{WR}$ strobe.

When using PIO data transfers, the Status Register must be polled to determine when data should be transferred. Note that the ADC capture data will be ready (CRDY HI) from the previous sample period shortly before the DAC playback data is ready (PRDY HI) for the next sample period.

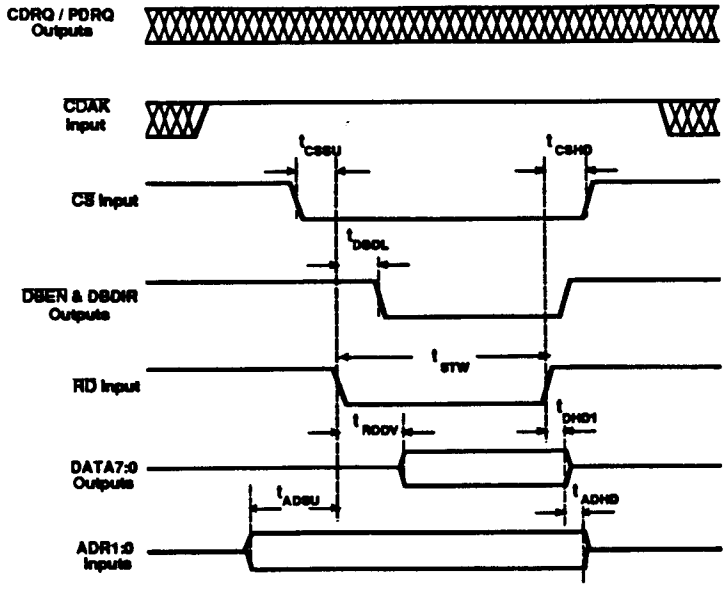

Figure 11. AD1848 Control Register / PIO Read Cycle

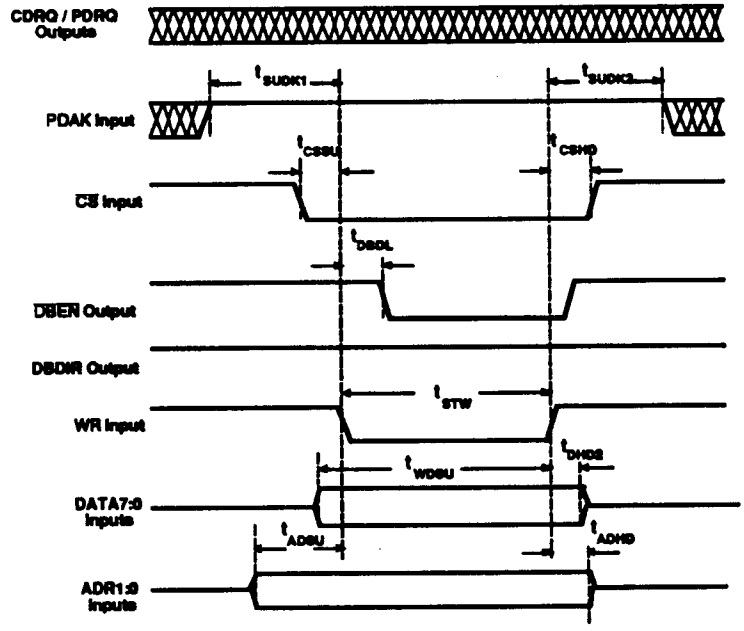

Figure 12. AD1848 Control Register / PIO Write Cycle

Direct Memory Access (DMA) Transfers

The second type of bus cycle supported by the AD1848 are DMA transfers. Both dual channel and single channel DMA operations are supported. To enable Playback DMA transfers, playback enable (PEN) must be set and PPIO cleared. To enable Capture DMA transfers, capture enable (CEN) must be set and CPIO cleared. During DMA transfers, the AD1848 asserts HI the Capture Data Request (CDRQ) or the Playback Data Request (PDRQ) followed by the host's asserting LO the DMA Capture Data Acknowledge ($\overline{\text{CDAK}}$) or Playback Data Acknowledge ($\overline{\text{PDAK}}$), respectively. The host's asserted Acknowledge signals cause the AD1848 to perform DMA transfers. The input address lines, ADR1:0, are ignored. Data is transferred between the proper internal sample registers.

The read strobe ($\overline{\text{RD}}$) and write strobe ($\overline{\text{WR}}$) delimit valid data for DMA transfers. Chip select ($\overline{\text{CS}}$) is a "don't care"; its state is ignored by the AD1848.

The AD1848 may assert the Data Request signals, CDRQ and PDRQ, at any time. Once asserted, these signals will remain active HI until the corresponding DMA cycle occurs with the host's Data Acknowledge signals. The Data Request signals will be deasserted after the falling edge of the *final* $\overline{\text{RD}}$ or $\overline{\text{WD}}$ strobe in the transfer of a sample, which typically consists of multiple bytes. See "Data Ordering" above for a definition of "sample."

DMA transfers may be independently aborted by resetting the Capture Enable (CEN) and/or Playback Enable (PEN) bits in the Interface Configuration Register. The current capture sample transfer will be completed if a capture DMA is terminated. The current playback sample transfer must be completed if a playback DMA is terminated. If CDRQ and/or PDRQ are asserted HI while the host is resetting CEN and/or PEN, the request must be acknowledged. The host must assert $\overline{\text{CDAK}}$ and/or $\overline{\text{PDAK}}$ LO and complete a final sample transfer.

Single-Channel DMA

Single-Channel DMA mode allows the AD1848 to be used in systems with only a single DMA controller. It is enabled by setting the SDC bit in the Interface Configuration Register. All captures and playbacks take place on the single playback channel. Obviously, the AD1848 cannot perform a simultaneous capture and playback in Single-Channel DMA mode.

Playback will occur in single-channel DMA mode exactly as it does in Two-Channel mode. Capture, however, is diverted to the playback channel which means that the capture data request occurs on the PDRQ pin and the capture data acknowledge must be received on the $\overline{\text{PDAK}}$ pin. The CDRQ pin will remain inactive LO. Any inputs to $\overline{\text{CDAK}}$ will be ignored.

Playback and capture are distinguished in Single-Channel DMA mode by the state of the playback enable (PEN) or cpature enable (CEN) control bits. If both PEN and CEN are set in Single-Channel DMA mode, playback will be presumed.

DMA Timing

Below, timing parameters are shown for 8-Bit Mono Sample Read/Capture and Write/Playback DMA transfers in Figures 13 and 14. The same timing parameters apply to multi-byte transfers. The relationship between timing signals is shown in Figures 15 and 16.

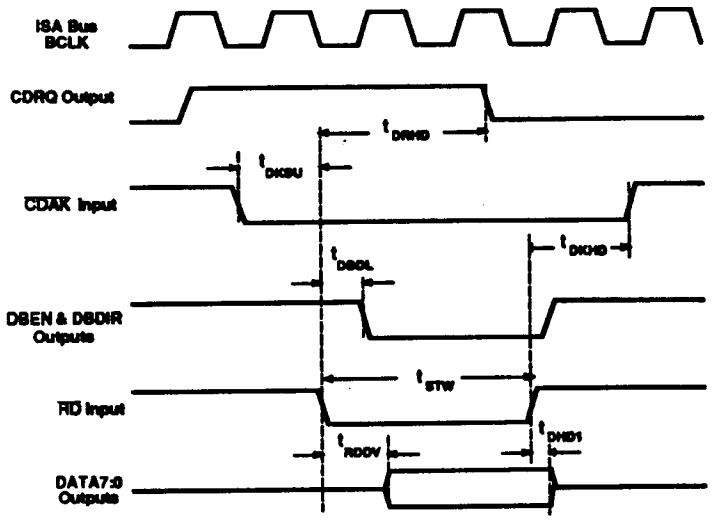

Figure 13. AD1848 8-Bit Mono DMA Read/Capture Cycle

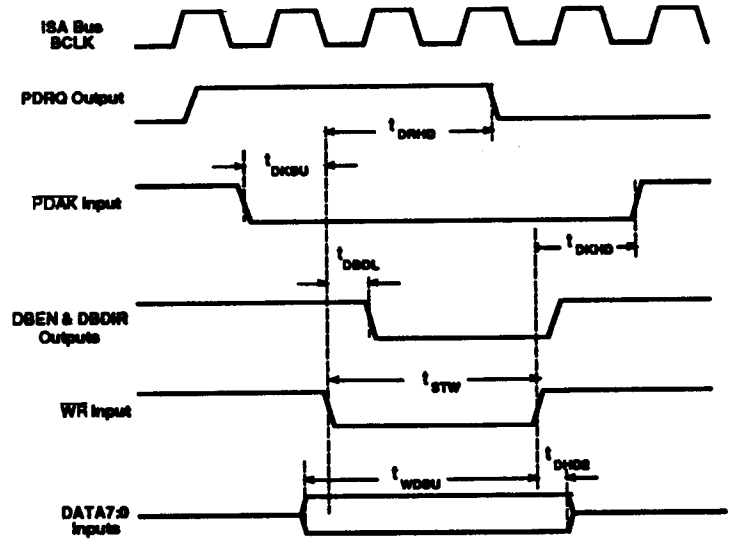

Figure 14. AD1848 8-Bit Mono DMA Write/Playback Cycle

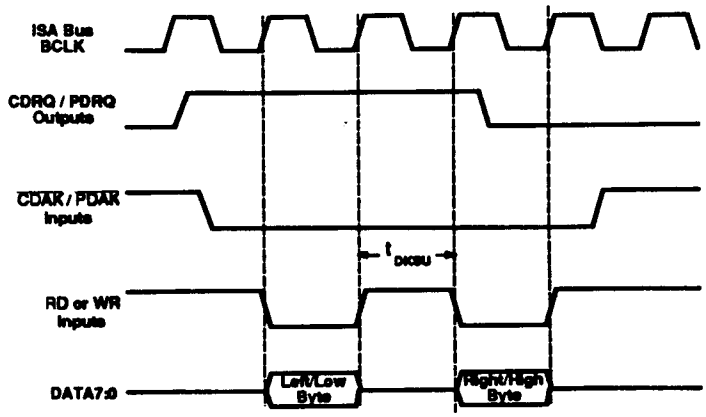

Figure 15. AD1848 8-Bit Stereo or 16-Bit Mono DMA Cycle

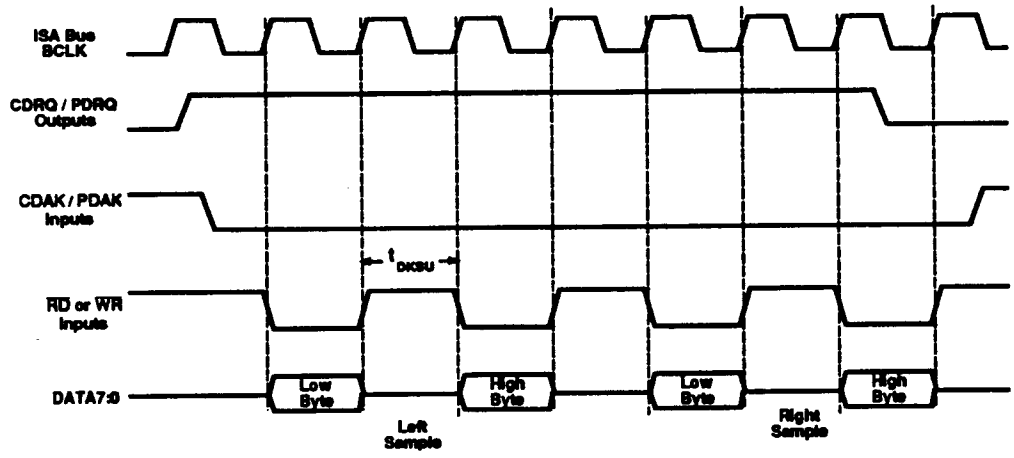

Figure 16. AD1848 16-Bit Stereo DMA Cycle

DMA Interrupt

External DMA controllers require an interrupt generated by the AD1848 to indicate the completion of a DMA transfer. Writing to the internal 16-bit Base Count Register sets up the count value for the number of *samples* to be transferred. Note that the number of bytes transferred for a given count will be a function of the selected global data format. The internal Current Count Register is updated with the current contents of the Upper and Lower Base Count Registers when a write occurs to the Upper Base Count Register.

The Current Count Register cannot be read by the host. Reading the Base Count Registers will only read back the initialization values written to them.

The Current Count Register decrements by one during every sample period. An interrupt event is generated after the Current Count Register is zero and an additional playback sample is transferred. The INT bit in the Status Register always reflects the current internal interrupt state defined above. The external INT pin will only go active HI if the Interrupt Enable (IEN) bit in the Interface Configuration Register is set. If the IEN bit is zero, the external INT pin will always stay LO, even though the Status Register's INT bit may be set.

POWER UP AND RESET

The $\overline{\text{PWRDWN}}$ pin should be held in its active LO state when power is applied to the AD1848. At any point when powered, the AD1848 can be put into a state for minimum power consumption by asserting $\overline{\text{PWRDWN}}$ LO. All analog and digital sections are shut down, and the AD1848's parallel interface does not function.

Deasserting $\overline{\text{PWRDWN}}$ by bringing it HI begins the AD1848's initialization. While initializing, the AD1848 ignores all writes and all reads will yield "1000000 (80h)." At the conclusion of reset initialization, all registers will be set to their default values listed in "Control Registers" above. The conclusion of the initialization process can be detected by polling the index register until some value *other* than "1000000 (80h)" is returned.

AUTOCALIBRATION

The AD1848 can calibrate the ADCs and DACs for greater accuracy by minimizing DC offsets. Autocalibration occurs whenever the AD1848 returns from Mode Change Enable and the ACAL bit in the Interface Configuration register has been set.

The completion of autocalibration can be determined by polling the Autocalibrate-In-Progress (ACI) bit in the Test and Initialization Register, which will be set during autocalibration. Autocalibration will take at least 128 sample periods. Transfers enabled during autocalibration do not begin until the completion of autocalibration.

The following summarizes the procedure for autocalibration:

- Mute left and right DAC outputs, AUX1 and AUX2 inputs, and digital mix
- Set the Mode Change Enable bit (MCE)
- Set the Autocalibration bit (ACAL)
- Clear the Mode Change Enable bit (MCE)
- The Autocalibrate-In-Progress bit (ACI) will shortly transition from LO to HI. It will remain HI for 384 sample periods. Poll the ACI bit until it transitions from HI to LO
- Unmute DAC outputs, AUX inputs, and digital mix.

During the autocalibration sequence, data output from the ADCs is meaningless. Inputs to the DACs are ignored. Even if the user specified the muting of all analog outputs, near the end of the autocalibration sequence, dc analog outputs very close to VREF will be produced at the line output.

CHANGING SAMPLE RATES

To change the selection of the current sampling rate requires a Mode Change Enable sequence since the bits that control that selection are in the Clock and Data Format Register. The fact that the clocks change requires are special sequence which is summarized as follows:

- Mute left and right DAC outputs. If autocalibration will take place at the end of this sequence, then also mute AUX1 and AUX2 inputs and the digital mix.
- Set the Mode Change Enable bit (MCE)
- In a single write cycle, change the Clock Frequency Divide Select (CFS2:0) and/or the Clock Source Select (CSS)
- The AD1848 now needs to resynchronize its internal states to the new clock. Writes to the AD1848 will be ignored. Reads will produce "10000000 (80h)" until the resynchronization is complete. Poll the Index Register until something *other* than this value is returned.
- Clear the Mode Change Enable bit (MCE)
- If ACAL is set, follow the procedure described in "Autocalibration" above
- If ACAL is not set, wait at 70 ms if the 16.9344 MHz crystal has been selected or 90 ms if the 24.576 MHz crystal has been selected
- Unmute DAC outputs.

APPLICATIONS CIRCUITS

The AD1848 Stereo Codec has been designed to require a minimum of external circuitry. What is recommended is shown in Figures 17 through 25. Analog Devices estimates that total cost of all the components shown in these Figures, including crystals, to be less than $3 in 10,000 quantities.

See Figure 1 for an illustration of the connection between the AD1848 SoundPort Codec and the Industry Standard Architecture (ISA) computer bus, also known as the "PC-AT bus." Note that the 245 transceiver receives its enable and direction signals directly from the Codec. Analog Devices recommends using the "slowest" 245 adequately fast to meet all AD1848 and computer bus timing and drive requirements. So doing will minimize the digital feedthrough effects of the 245 transceiver when driving the AD1848.

Industry-standard compact disc "line-levels" are 2 V rms centered around analog ground. (For other audio equipment, "line level" is much more loosely defined.) The AD1848 SoundPort is a +5V only device. Line voltage swings for the AD1848 are defined to be 1 V rms for ADC input and 0.707 V rms for DAC output. Thus, 2 V rms input analog signals must be attenuated and either centered around a voltage intermediate between 0 V and +5 V or ac-coupled. The VREF pin will be at this intermediate voltage, nominally 2.25 V. It has limited drive but can be used as a datum to an op amp input. Note, however, that dc coupling inputs is not recommended, as it provides no performance benefits with the AD1848 architecture. Furthermore, dc offset differences between multiple dc-coupled inputs create the potential for "clicks" when changing the input mux selection.

A circuit for 2 V rms line-level inputs and auxiliaries is shown in Figure 17. Note that this is approximately a divide-by-two resistive divider. The input resistor and 100 pF capacitor provides the single-pole of anti-alias filtering required for the ADCs.

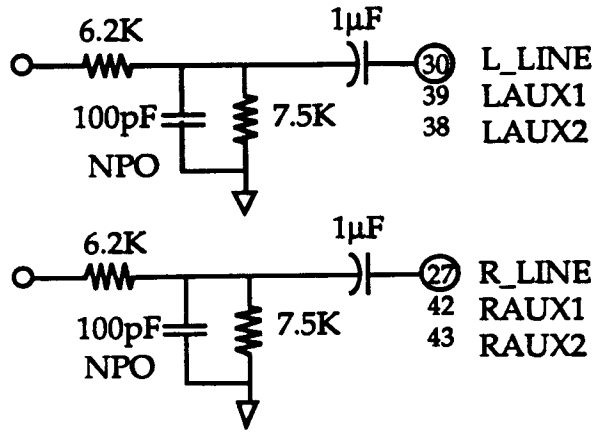

Figure 17. AD1848 2 V rms Line-Level Input Circuit

The AD1848 Codec contains an optional +20 dB gain block to accommodate condenser microphones. What your system requires will depend upon the characteristics of the intended microphone. Figure 18 illustrates one example of how an electret condenser mike requiring phantom power could be connected to the AD1848. VREF is shown buffered by an op amp; a transistor like a 2N4124 should also work fine for this purpose. The values of R_1, R_2, and C should be chosen in light of the mic characteristics and intended gain.

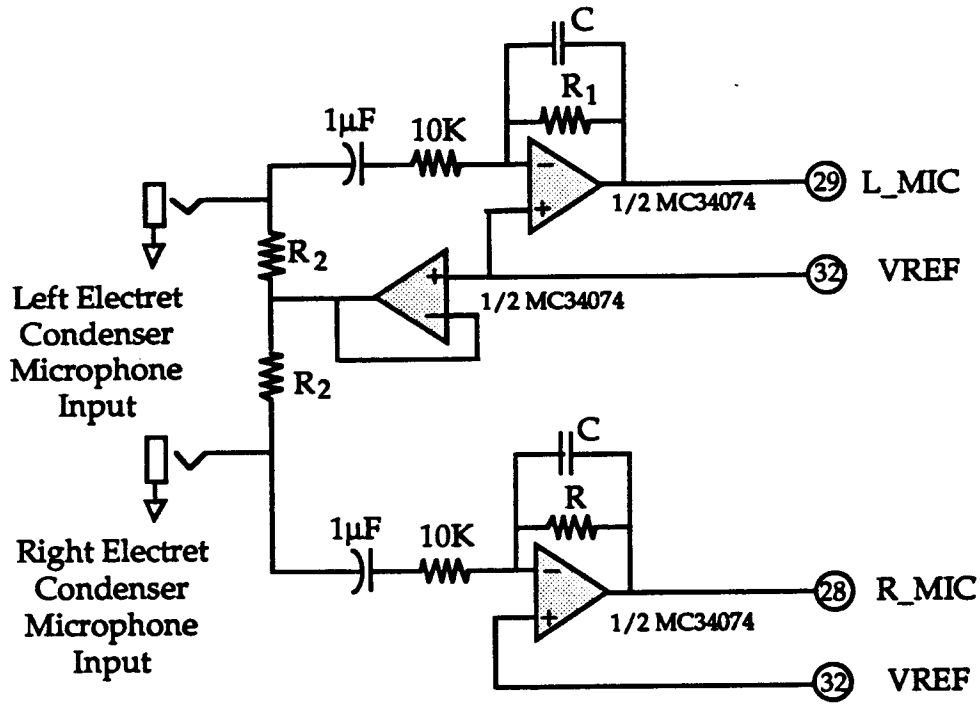

Figure 18. AD1848 "Phantom-Powered" Microphone Input Circuit

Figure 19 shows ac-coupled line outputs. The resistors are used to center the output signals around analog ground. VREF could be used with op amps as mentioned above for dc coupling, if desired.

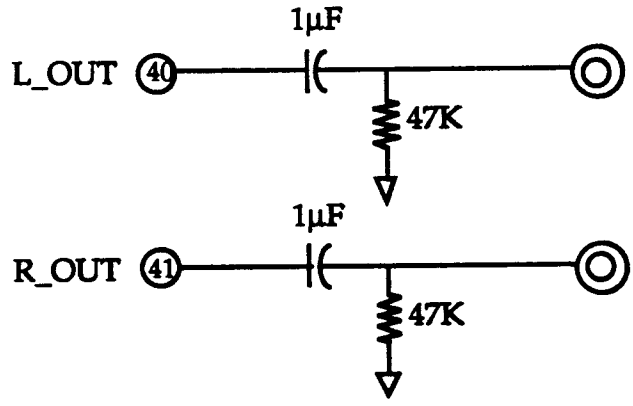

Figure 19. AD1848 Line Output Connections

A circuit for headphone drive is illustrated in Figure 20. Drive is supplied by +5 V power amplifiers. The

circuit shown ac couples the headphones to the line output. For the TDA7053, pins 9 and 16 are outputs and 12 and 13 are no-connects.

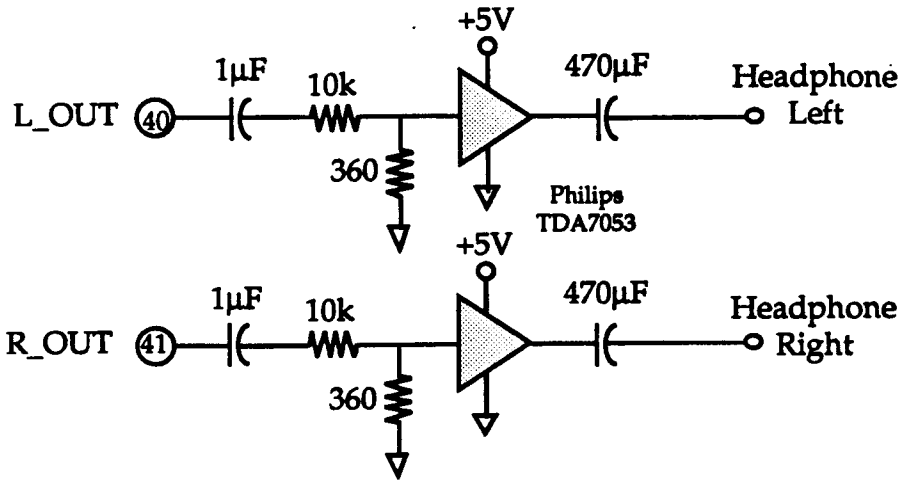

Figure 20. AD1848 Headphone Drive Connections

Figures 21 and 22 illustrate reference bypassing and signal-path filtering capacitors. VREF_F should only be connected to its bypass capacitors. Note that the values recommended here (1000 pF) will increase to a value not yet established with the next revision of silicon. Allow enough board space for a 1 µF capacitor.

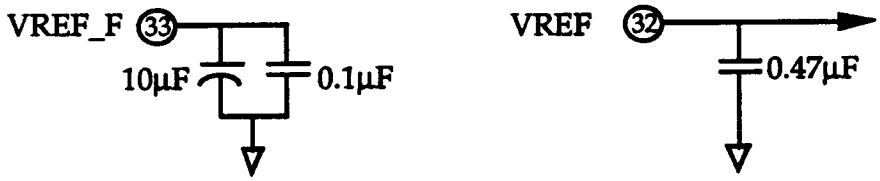

Figure 21. AD1848 Voltage Reference Bypassing

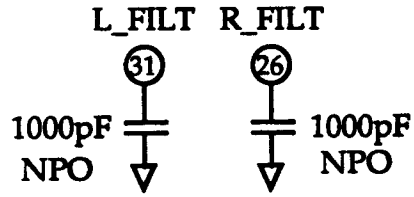

Figure 22. AD1848 External Filter Capacitor Connections

The crystals shown in the crystal connection circuitry of Figure 23 should be fundamental-mode and parallel-tuned. One source for the exact crystals specified is Component Marketing Services in Massachusetts, U.S. at 617-762-4339. Note that using the exact data sheet frequencies is not required and that external clock sources can be used to overdrive the AD1848's internal oscillators. (See description of CFS2:0 control bits above.) If using an external clock source, apply it to the crystal input pins while leaving the crystal output pins unconnected. External input clocks should be low-jitter clocks.

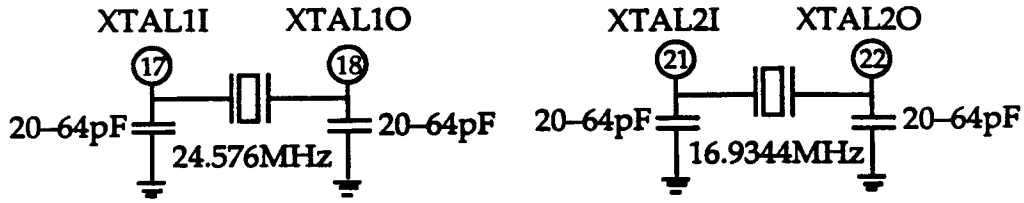

Figure 23. AD1848 Crystal Connections

Analog Devices also recommends pull-down resistors for $\overline{\text{PWRDWN}}$.

Good, standard engineering practices should be applied for power-supply decoupling. Decoupling capacitors should be placed as close as possible to package pins. If a separate analog power supply is not available, we recommend the circuit shown in Figure 24 for using a single +5V supply. Ferrite beads suffice for the inductors shown. This circuitry should be as close to the supply pins as is practical.

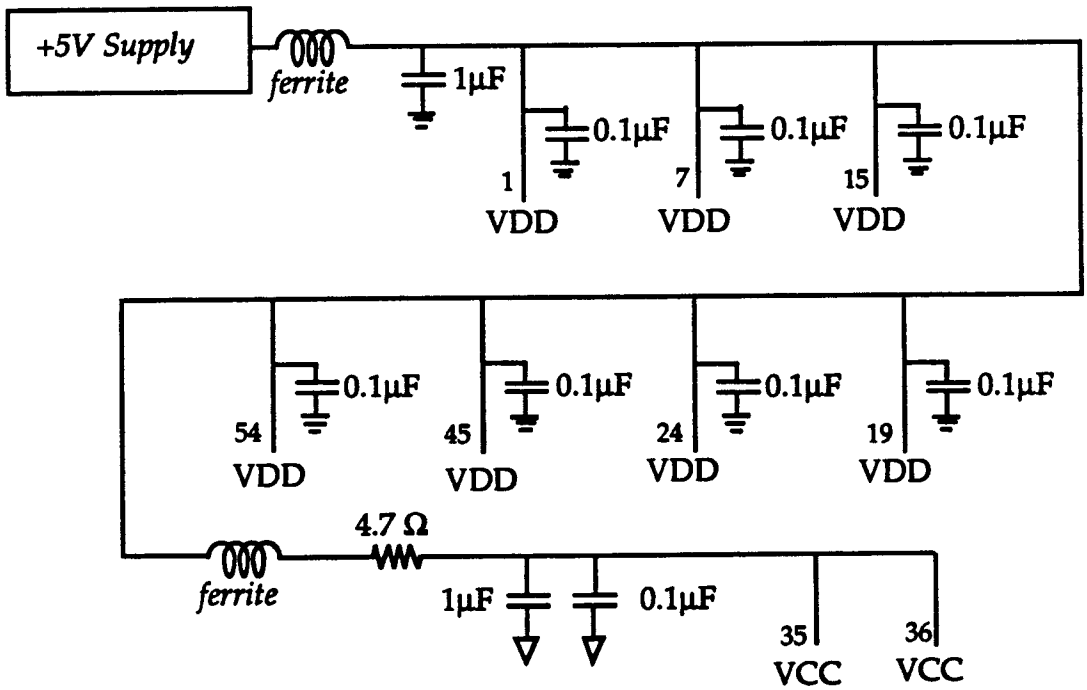

Figure 24. AD1848 Recommended Power Supply Bypassing

Analog Devices recommends a split ground plane as shown in Figure 25. The analog plane and the digital plane are connected directly under the AD1848. Splitting the ground plane directly under the SoundPort Codec is optimal because analog pins will be located above the analog ground plane and digital pins will be located directly above the digital ground plane for the best isolation. Other schemes may also yield satisfactory results.

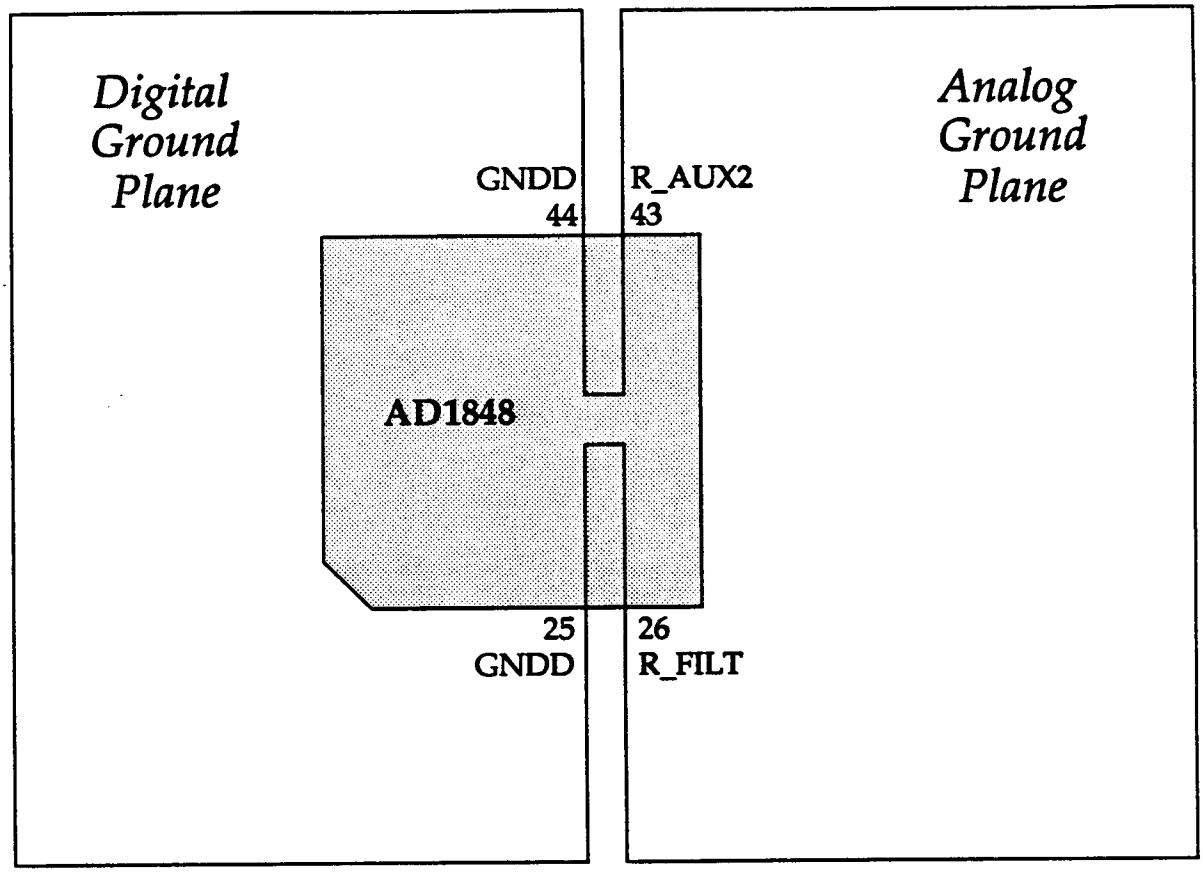

Figure 25. AD1848 Recommended Ground Plane

PRELIMINARY ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

	Min	Max	Units
Power Supplies			
Digital (VDD)	–0.3	6.0	V
Analog (VAA)	–0.3	6.0	V
Input Current (except supply pins)		±10.0	mA
Analog Input Voltage (signal pins)	–0.3	(VA+)+0.3	V
Digital Input Voltage (signal pins)	–0.3	(VD+)+0.3	V
Ambient Temperature (operating)	0	+70	°C
Storage Temperature	–65	+150	°C
ESD Tolerance (Human Body Model per Method 3015.2 of MIL-STD-883B)	1000		V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS UNLESS OTHERWISE NOTED

Temperature	25	°C	
Digital Supply (VD)	5.0	V	
Analog Supply (VA)	5.0	V	
Word Rate (F_s)	48	kHz	
Input Signal	996	Hz	
Analog Output Passband	20	Hz	to 20 kHz
FFT Size	4096		
V_{IH}	TBD	V	
V_{IL}	TBD	V	
V_{OH}	TBD	V	
V_{OL}	TBD	V	

DAC Input Conditions
- 0 dB attenuation
- Full-scale digital inputs
- 16-bit linear mode
- No output load
- Mute off

ADC Input Conditions
- 0 dB gain
- –1.0 dB relative to full-scale
- Line input

All tests are performed on all ADC and DAC channels.

PROGRAMMABLE GAIN AMPLIFIER — ADC

	Min	Typ	Max	Units
Step size (0.0 dB to 18 dB)	1.3	1.5	1.7	dB
Step size (19.5, 21, 22.5 dB) (All steps tested, –30 dB input)	1.0	1.5	2.0	dB
Input Gain Range†	–0.2		22.7	dB

AUXILIARY INPUT ANALOG ATTENUATORS

	Min	Typ	Max	Units
Step size (0.0 dB to –22.5 dB) (All steps tested, –30 dB input)	1.3	1.5	1.7	dB
Input Gain Range†	+0.2		–22.7	dB

DAC ATTENUATOR

	Min	Typ	Max	Units
Step size (0.0 dB to–81 dB) (Tested at steps–19.5, –39 and –60 dB)	1.3	1.5	1.7	dB
Step size (–82.5 dB to–94.5 dB)†	1.0	1.5	2.0	dB
Output Attenuation†	–95		0.2	dB

ANALOG-TO-DIGITAL AND DIGITAL-TO-ANALOG CONVERTERS

	Min	Max	Units

Resolution (No missing codes from ± 10 LSB ramp around mid-scale)	16		bits
Dynamic Range (–60 dB input, THD+N referenced to full scale)	80		dB
Signal-to-(THD+N)		0.02 74	% dB
Signal-to-Intermodulation Distortion†	90		
ADC Crosstalk			
Line Inputs (Input L, ground R, read R; input R, ground L, read L)		–80	dB
Line to Mic (Input LINE ground and select MIC, read both channels)		–60	dB
Line to AUX1		–60	dB
Line to AUX2		–60	dB
DAC Crosstalk (Input L, zero R, measure R_LOUT; input R, zero L, measure L_LOUT)		–80	dB
Gain Error (Full-scale span relative to nominal)		5	%
Interchannel Gain Mismatch (Difference of Gain Errors)		0.5	dB
System Frequency Response† (Line In to Line Out)	–1.0	+0.4	dB
Differential Non-Linearity†		±1	bit
Phase Linearity Deviation†		5	degrees
Total Out-of-Band Energy (Measured from $0.6 \bullet F_s$ to 100 kHz)		–45	dB

DIGITAL DECIMATION AND INTERPOLATION FILTERS†

	Min	Max	Units
Passband	0	$0.4 \bullet F_s$	Hz

Frequency Response	–0.5	+0.2	dB
Passband Ripple		±0.1	dB
Transition Band	$0.4 \bullet F_s$	$0.6 \bullet F_s$	Hz
Stopband	$0.4 \bullet F_s$	∞	Hz
Stopband Rejection	74		dB
Group Delay		$30/F_s$	
Group Delay Variation Over Passband		0.0	µs

ANALOG INPUT

	Min	Max	Units
Input Voltage			
Line		1	V_{rms}
		2.8	V_{p-p}
Mic with +20 dB gain (MGE=1)		0.1	V_{rms}
		0.28	V_{p-p}
Mic with 0 dB gain (MGE=0)		1	V_{rms}
		2.8	V_{p-p}
Input Impedance	20K		Ω
Input Capacitance		15	pF

ANALOG OUTPUT†

	Min	Typ	Max	Units
Full-Scale Output Voltage		0.707		V_{rms}
	1.85	2.0	2.1	V_{p-p}
Output Impedance			600	Ω
External Load Impedance	10			kΩ
Output Capacitance			15	pF

Preliminary Technical Data: This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

External Load Capacitance			100	pF
VREF (clock running)	2.15	2.25	2.35	V
VREF current drive		100		µA
Mute Attenuation of 0 dB Fundamental† (LOUT)			–80	dB

POWER SUPPLY

	Min	Max	Units
Power Supply Range – Digital & Analog (SNR & THD confirmed at limits)	4.75	5.25	V
Power Supply Current – Operating (10k Ω load line)		150	mA
Analog Supply Current – Operating (10k Ω load line)		80	mA
Digital Supply Current – Operating (10k Ω load line)		70	mA
Digital Power Supply Current – Power Down		2	mA
Analog Power Supply Current – Power Down		2	mA
Power Dissipation – Operating (Current • Nominal Supply)		750	mW
Power Dissipation – Power Down (Current • Nominal Supply)		10	mW
Power Supply Rejection (@ 1 kHz)†	40		dB

STATIC DIGITAL SPECIFICATIONS

(All tests performed at TBD logic levels)

	Min	Max	Units
High-Level Input Voltage (V_{IH})			
Digital Inputs	2.0	(VD+)+0.3	V
XTAL1/2I	2.4	(VD+)+0.3	V
Low-Level Input Voltage			

(V_{IL})	–0.3	0.8	V
High-Level Output Voltage (V_{OH})	2.4		V
Low-Level Output Voltage (V_{OL})		0.4	V
Input Leakage Current (GO/NOGO tested)	–10	10	µA
Output Leakage Current (GO/NOGO tested)	–10	10	µA

TIMING PARAMETERS

(All tests performed at TBD logic levels)

	Min	Max	Units
$\overline{WR}/\overline{RD}$ Strobe Width (t_{STW})	120		ns
$\overline{WR}/\overline{RD}$ Rising to $\overline{WR}/\overline{RD}$ Falling (t_{BWND})	180		ns
Write Data Setup to $\overline{WR}$ Rising (t_{WDSU})	22		ns
$\overline{RD}$ Falling to Valid Read Data (t_{RDDV})	0	70	ns
$\overline{CS}$ Setup to $\overline{WR}/\overline{RD}$ Falling (t_{CSSU})	50		ns
$\overline{CS}$ Hold from $\overline{WR}/\overline{RD}$ Rising (t_{CSHD})	0		ns
Adr Setup to $\overline{WR}/\overline{RD}$ Falling (t_{ADSU})	22		ns
Adr Hold from $\overline{WR}/\overline{RD}$ Rising (t_{ADSU})	32		ns
$\overline{DAK}$ Rising to $\overline{WR}/\overline{RD}$ Falling (t_{SUDK1})	60		ns
$\overline{DAK}$ Falling to $\overline{WR}/\overline{RD}$ Rising (t_{SUDK2})	0		ns
$\overline{DAK}$ Setup to $\overline{WR}/\overline{RD}$ Falling (t_{DKSU})	25		ns
Data Hold from $\overline{RD}$ Rising (t_{DHD1})	0	20	ns
Data Hold from $\overline{WR}$ Rising (t_{DHD2})	25		ns
DRQ Hold from $\overline{WR}/\overline{RD}$ Falling (t_{DRHD})	0	25	ns

$\overline{DAK}$ Hold from $\overline{WR}$ Rising (t_{DKHDa})	155		ns
$\overline{DAK}$ Hold from $\overline{RD}$ Rising (t_{DKHDb})	100		ns
$\overline{DBEN}$/DBDIR delay from $\overline{WR}$/$\overline{RD}$ Falling (t_{DBDL})	0	30	ns

CLOCK SPECIFICATIONS†

	Min	Max	Units
Input Clock Frequency		27	MHz
Maximum Allowed Input Clock Jitter		±50	ps
Maximum Output Clock Jitter		±5	ns
Initialization / Sample Rate Change Time			
16.9344 MHz Crystal Selected		70	ms
24.576 MHz Crystal Selected		90	ms

REVISION HISTORY

Rev. 1.1 is the first complete preliminary data sheet.

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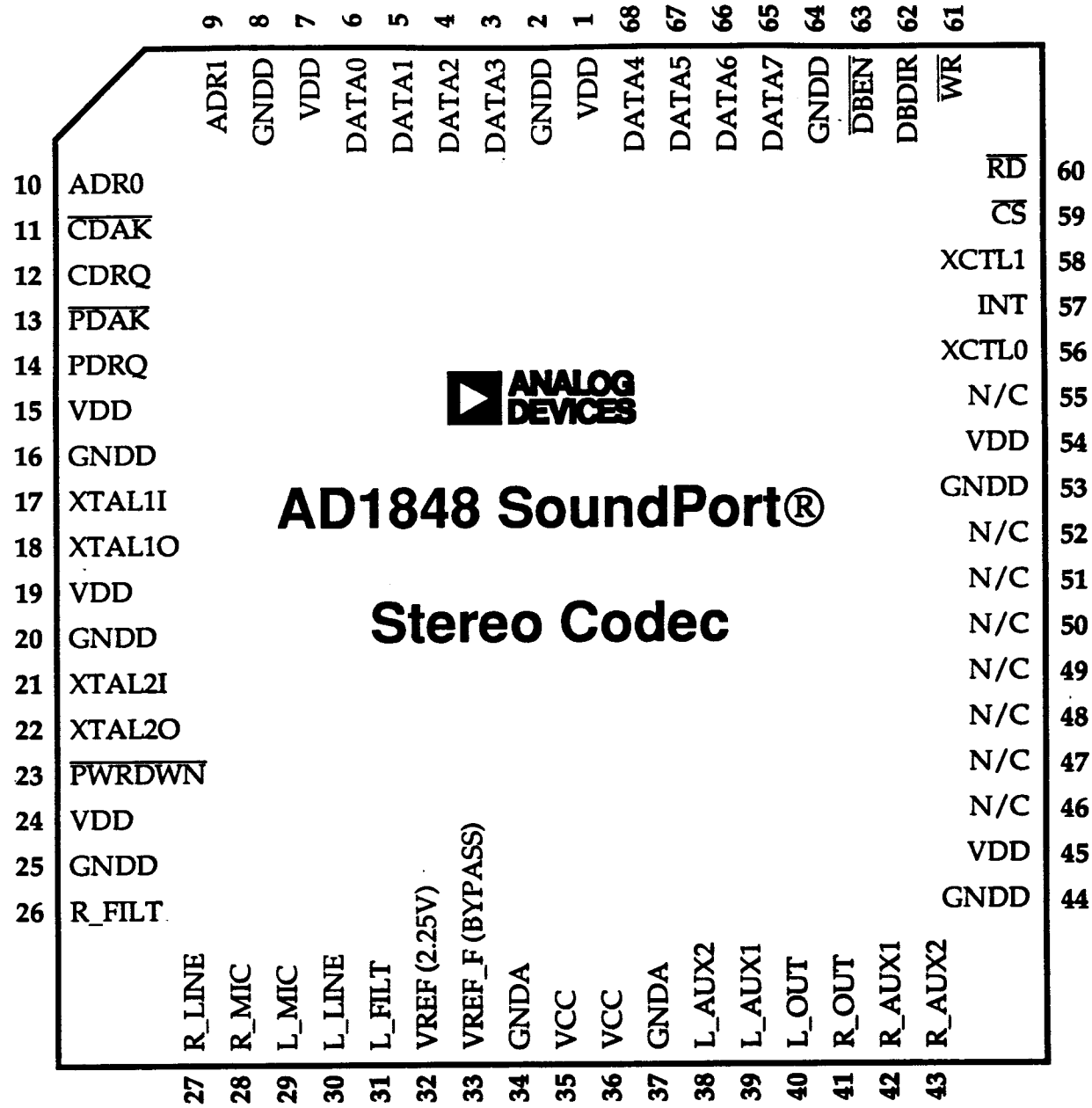
† Characterized, not tested



AD1848 Pinout
68-Lead PLCC

7/29/92