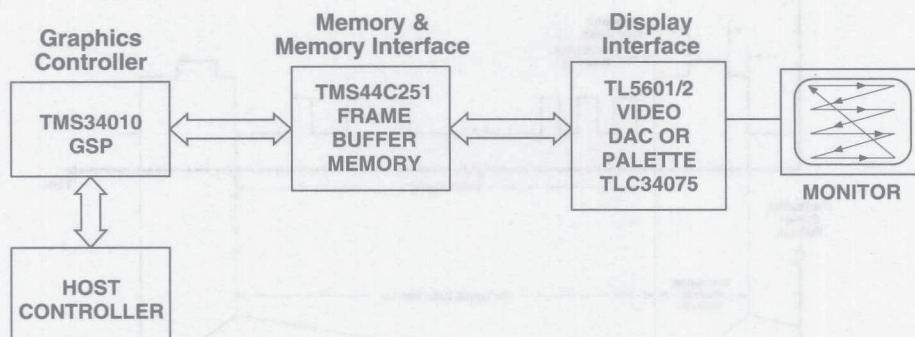


## Generic Graphics System



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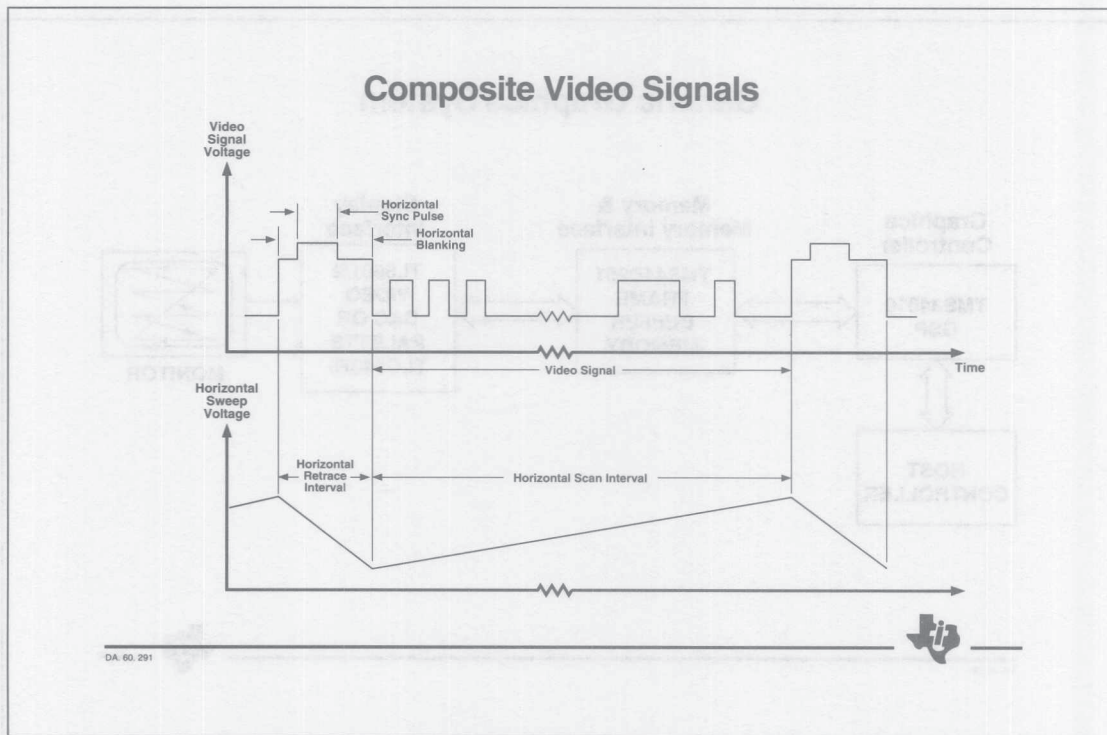


## 6 Graphics Systems

### Display Overview

The basic building blocks of image creation are a host processor, a graphics controller, the memory and memory interface, a display or monitor interface, and a CRT display monitor. The controller determines display timing, provides the image manipulation required, and stores the image in the memory. The video interface for driving a monochrome display is typically some form of digital-to-analog converter (DAC) that changes the digital data to analog voltages to drive the CRT. When color displays are used, the display interface is known as a color palette or video interface palette, which performs many more functions than a DAC.

Within the display monitor are the analog video amplifiers, the CRT grid drivers, sweep timing, and drive circuits. The inside of the CRT screen is coated with an array of phosphor dots (pixels) that emit light when struck by a beam of electrons from the CRT gun. Images are formed on a CRT screen when the electron beam sweeps horizontally across and vertically down the screen, striking the array of pixels one pixel at a time until it has successively swept through the entire array.



**Figure 34 - Composite Video Signals**

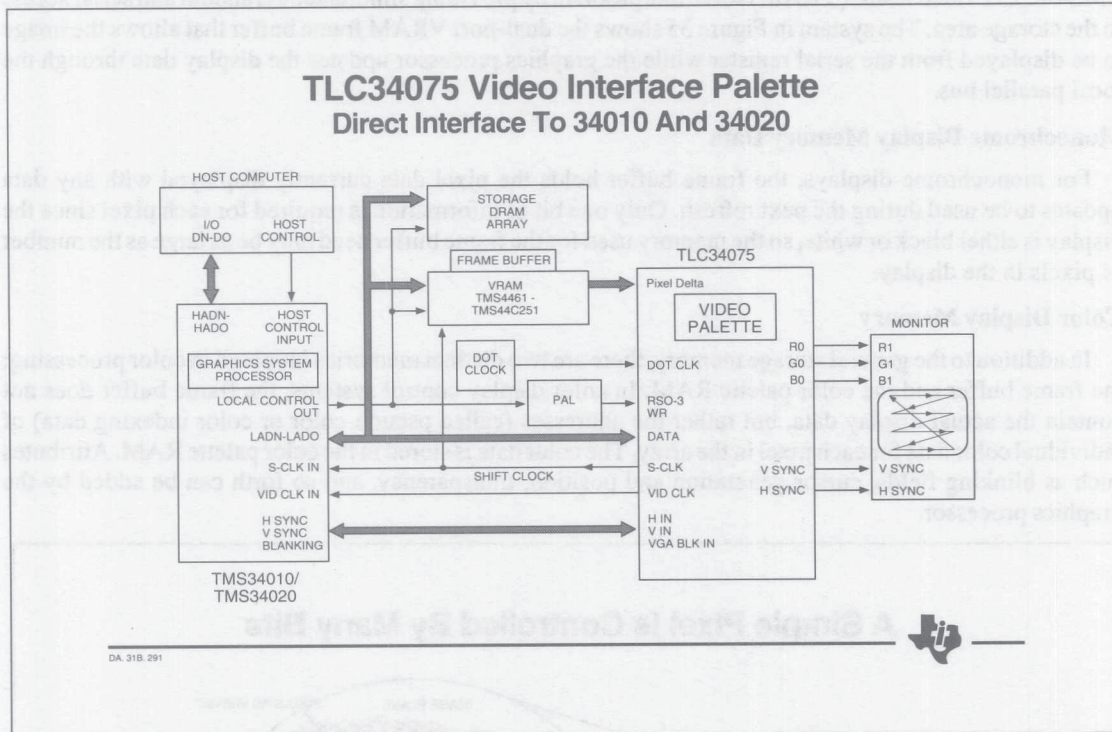
Return of the beam from right to left occurs during the horizontal retrace time and from bottom to top during the vertical retrace time. During the retrace, the screen is blanked by the horizontal and vertical blanking pulses. This horizontal and vertical (H and V) sweeping of the beam is called raster scanning and is the most widely used display method mainly because it can control bit-mapped graphics. The visual display created by this scanning method is called the raster. As shown for the horizontal sweep in Figure 34, the V & H sync pulses assure the proper beam start position on the screen for each scan. The sync pulses occur during the corresponding V or H blanking interval, which is also the beam retrace time. Of course, all horizontal lines are scanned between vertical sync pulses. Also, during the beam scanning, the individual pixel data is sequentially timed with the beam position by the video clock such that the image appears in the proper screen location. The brightness of the screen is determined by the intensity of the beam with the intensity controlled by the video amplifier output to the control grids of the CRT. If the beam intensity is kept constant during horizontal and vertical scan periods, the entire screen is a uniform brightness. The phosphor persistence retains the image for the duration of the vertical scan time such that an entire screen image is maintained. However, since the display will fade with time, the pixel array must be refreshed periodically to prevent the image from flickering. Flicker is the noticeable dimming of the screen image just prior to a display refresh. Most display systems refresh the screen on every vertical scan to prevent this condition. Typical refresh rates used are 60 Hz and 72 Hz.

### **Color CRT Displays**

In color monitors there are three separate channels: one for red data, one for blue data, and one for green data. The face of the CRT has a red array, a blue array, and a green array that are bombarded by beams from three CRT guns through three control grids. A metal mask inside the CRT face ensures that the proper beam



goes only to the corresponding red, blue, or green pixel array. The input color data is fed to three video amplifiers and then to an interface circuit that level-shifts the signals to the proper grid signal level (the LM1203 is an example of the video amplifiers commonly used). By varying the three beam intensities independently, this color data representing the three primary colors could theoretically reproduce any color desired. Equal red, green and blue data would produce a white to dark gray raster depending on the intensity level supplied by the video amplifiers.



**Figure 35 - A Color Graphics System Graphics Display System**

The generation and manipulation of bit-mapped images in memory is the primary function of a graphics display system. Figure 35 is a diagram of a color graphics system, showing the basic signal connections between the four basic elements of the system: the graphics controller, the frame buffer and general-purpose memory, the video color palette, and the monitor. The graphics controller offloads the host processor of the routine display tasks by handling the data updates and bit manipulation and synchronizing functions for the screen display. The host, however, can directly access the graphics processor, the frame buffer memory, or the video color palette when necessary to input new data or request status.

### The Frame Buffer

The information used to update the display during refresh is stored in memory. That area of memory reserved for a full frame of information is called the frame buffer. For monochrome displays, the frame buffer need only have one bit of information for each pixel. For high-quality color displays, the information for each pixel may contain several bytes of data. In these higher-performance systems, the memory size can be quite large and DRAM-type memory, due to its cost and physical size advantages, is used to implement the frame buffer. The standard DRAMs, however, have only one access port and can either be

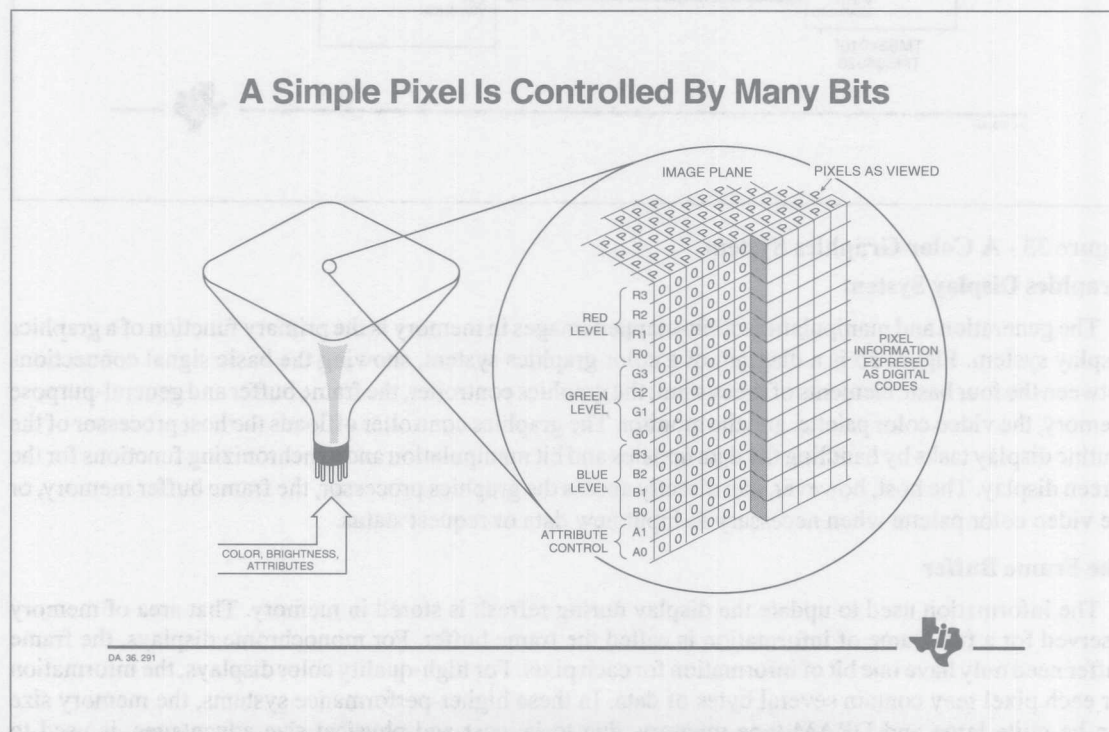
written to or read from at any point in time but not both. This type of memory access is too slow for high-performance graphics systems because the screen display must be interrupted for the frame buffer to be updated unless the updates can be inserted into the retrace time. Updating the frame buffer during retrace, however, would require a much faster clock speed and memory access time because the retrace time is only 25% of the total display period. Even if External dual-port logic were used, the DRAM access time would have to be very fast. Such fast DRAMs are costly and usually power hungry. Multiport devices such as the TMS44C251 video RAM (VRAM) solve this problem by providing simultaneous random and serial access to the storage area. The system in Figure 35 shows the dual-port VRAM frame buffer that allows the image to be displayed from the serial register while the graphics processor updates the display data through the local parallel bus.

### Monochrome Display Memory Data

For monochrome displays, the frame buffer holds the pixel data currently displayed with any data updates to be used during the next refresh. Only one bit of information is required for each pixel since the display is either black or white, so the memory used for the frame buffer need only be as large as the number of pixels in the display.

### Color Display Memory

In addition to the general storage memory, there are two distinct memories involved in color processing: the frame buffer and the color palette RAM. In color display control systems, the frame buffer does not contain the actual display data, but rather the addresses (called pseudo-color or color indexing data) of individual color data for each pixel in the array. The color data is stored in the color palette RAM. Attributes such as blinking fields, cursor generation and position, transparency, and so forth can be added by the graphics processor.



**Figure 36 - Color Data Required for an Individual Pixel**



An example of the color data required for an individual pixel is shown in Figure 36 as four bits each of red, green, and blue data per pixel with two attribute bits similar to EGA. Only four bits per color are shown for clarity. Higher-resolution display systems such as VGA and beyond use eight bits per color, and intensity data is usually coded into these eight bits. The color palette RAM usually exists as part of the video interface palette; however, it can also be external memory. The TLC34075 Video Interface Palette (VIP) has an on-board 256-by-24-bit palette RAM and is directly accessible by the host. This organization allows up to 256 colors to reside in the VIP palette RAM at any one time. The 24 bits are composed of a red data byte, a green data byte, and a blue data byte. As required by the application, the 256 colors are loaded into the palette RAM, usually by the host processor. When the palette RAM is addressed, it outputs the appropriate three bytes of data to the individual red, green, and blue video converter channel. If all eight bits are significant for each of the red, green, and blue colors, over 16 million ( $2^8 \times 2^8 \times 2^8$ ) colors would be available selected 256 at a time. The 256 selected colors or the later selection of 256 new colors is application-specific.

For what is known as *true color* display, a color palette memory would also contain eight bits of information for each of the red, green, and blue colors but would have the dimensions of at least 16M by 24. Instead of only 256 colors, this memory organization would allow any one of the 16 million colors to be displayed at any pixel during the display scan. The total number of colors, however, shown on a given screen is limited to the total number of pixels on the screen. For example, a 1024-by-768-pixel array can only display 786,432 colors at one time, but on the next refresh could display another 786,432 colors and so on up to a total of 16 million.

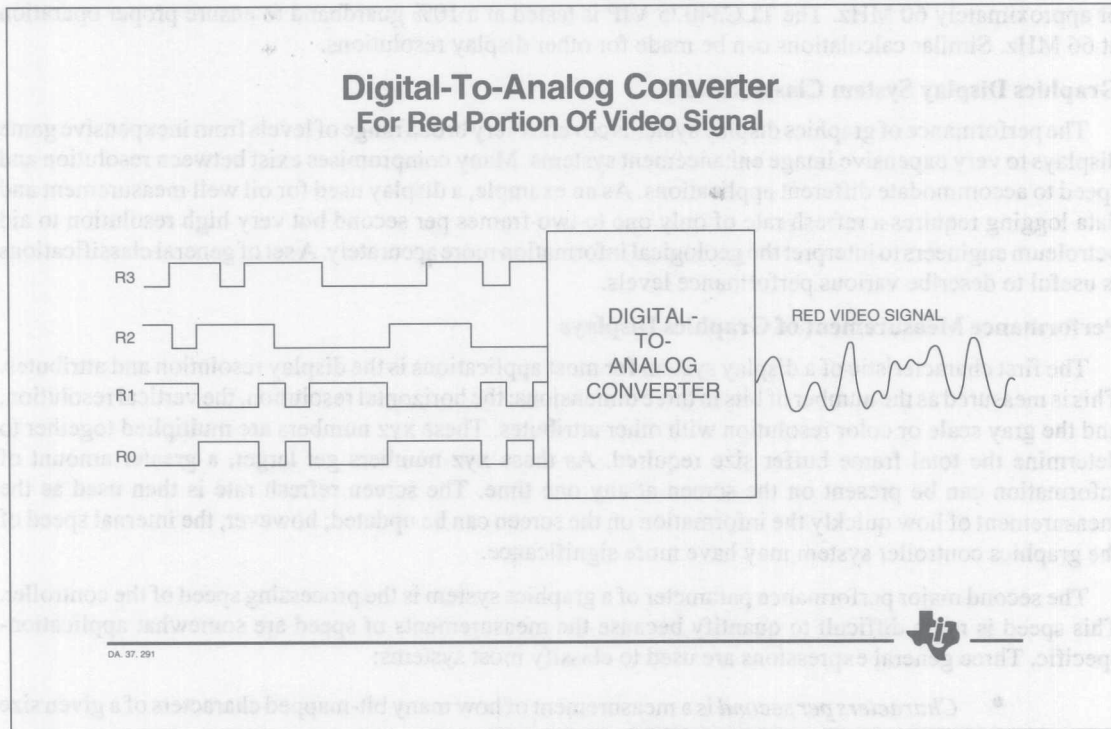


Figure 37 - Output Digital-to-Analog Converter (DAC)



### Color Output to the Monitor

Color and brightness can only be displayed by a CRT monitor if they are in the form of a continuously variable voltage. Therefore, the digital information stored in the frame buffer or palette memory must be converted to voltage levels that can be used by the monitor. This is the function of the output digital-to-analog converter (DAC) shown in Figure 37. Since color is represented as a mix of the three primary colors red, green and blue, there is a DAC output for each of these. Most RGB monitors accept signals that have a 75- $\Omega$  characteristic impedance. The analog output circuits must be able to drive this impedance to ensure that the video signal is transferred to the monitor with the proper voltage levels. The TLC34075 VIP integrates this video output capable of driving video signal levels into a doubly balanced 75- $\Omega$  line according to the RS-343A video output specification.

### Calculation of the Required Dot Clock Frequency

The refresh rate and the display resolution determine the dot clock frequency. For example, assume a display resolution of 1024 by 768 pixels and a vertical period of 1/60 second. Since all pixels need to be refreshed in that interval, then the total number of pixels to be refreshed in 1/60 second is  $1024 \times 768 = 786,432$  pixels. Within the vertical period, however, the vertical blanking uses about 25% of the total time and cannot be used for refresh. Therefore, the pixel or dot clock frequency is

$$f(\text{dot}) = \frac{\text{total no. of pixels}}{(1/60) \text{ second}} \times 1.25 = 786,432 \times 60 \times 1.25 \text{ Hertz} = 58.98 \text{ MHz}$$

or approximately 60 MHz. The TLC34075 VIP is tested at a 10% guardband to ensure proper operation at 66 MHz. Similar calculations can be made for other display resolutions.

### Graphics Display System Classification

The performance of graphics display systems covers a very broad range of levels from inexpensive game displays to very expensive image enhancement systems. Many compromises exist between resolution and speed to accommodate different applications. As an example, a display used for oil well measurement and data logging requires a refresh rate of only one to two frames per second but very high resolution to aid petroleum engineers to interpret the geological information more accurately. A set of general classifications is useful to describe various performance levels.

### Performance Measurement of Graphics Displays

The first characteristic of a display system for most applications is the display resolution and attributes. This is measured as the number of bits in three dimensions: the horizontal resolution, the vertical resolution, and the gray scale or color resolution with other attributes. These xyz numbers are multiplied together to determine the total frame buffer size required. As these xyz numbers get larger, a greater amount of information can be present on the screen at any one time. The screen refresh rate is then used as the measurement of how quickly the information on the screen can be updated; however, the internal speed of the graphics controller system may have more significance.

The second major performance parameter of a graphics system is the processing speed of the controller. This speed is more difficult to quantify because the measurements of speed are somewhat application-specific. Three general expressions are used to classify most systems:

- *Characters per second* is a measurement of how many bit-mapped characters of a given size can be generated from ASCII in one second.
- *Vectors per second* is a measurement of how many dotted lines can be plotted on the screen per second from vector or x-y coordinate information.




- *Polygon generation speed* is useful in some applications if the same type of polygon is used to compare various systems. Lower-cost systems may not generate polygons at the graphics processor level but rely on the host processor to calculate the component line position to build the polygon.

The processing performance requirements for an application depend on the intended end use of the display and the specific timing characteristics of the CRT that are chosen for a design.

## TLC34075 Video Interface Palette

**Features:**

|   |   |
|---|---|
| <ul style="list-style-type: none"> <li>• Versatile Multiplexing Interface Allows A Lower Bus Rate</li> <li>• Direct VGA Pass-Through Capability</li> <li>• Directly Interfaces To TMS34010/34020</li> <li>• 66MHz, 85MHz, 110MHz, And 135MHz Versions</li> <li>• Triple 8-Bit D/A Converters</li> <li>• 256 Word Color Palette RAM</li> <li>• Palette Page Register</li> <li>• RS-343A Compatible Outputs</li> <li>• LinEPIC 1um CMOS Process</li> <li>• 84 Pin PLCC</li> </ul> | <ul style="list-style-type: none"> <li>• TTL Compatible Inputs</li> <li>• Standard MPU Interface</li> <li>• Pixel Word Mask</li> <li>• On-Chip Clock Selection</li> <li>• "True Color" (Direct Addressing) Mode</li> <li>• Direct Interfacing To Video RAM</li> <li>• Support For Split Shift Register Transfers</li> <li>• Software Downward Compatible With IMSG1768 &amp; BT467/8 (VGA)</li> <li>• TIGA Software Compatible</li> </ul> |
|---|---|

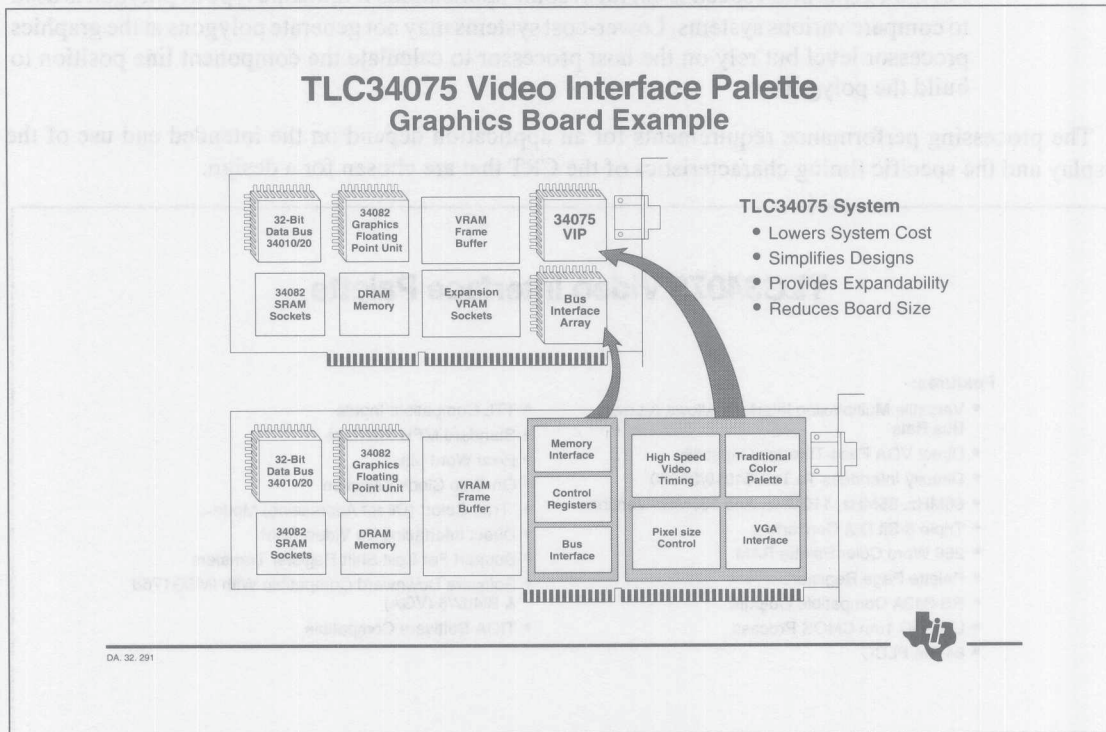


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**Figure 38**

### Beyond VGA — The TLC34075

Traditionally, the graphics board designer has had, among others, the following major considerations: 1) RF noise suppression, 2) maximum signal skew allowable, and 3) functional flexibility for working with various screen resolutions and data formats required for upward or downward compatibility with other systems. The features of the TLC34075 Video Interface Palette (VIP), which addresses these and other design considerations, are shown in Figure 38.



**Figure 39**

The TLC34075 reduces RF noise and signal skew by incorporating all of the high-speed timing, synchronizing, and multiplexing logic usually associated with graphics systems into one device, greatly reducing board chip count as shown in Figure 39. Since all high-speed signals (excluding clock source) are contained on chip, RF noise and signal skew are greatly reduced for the designer.

The TLC34075's various pixel multiplexing options allow for 32-, 16-, 8-, and 4-bit pixel buses to be accommodated without any circuit modification, enabling the system to be easily reconfigured for varying amounts of available video RAM. Data can be split into 1-, 2-, 4-, or 8-bit data lengths to accommodate differing system requirements. This data is used to address a 256-by-24 color lookup table, and the color lookup data drives triple 8-bit DACs.

The device features a separate VGA bus that allows data from the feature connector of most VGA-supported personal computers to be tied directly into the palette without the need for external data multiplexing. This allows a replacement graphics board to remain downward compatible by using the existing graphics circuitry often located on the motherboard.

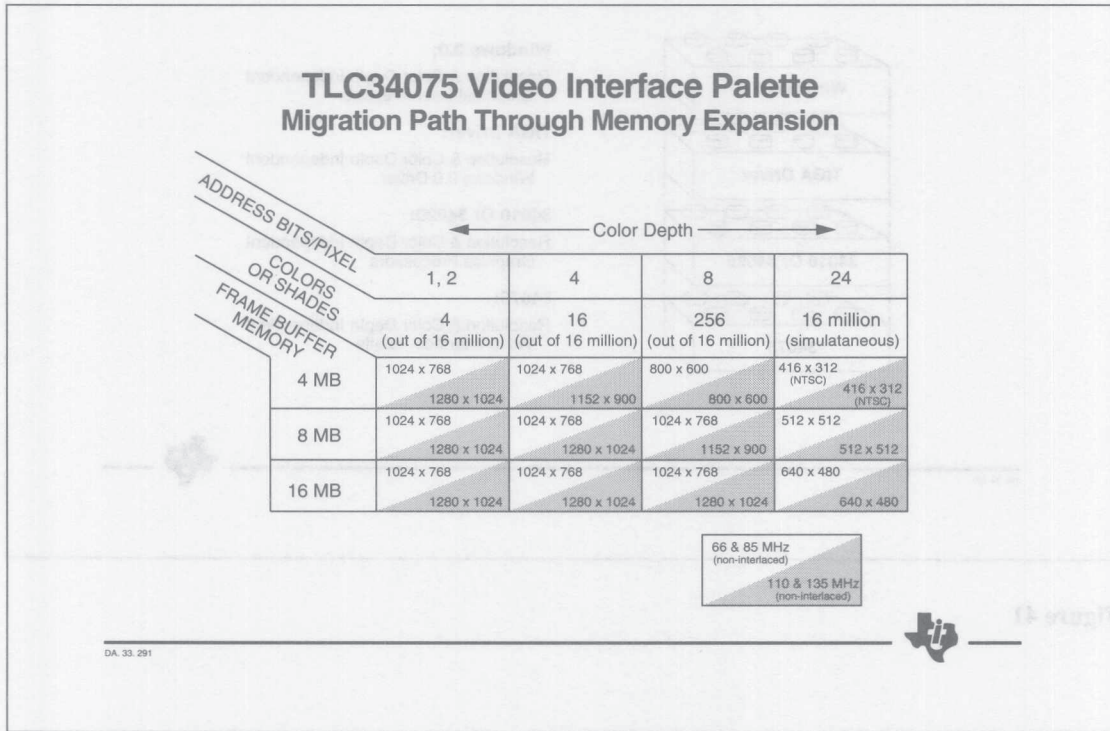
Sync generation is incorporated on the green output channel. HSYNC and VSYNC are fed through the device and optionally inverted to indicate screen resolution to the monitor.

Clocking is provided by one of four (3 TTL and 1 ECL/TTL) software-selectable inputs to support various screen resolutions. The TLC34075 can be connected directly to the serial port of VRAM devices, eliminating the need for discrete logic. It will also support split shift register transfers (SSRT). Split shift register transfers allow more efficient use of the available VRAM.



A palette page register provides additional bits of palette address when 1-, 2-, or 4-bit transfers are used. This paging feature allows the screen colors to be changed with only one MPU write cycle.

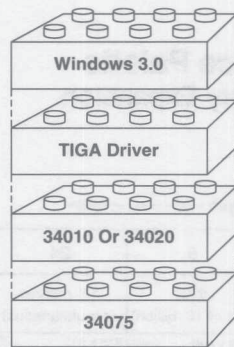
A true color mode transfers 24 (3 × 8) bits of color information from the pixel port directly to the DACs. In this mode, the remaining 8 bits (of 32 total) on the pixel bus provide an overlay function.



**Figure 40**

Figure 40 shows the size of the frame buffer memory required to support a given resolution.

## TI's Hardware And Software Plug-And-Play Together To Unleash The Power Of Windows 3.0



**Windows 3.0:**  
Resolution & Color Depth Independent  
Graphical User Interface

**TIGA Driver:**  
Resolution & Color Depth Independent  
Windows 3.0 Driver

**34010 Or 34020:**  
Resolution & Color Depth Independent  
Graphics Processors

**34075:**  
Resolution & Color Depth Independent  
Video Interface Palette

DA 34 291



Figure 41



## TLC34058 – 256 x 12 Or 24 Color Palette

### Key Features:

- RS-343 Compatible Outputs
- Direct Interface To TMS340XX Graphics Processors
- 125 MHz Pipelined Architecture
- Direct Replacements For The Brooktree Bt458

### Customer Benefits

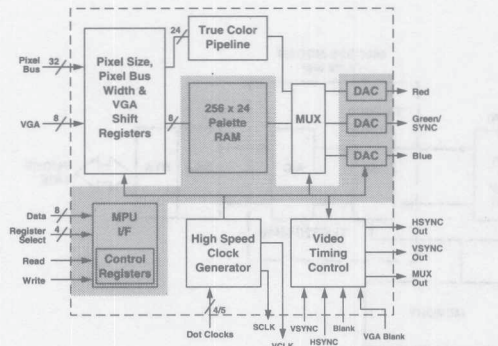
- Industry Standard Output for Direct Interfacing With External Circuits
- Simplifies Layout And Interconnection For Compactness And Reliability
- Fast Display And Rewrite
- Second Source For Existing Designs

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Figure 58

## TLC34075 Video Interface Palette Functional Block Diagram



- 256 Color Palette
- VGA Palette Register Compatible
- Direct VGA Pass-Through
- Monitor Detection
- Directly Supports 1, 2, 4, 8, 24 Bits Per Pixel
- Programmable Pixel Bus Widths - 4, 8, 16 & 32
- Direct Interface to VRAM
- On-Chip Shift Registers
- On-Chip Dot Clock Mux
- On-Chip DAC Reference
- SYNC On Green

The TLC34075 VIP Supports High Resolution Graphics While Providing Backward Compatibility For VGA  
The White Areas Show the Additional Functionality of the "TLC34075" Over the Standard Color Palette (in grey).

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Figure 59