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FDDI on Copper with AMD PHY Components

by Eugen Gershon

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INTRODUCTION

This application note outlines an implementation using AMD PHY components found in either the SUPERNET 1 or SUPERNET 2 families to drive and receive signals over shielded twisted pair media. The circuit described meets the electrical specification of the interoperable solution (PID 16011A) endorsed by AMD, Chipcom, DEC, Motorola, and SynOptics. This interoperable solution (IOS) is designed to minimize the cost of FDDI connections confined within 100 meter range by replacing the optical transceiver and fiber with a shielded twisted pair (STP) transceiver and STP cabling. If a design utilizes AMD's SUPERNET 1 or SUPERNET 2 chipsets, no major changes are required; only a simple interface circuit from the PHY transmitter to the cable and another interface from the cable to the PHY receiver are necessary. The interface can be implemented at minimal cost and with no more board space requirements than available optical Media Interface Connectors (MICs). We built the circuit described herein using surface mount devices on a small daughter board that was form factor and pin-out compatible with the MIC device found on one of our demonstration platforms.

When optical PMD devices are removed from the board, the signals at their interface to the system should be kept intact, both in logical content and as voltage/current levels – see Figure 1. The optical transmitter accepts both "Serial Data Out" from the PHY transmitter and "Output Disable" control (not used in IOS), at P-ECL levels. Similarly, the optical receiver supplies "Serial Data In" to the PHY receiver and "Carrier Detect" status (here called "Link Detect") at the same P-ECL levels. One new signal handled by the copper interface circuit is a status signal, incorporated into Link Detect, that shows that the cable is connected at both ends. It is detected by both transmitter and receiver because each one uses a separate twisted pair.

This solution is designed to work on STP cable, 150 ohm, Type 1 or 2. It specifies a maximum FDDI signal attenuation of 12 dB (a factor of 4) at 100 meters.

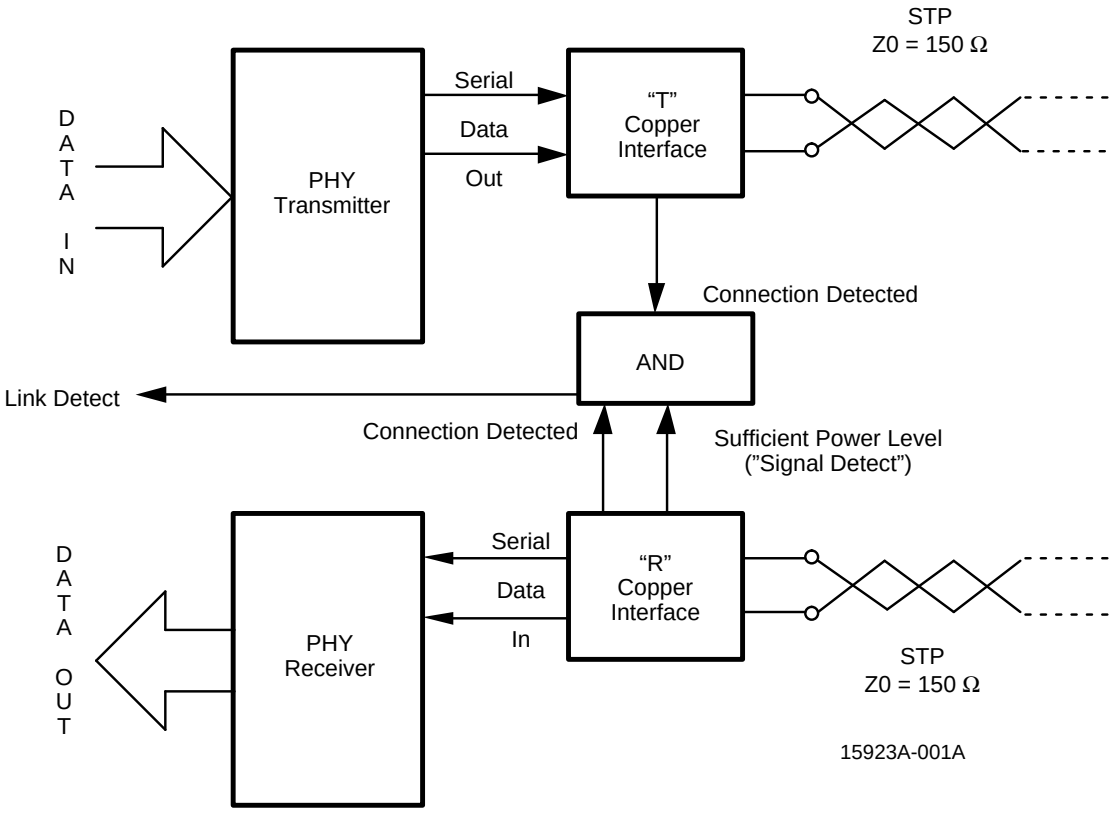

Figure 1. Block Diagram

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The transmit waveform going to the cable is required to meet a template based on a differential P-ECL output waveform, such as at the PDT (ENDEC) outputs. This means that AMD parts can be used to drive the STP cable directly (source terminations should be added as required by the IOS specifications). Also, the attenuated signal coming out of the cable at the receiver end is sufficient to allow clock and data recovery by the PDR (EDS) without any need for amplification.

Transmitter Interface

The main coupling component to the cable is a transformer, which should be designed for the speed (rise and fall time) and the frequency spectrum of the FDDI signal. Figure 2 shows the data path. The transformer shown is a 1:1 transformer with center taps made by Pulse Engineering, Inc. R1 and R2 are biasing resistors for the output driver stage inside the PDT (ENDEC). The output voltages are roughly 3 volts for "LOW" and 4 volts for "HIGH", therefore the resistor values can be calculated from the average DC current: 3.5 V/R1 = 10 to 20 mA. R3 and R4 combined with the output impedance of the driver and with the transformer series impedance form the cable termination (150 ohms) at the transmitter end. R3 and R4 will reduce the output signal to the cable by a factor of two. The PDT output driver sees a differential impedance of about 300 ohms in parallel with the 540 ohm biasing resistors. This requires less than its full driving capability of 100 ohms differential.

IOS specifies no precompensation at the transmitter end in order to minimize high frequency power levels in the transmitted signal spectrum, which improves the FCC-related performance.

Receiver Interface

The main coupling component at the receiver end is also the transformer. Figure 3 shows the data path. R4, R5 and R6 are bias resistors to bring the input stage of the PDR (EDS) to its DC operating point of about 3.5 volts. R5 provides a small offset voltage between RX and RY to keep the inputs (and outputs) stable in the absence of a carrier. The bias voltage level is isolated from the transformer secondary by C3 and C4. It is also possible to include the transformer in the DC path in order to avoid the need for capacitors C3 and C4. In this case a two-transformer option is a better choice. The R1, R2 and R3//R5 combination, and the parallel loading of Link Detect (not shown) give the proper cable termination at the receiver end (150 ohms). R1 and R2 with their parallel capacitors C1 and C2 form a high-pass filter that compensates for the high-frequency attenuation and phase shift in the cable. There are many possible correct schemes for compensation. AMD's parts can run a 100 meter link without compensation in most cases, provided the signal is not deteriorated by low performance transformers or external noise. However, in the interest of providing a robust implementation over the IOS specification, compensation has been included.

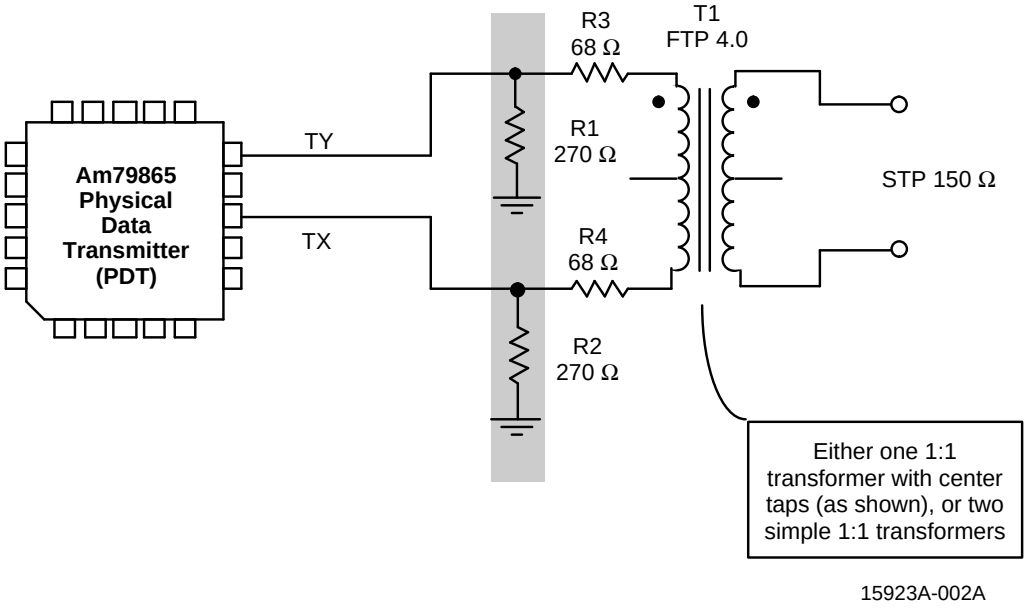

Figure 2. Transmitter Interface for Data Out

Cable Continuity Detection

As mentioned before IOS requires a DC path to check cable connection between two (“master” and “slave”) stations. The cable continuity signal is one part of “Link Detect” status, which is comprised of both cable continuity and minimum signal level.

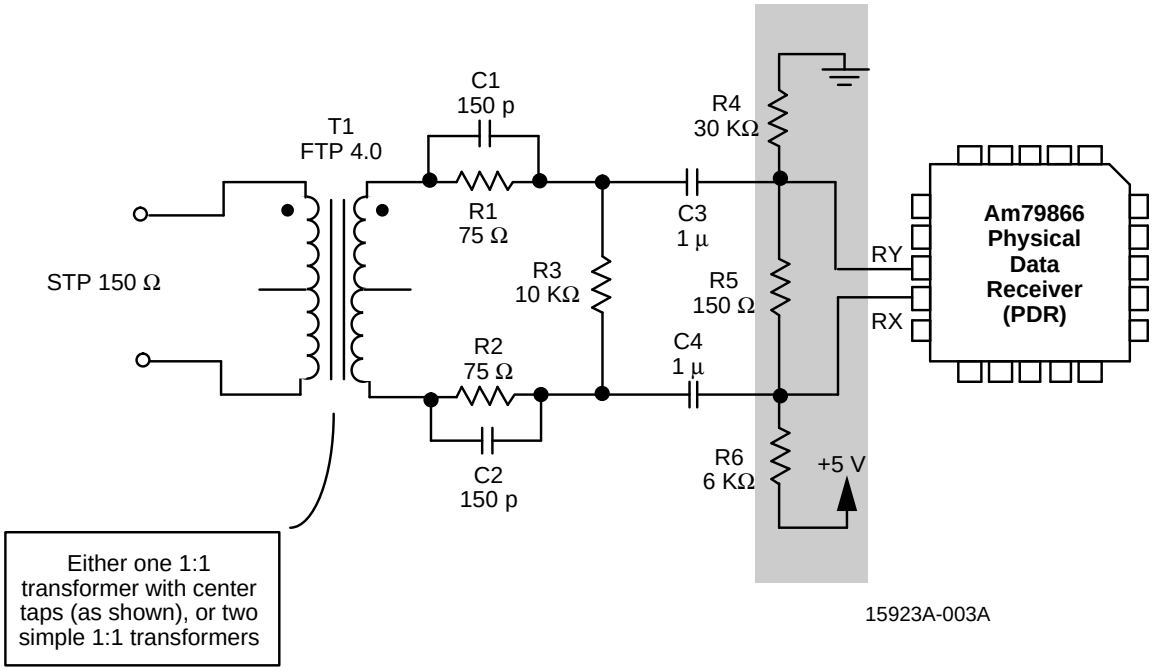

Figure 3. Receive Interface for Data In

Figure 4 shows the required DC path for which there are two interoperable options. The simpler of the two solutions (shown) reports continuity if at least one of the wires in the twisted pair is connected. The second option requires both wires to be connected in order to report continuity, but its implementation uses more components. For example, the second option requires two transformers at each twisted pair end and cannot be implemented with one center-tapped transformer. Both implementation options are shown in the IOS document, Appendix 1.

The S-port cable continuity test will signal a “high” at the emitter output or a “low” at the collector output when the cable is connected.

An M-port needs to check that the voltage across the resistor is within a “window”. A low voltage indicates no connection; a high voltage indicates a loop-back condition. In both cases cable continuity signal is “false.”

Signal Level Detection

The circuit for input signal level detection is based on a fast comparator. In Figures 5 and 6 the comparator is built from a 4 transistor amplifier and a peak detector. In Figure 7, a fast IC comparator is used. Other implementations are shown in the IOS document. If the input signal level is 50 mV or more peak-to-peak, and the cable is connected, the output level of Link Detect goes to “high” (4 volts).

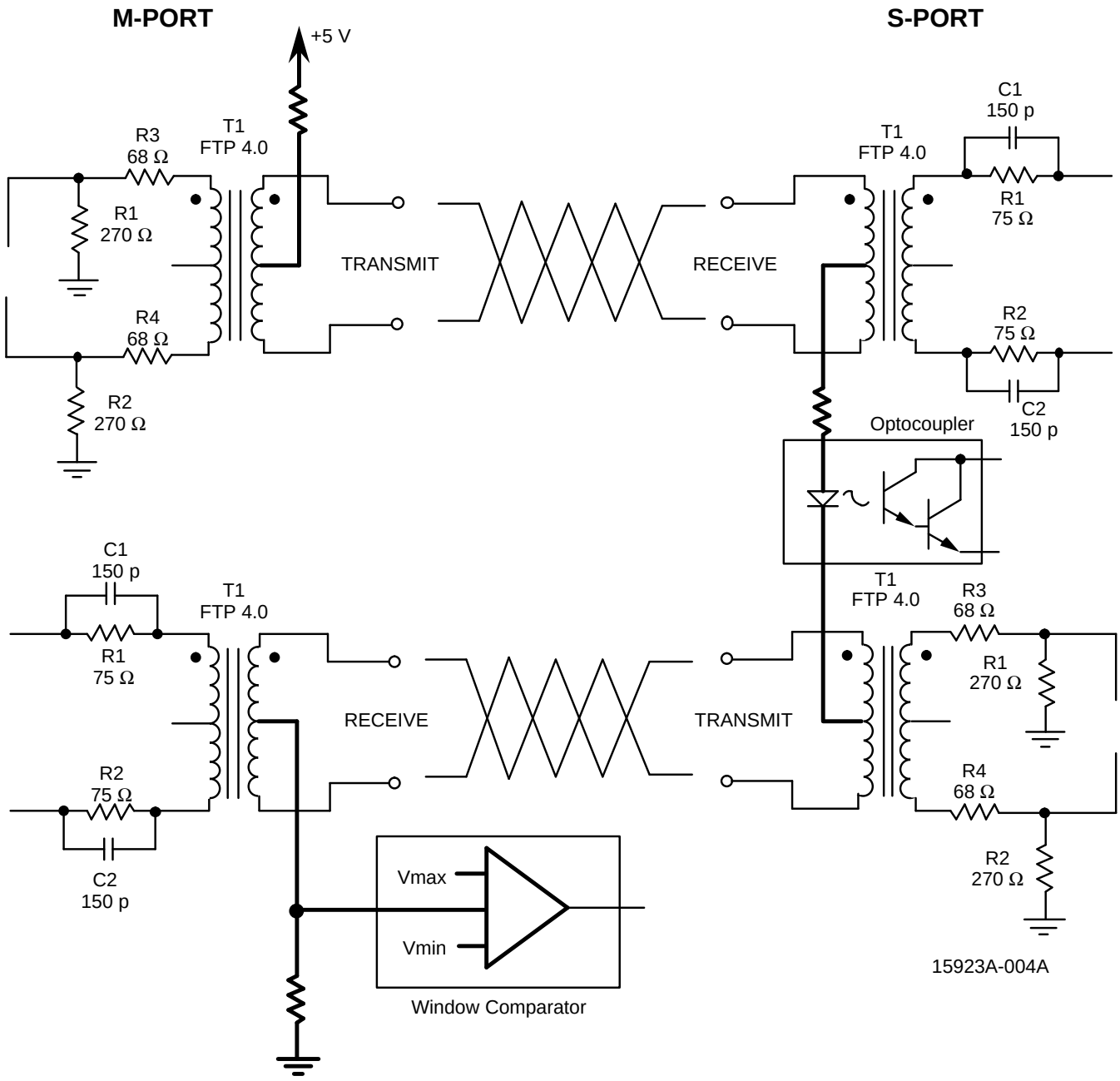

Figure 4. The Simple Option for Cable Continuity Detection

Lay-Out

During the time we have been experimenting with the copper interface, it has become apparent that one major source of problems is the computer noise coupled into the transmitted and received signals. Little serial inductors were added to the serial lines that come from the PDT or ENDEC (TX, TY), and go to the PDR or EDS (RX, RY), to filter high frequency components that do not belong to the FDDI signal.

The protoypes we have built for preliminary testing were based on FASTcards (ENDEC and EDS). The whole interface circuit, including data path, bias resistors and Link Detect, was plugged into the ODL footprint. The newer generation of FASTcards based on PDT/Rs will use exactly the same interface. Detailed schematics of an S-port and an M-port are shown in Figures 5 and 6 respectively.

Since FCC compliance is dependent on both the circuit characteristics and the system lay-out and configuration, test results will vary from implementation to implementation. However, the circuit includes noise suppressing elements to minimize EMI.

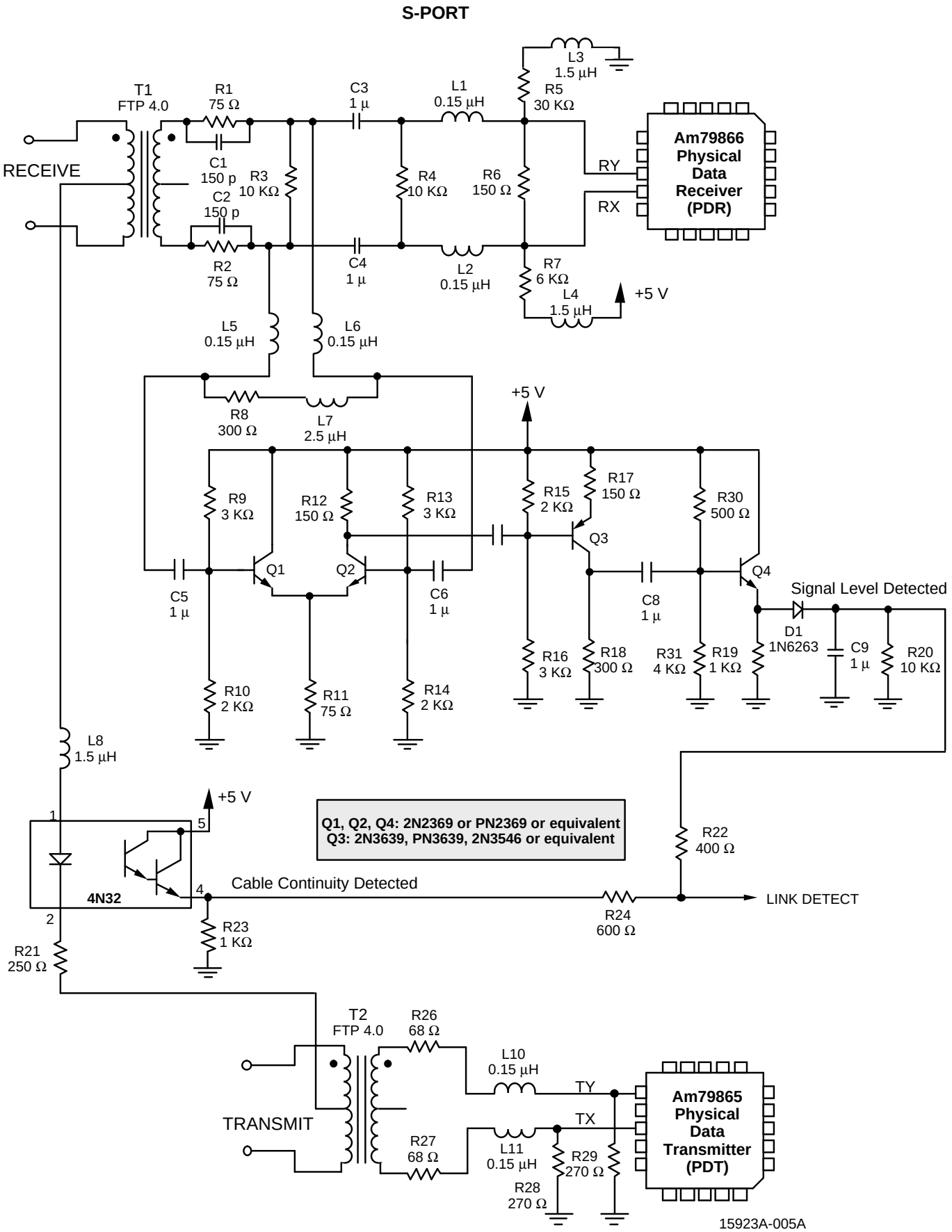

Figure 5. Schematic For the S-Port

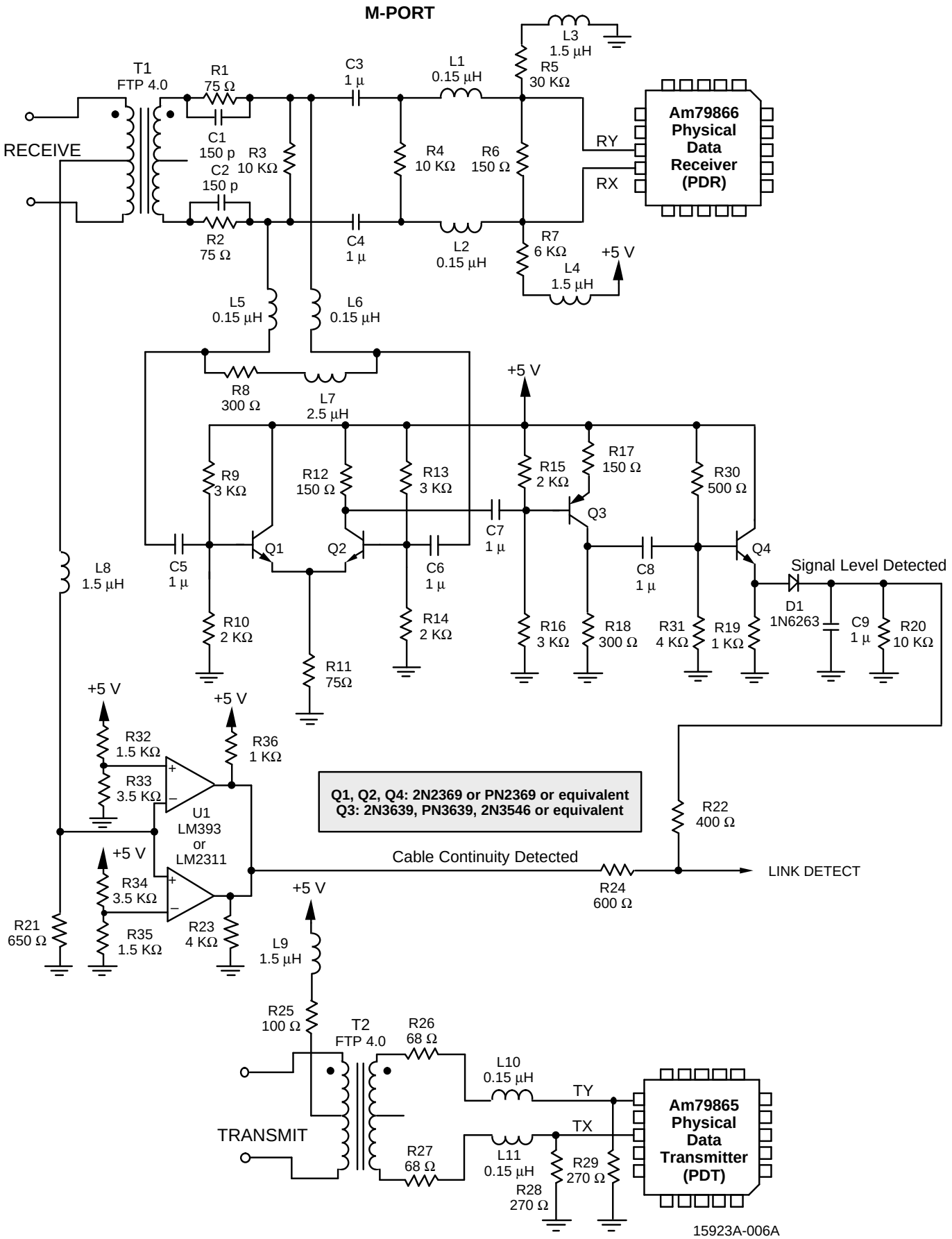

Figure 6. Schematic For the M-Port

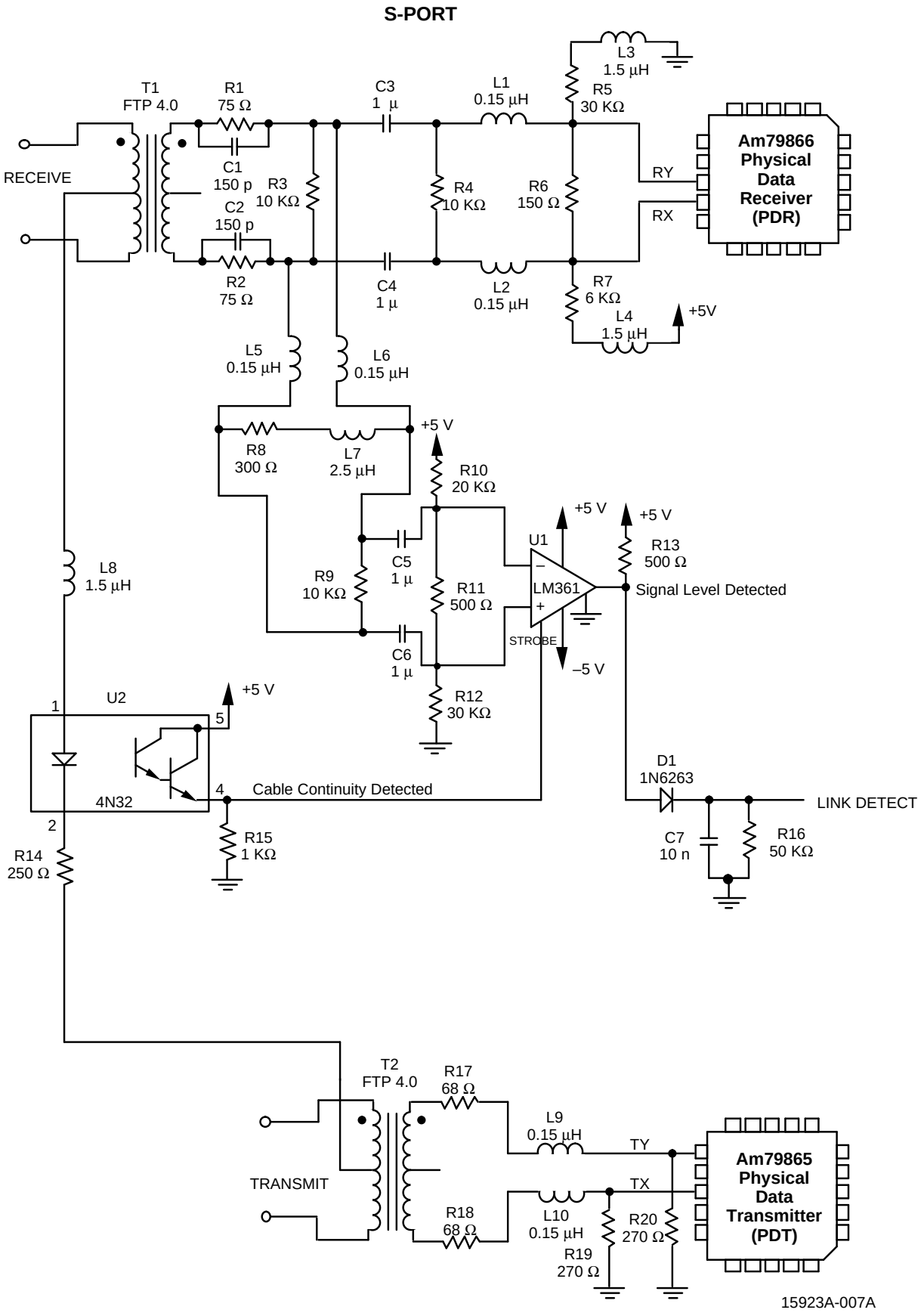

Figure 7. Alternative Schematic For the S-Port Using a Fast Comparator For Signal Detect