HS-80C86RH

Radiation Hardened 16-Bit CMOS Microprocessor

September 1995

Features

- **Radiation Hardened**
  - **Latch Up Free EPI-CMOS**
  - **Total Dose >100K RAD (Si)**
  - **Transient Upset >10^8 RAD (Si)/s**
- **Low Power Operation**
  - **ICCSB = 500μA (Max)**
  - **ICCOP = 12mA/MHz (Max)**
- **Pin Compatible with NMOS 8086 and Intersil 80C86**
- **Completely Static Design DC to 5MHz**
- **1MB Direct Memory Addressing Capability**
- **24 Operand Addressing Modes**
- **Bit, Byte, Word, and Block Move Operations**
- **8-Bit and 16-Bit Signed/Unsigned Arithmetic**
  - **Binary or Decimal**
  - **Multiply and Divide**
- **Bus-hold Circuitry Eliminates Pull-up Resistors for CMOS Designs**
- **Hardened Field, Self-Aligned, Junction-Isolated CMOS Process**
- **Single 5V Power Supply**
- **Military Temperature Range -35°C to +125°C**
- **Minimum LET for Single Event Upset -6MEV/mg/cm^2 (Typ)**

Description

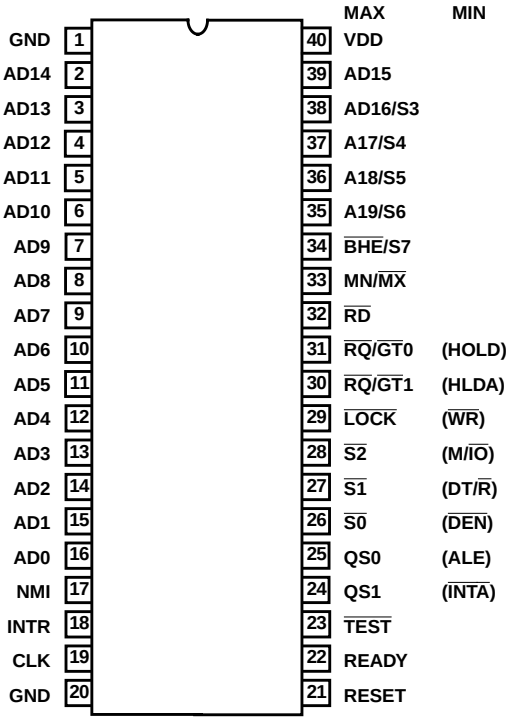
The Intersil HS-80C86RH high performance radiation hardened 16-bit CMOS CPU is manufactured using a hardened field, self aligned silicon gate CMOS process. Two modes of operation, MINimum for small systems and MAXimum for larger applications such as multiprocessing, allow user configuration to achieve the highest performance level. Industry standard operation allows use of existing NMOS 8086 hardware and software designs.

Ordering Information

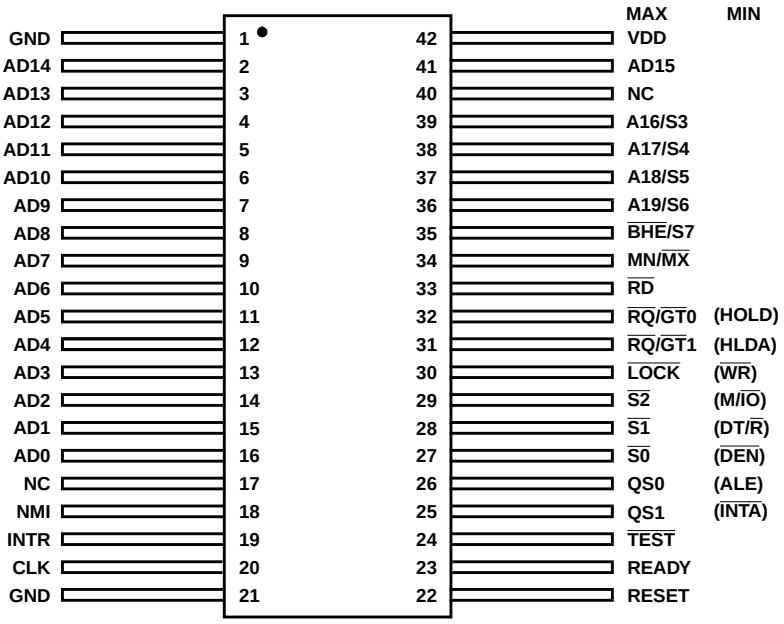
PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
HS1-80C86RH-8	-35°C to +125°C	Intersil Class B Equivalent	40 Lead Braze Seal DIP
HS1-80C86RH-Q	-35°C to +125°C	Intersil Class S Equivalent	40 Lead Braze Seal DIP
HS9-80C86RH-8	-35°C to +125°C	Intersil Class B Equivalent	42 Lead Braze Seal Flatpack
HS9-80C86RH-Q	-35°C to +125°C	Intersil Class S Equivalent	42 Lead Braze Seal Flatpack
HS9-80C86RH-SAMPLE	25°C	Sample	42 Lead Braze Seal Flatpack
HS1-80C86RH-SAMPLE	25°C	Sample	40 Lead Braze Seal DIP
HS9-80C86RH-PROTO	-35°C to +125°C	Prototype	42 Lead Braze Seal Flatpack
HS1-80C86RH-PROTO	-35°C to +125°C	Prototype	40 Lead Braze Seal DIP

Pinouts

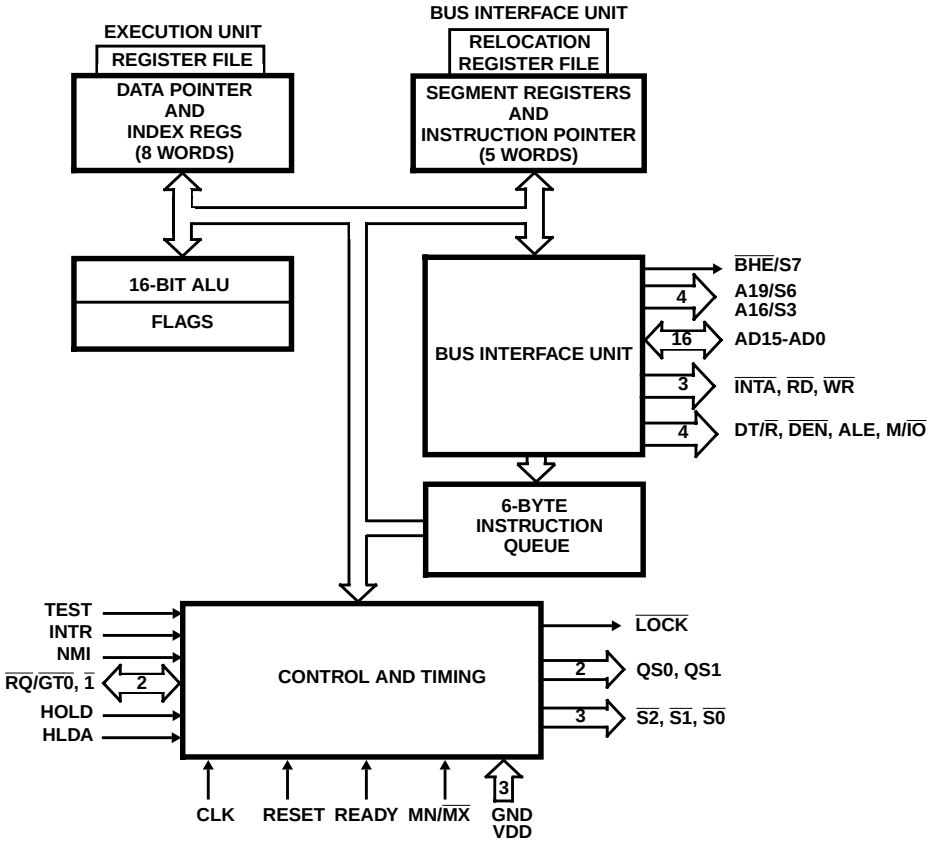
HS-80C86RH 40 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE (SBDIP)
MIL-STD-1835, CDIP2-T40
TOP VIEW

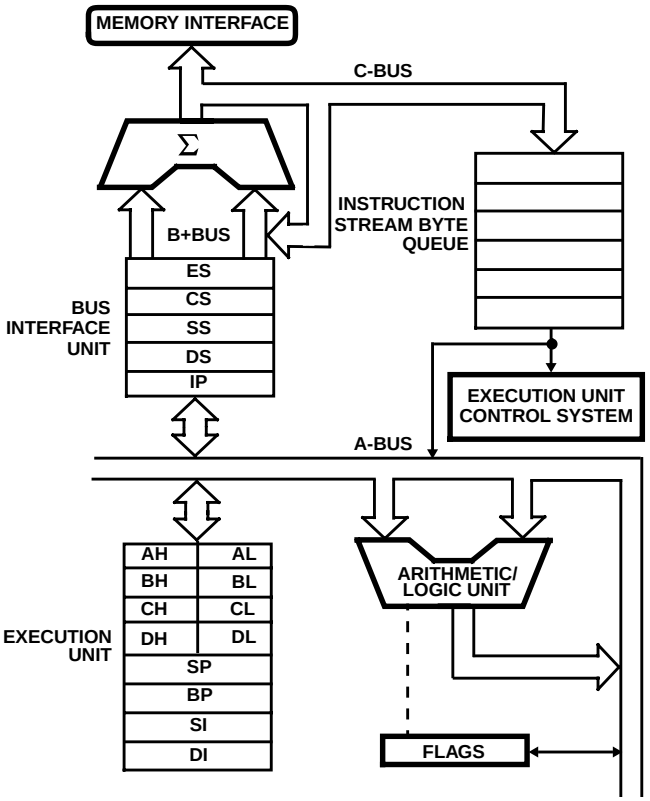


HS-80C86RH 42 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE (FLATPACK)
INTERSIL OUTLINE K42.A
TOP VIEW



Functional Diagram





Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
The following pin function descriptions are for HS-80C86RH systems in either minimum or maximum mode. The “Local Bus” in these descriptions is the direct multiplexed bus interface connection to the HS-80C86RH (without regard to additional bus buffers).			
AD15-AD0	2-16, 39	I/O	ADDRESS DATA BUS: These lines constitute the time multiplexed memory/IO address (T1) and data (T2, T3, TW, T4) bus. AO is analogous to $\overline{BHE}$ for the lower byte of the data bus, pins D7-D0. It is LOW during T1 when a byte is to be transferred on the lower portion of the bus in memory or I/O operations. Eight-bit oriented devices tied to the lower half would normally use AD0 to condition chip select functions (See $\overline{BHE}$). These lines are active HIGH and are held at high impedance to the last valid logic level during interrupt acknowledge and local bus “hold acknowledge” or “grant sequence”.
A19/S6 A18/S5 A17/S4 A16/S3	35-38	O	ADDRESS/STATUS: During T1, these are the four most significant address lines for memory operations. During I/O operations these lines are low. During memory and I/O operations, status information is available on these lines during T2, T3, TW, T4. S6 is always zero. The status of the interrupt enable FLAG bit (S5) is updated at the beginning of each CLK cycle. S4 and S3 are encoded. This information indicates which segment register is presently being used for data accessing. These lines are held at high impedance to the last valid logic level during local bus “hold acknowledge” or “grant sequence”. **S4** **S3** 0 0 Extra Data 0 1 Stack 1 0 Code or None 1 1 Data
$\overline{BHE}$/S7	34	O	BUS HIGH ENABLE/STATUS: During T1 the bus high enable signal ($\overline{BHE}$) should be used to enable data onto the most significant half of the data bus, pins D15-D8. Eight bit oriented devices tied to the upper half of the bus would normally use $\overline{BHE}$ to condition chip select functions. $\overline{BHE}$ is LOW during T1 for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the high portion of the bus. The S7 status information is available during T2, T3 and T4. The signal is active LOW, and is held at high impedance to the last valid logic level during interrupt acknowledge and local bus “hold acknowledge” or “grant sequence”; it is LOW during T1 for the first interrupt acknowledge cycle. **$\overline{BHE}$** **A0** 0 0 Whole Word 0 1 Upper Byte from/to Odd Address 1 0 Lower Byte from/to Even Address 1 1 None
$\overline{RD}$	32	O	READ: Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the M/$\overline{IO}$ or $\overline{S2}$ pin. This signal is used to read devices which reside on the HS-80C86RH local bus. $\overline{RD}$ is active LOW during T2, T3 and TW of any read cycle, and is guaranteed to remain HIGH in T2 until the 80C86 local bus has floated. This line is held at a high impedance logic one state during “hold acknowledge” or “grant sequence”.
READY	22	I	READY: is the acknowledgment from the addressed memory or I/O device that will complete the data transfer. The RDY signal from memory or I/O is synchronized by the HS-82C85RH Clock Generator to form READY. This signal is active HIGH. The HS-80C86RH READY input is not synchronized. Correct operation is not guaranteed if the Setup and Hold Times are not met.
INTR	18	I	INTERRUPT REQUEST: is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. If so, an interrupt service routine is called via an interrupt vector lookup table located in system memory. INTR is internally synchronized and can be internally masked by software resetting the interrupt enable bit. This signal is active HIGH.
$\overline{TEST}$	23	I	TEST: input is examined by the “Wait” instruction. If the $\overline{TEST}$ input is LOW execution continues, otherwise the processor waits in an “Idle” state. This input is synchronized internally during each clock cycle on the leading edge of CLK.
NMI	17	I	NON-MASKABLE INTERRUPT: is an edge triggered input which causes a type 2 interrupt. An interrupt service routine is called via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.

Pin Description (Continued)

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
RESET	21	I	RESET: causes the processor to immediately terminate its present activity. The signal must change from LOW to HIGH and remain active HIGH for at least 4 CLK cycles. It restarts execution, as described in the Instruction Set description, when RESET returns LOW. RESET is internally synchronized.
CLK	19	I	CLOCK: provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.
VDD	40		VDD: +5V power supply pin. A 0.1µF capacitor between pins 20 and 40 is recommended for decoupling.
GND	1, 20		GND: Ground. Note: both must be connected. A 0.1µF capacitor between pins 1 and 20 is recommended for decoupling.
MN/$\overline{MX}$	33	I	MINIMUM/$\overline{MAXIMUM}$: Indicates what mode the processor is to operate in. The two modes are discussed in the following sections.
The following pin function descriptions are for the HS-80C86RH system in maximum mode (i.e., MN/$\overline{MX}$ = GND). Only the pin functions which are unique to maximum mode are described below.			
$\overline{S0}$, $\overline{S1}$, $\overline{S2}$	26-28	O	STATUS: is active during T4, T1 and T2 and is returned to the passive state (1,1,1) during T3 or during TW when READY is HIGH. This status is used by the 82C88 Bus Controller to generate all memory and I/O access control signals. Any change by $\overline{S2}$, $\overline{S1}$, or $\overline{S0}$ during T4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T3 or TW is used to indicate the end of a bus cycle. These status lines are encoded. These signals are held at a high impedance logic one state during "grant sequence". **$\overline{S2}$ $\overline{S1}$ $\overline{S0}$** 0 0 0 Interrupt Acknowledge 0 0 1 Read I/O Port 0 1 0 Write I/O Port 0 1 1 Halt 1 0 0 Code Access 1 0 1 Read Memory 1 1 0 Write Memory 1 1 1 Passive
$\overline{RQ}$/$\overline{GT}$0 $\overline{RQ}$/$\overline{GT}$1	31, 30	I/O	REQUEST/GRANT: pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bidirectional with RQ/GT0 having higher priority than RQ/GT1. RQ/GT has an internal pull-up bus hold device so it may be left unconnected. The request/grant sequence is as follows (see RQ/GT Sequence Timing.) 1. A pulse of 1 CLK wide from another local bus master indicates a local bus request ("hold") to the HS-80C86RH (pulse 1). 2. During a T4 or T1 clock cycle, a pulse 1 CLK wide from the HS-80C86RH to the requesting master (pulse 2) indicates that the HS-80C86RH has allowed the local bus to float and that it will enter the "grant sequence" state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "grant sequence". 3. A pulse 1 CLK wide from the requesting master indicates to the HS-80C86RH (pulse 3) that the "hold" request is about to end and that the HS-80C86RH can reclaim the local bus at the next CLK. The CPU then enters T4 (or T1 if no bus cycles pending). Each Master-Master exchange of the local bus is a sequence of 3 pulses. There must be one idle CLK cycle after each bus exchange. Pulses are active low. If the request is made while the CPU is performing a memory cycle, it will release the local bus during T4 of the cycle when all the following conditions are met: 1. Request occurs on or before T2. 2. Current cycle is not the low byte of a word (on an odd address). 3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence. 4. A locked instruction is not currently executing. If the local bus is idle when the request is made the two possible events will follow: 1. Local bus will be released during the next cycle. 2. A memory cycle will start within 3 CLKs. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied.

Pin Description (Continued)

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
$\overline{LOCK}$	29	O	LOCK: output indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active LOW. The $\overline{LOCK}$ signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and is held at a HIGH impedance logic one state during "grant sequence". In MAX mode, $\overline{LOCK}$ is automatically generated during T2 of the first $\overline{INTA}$ cycle and removed during T2 of the second $\overline{INTA}$ cycle.
QS1, QS0	24, 25	O	QUEUE STATUS: The queue status is valid during the CLK cycle after which the queue operation is performed. QS1 and QS2 provide status to allow external tracking of the internal HS-80C86RH instruction queue. Note that QS1, QS0 never become high impedance. **QS1 QS0** 0 0 No Operation 0 1 First Byte of Opcode from Queue 1 0 Empty the Queue 1 1 Subsequent Byte from Queue
The following pin function descriptions are for the HS-80C86RH in minimum mode (i.e. MN/$\overline{MX}$ = VDD). Only the pin functions which are unique to minimum mode are described; all other pin functions are as described below.			
M/$\overline{IO}$	28	O	STATUS LINE: logically equivalent to $\overline{S2}$ in the maximum mode. It is used to distinguish a memory access from an I/O access. M/$\overline{IO}$ becomes valid in the T4 preceding a bus cycle and remains valid until the final T4 of the cycle (M = HIGH, IO = LOW). M/$\overline{IO}$ is held to a high impedance logic zero during local bus "hold acknowledge".
$\overline{WR}$	29	O	WRITE: indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the M/$\overline{IO}$ signal. $\overline{WR}$ is active for T2, T3 and TW of any write cycle. It is active LOW, and is held to high impedance logic one during local bus "hold acknowledge".
$\overline{INTA}$	24	O	INTERRUPT ACKNOWLEDGE: is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T2, T3 and TW of each interrupt acknowledge cycle. Note that $\overline{INTA}$ is never floated.
ALE	25	O	ADDRESS LATCH ENABLE: is provided by the processor to latch the address into the 82C82 latch. It is a HIGH pulse active during clock LOW of Tl of any bus cycle. Note that ALE is never floated.
DT/$\overline{R}$	27	O	DATA TRANSMIT/RECEIVE: is needed in a minimum system that desires to use a data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically, DT/$\overline{R}$ is equivalent to $\overline{S1}$ in maximum mode, and its timing is the same as for M/$\overline{IO}$ (T = HIGH, R = LOW). DT/$\overline{R}$ is held to a high impedance logic one during local bus "hold acknowledge".
$\overline{DEN}$	26	O	DATA ENABLE: provided as an output enable fora bus transceiver in a minimum system which uses the transceiver. $\overline{DEN}$ is active LOW during each memory and I/O access and for $\overline{INTA}$ cycles. For a read or $\overline{INTA}$ cycle it is active from the middle of T2 until the middle of T4, while for a write cycle it is active from the beginning of T2 until the middle of T4. $\overline{DEN}$ is held to a high impedance logic one during local bus "hold acknowledge".
HOLD HLDA	31 30	I O	HOLD: indicates that another master is requesting a local bus "hold". To be a acknowledged, HOLD must be active HIGH. The processor receiving the "hold" will issue a "hold acknowledge" (HLDA) in the middle of a T4 or T1 clock cycle. Simultaneously with the issuance of HLDA, the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor will lower HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. HOLD is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the setup time.

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input or Output Voltage
Applied for all Grades . . . . . .VSS-0.3V to VDD+0.3V
Storage Temperature Range . . . . . -65°C to +150°C
Junction Temperature . . . . . +175°C
Lead Temperature (Soldering 10s) . . . . . +300°C
Typical Derating Factor . . . . . 12mA/MHz Increase in IDDOP
ESD Classification . . . . . Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
SBDIP Package	40.0°C/W	8.6°C/W
Ceramic Flatpack Package	72.1°C/W	9.7°C/W

Maximum Package Power Dissipation at +125°C Ambient
SBDIP Package 1.25W
Ceramic Flatpack Package 0.69W
If Device Power Exceeds Package Dissipation Capability, Provide Heat Sinking or Derate Linearly at the Following Rate
SBDIP Package . . . . . 25.0mW/°C
Ceramic Flatpack Package . . . . . 13.9mW/°C
Gate Count . . . . . 9750 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage Range (VDD) . . . . . +4.75V to +5.25V
Operating Temperature Range (T_A) . . . . . -35°C to +125°C
Input Low Voltage (VIL) . . . . . 0V to +0.8V
Input High Voltage (VIH) . . . . . 3.5V to VDD
Clock Input Low Voltage (VILC) . . . . . 0.0V to 0.8V
CLK and MN/$\overline{MX}$ Input High (VIHC) . . . . . VDD - 0.8V to VDD

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
TTL High Level Output Voltage	VOH1	VDD = 4.75V, IO = -2.5mA VIN = 0V or VDD	1, 2, 3	-35°C, +25°C, +125°C	3.0	-	V
CMOS High Level Output Voltage	VOH2	VDD = 4.75V, IO = -100µA VIN = 0V or VDD	1, 2, 3	-35°C, +25°C, +125°C	VDD - 0.4V	-	V
Low Level Output Voltage	VOL	VDD = 4.75V, IO = +2.5mA VIN = 0V or VDD	1, 2, 3	-35°C, +25°C, +125°C	-	0.4	V
Input Leakage Current	IIH or IIL	VDD = 5.25V VIN = 0V or VDD Pins: 17-19, 21-23, 33	1, 2, 3	-35°C, +25°C, +125°C	-1.0	1.0	µA
Output Leakage Current	IOZL or IOZH	VDD = 5.25V VIN = 0V or VDD Pins: 2-16, 26-29, 32, 34-39	1, 2, 3	-35°C, +25°C, +125°C	-10	10	µA
Input Current Bus Hold High	IBHH	VDD = 4.75V and 5.25V VIN = 3.0V (Note 1) Pins: 2-16, 26-32, 34-39	1, 2, 3	-35°C, +25°C, +125°C	-600	-40	µA
Input Current Bus Hold Low	IBHL	VDD = 4.75V and 5.25V VIN = 0.8V (Note 2) Pins: 2-16, 34-39	1, 2, 3	-35°C, +25°C, +125°C	40	600	µA
Standby Power Supply Current	IDDSB	VDD = 5.25V, VIN = GND or VDD, IO = 0mA (Note 3)	1, 2, 3	-35°C, +25°C, +125°C	-	500	µA
Operating Power Supply Current	IDDOP	VDD = 5.25V, VIN = GND or VDD, IO = 0mA, f = 1MHz	1, 2, 3	-35°C, +25°C, +125°C	-	12	mA/MHz
Functional Tests	FT	VDD = 4.75V and 5.25V, VIN = GND or VDD, f = 1MHz	7, 8A, 8B	-35°C, +25°C, +125°C	-	-	-
Noise Immunity Functional Tests	FN	VDD = 4.75V and 5.25V, VIN = GND or 3.5V and VDD = 4.5V, VIN = 0.8V or VDD (Note 4)	7, 8A, 8B	-35°C, +25°C, +125°C	-	-	-

NOTES:

1. IBHH should be measured after raising VIN to VDD and then lowering to 3.0V.
2. IBHL should be measured after lowering VIN to VSS and then raising to 0.8V.
3. IDDSB tested during Clock high time after halt instruction executed.
4. CLK and MN/$\overline{MX}$ Input High (VIHC) = VDD -0.8

TABLE 2A. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (MIN MODE)

ACs tested at worst case VDD, ACs guaranteed over full operating specifications.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
CLK Cycle Period	TCLCL	VDD = 4.75V VDD = 5.25V	9, 10, 11	-35°C, +25°C, +125°C	200	-	ns
CLK Low Time	TCLCH	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	118	-	ns
CLK High Time	TCHCL	VDD = 4.75V VDD = 5.25V	9, 10, 11	-35°C, +25°C, +125°C	69	-	ns
Data in Setup Time	TDVCL	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	30	-	ns
Data in Hold Time	TCLDX1	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	10	-	ns
Ready Setup Time into 80C86RH	TRYHCH	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	113	-	ns
Ready Hold Time into 80C86RH	TCHRYX	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	30	-	ns
Ready Inactive to CLK (Note 2)	TRYLCL	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	-8	-	ns
Hold Setup Time	THVCH	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	35	-	ns
INTR, NMI, Test/Setup Time	TINVCH	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	30	-	ns
MIN MODE TIMING RESPONSES (CL = 100pF)							
Address Valid Delay	TCLAV	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	10	110	ns
ALE Width	TLHLL	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	TCLCH - 20	-	ns
ALE Active Delay	TCLLH	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	-	80	ns
ALE Inactive Delay	TCHLL	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	-	85	ns
Address Hold Time to ALE Inactive	TLLAX	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	TCHCL - 10	-	ns
Control Active Delay 1	TCVCTV	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	10	110	ns
Control Active Delay 2	TCHCTV	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	10	110	ns
Control Inactive Delay	TCVCTX	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	10	110	ns
$\overline{RD}$ Active Delay	TCLRL	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	10	165	ns
$\overline{RD}$ Inactive Delay	TCLRH	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	10	150	ns
$\overline{RD}$ Inactive to Next Address Active	TRHAV	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	TCLCL - 45	-	ns
HLDA Valid Delay	TCLHAV	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	10	160	ns

TABLE 2A. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (MIN MODE) (Continued)

ACs tested at worst case VDD, ACs guaranteed over full operating specifications.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
$\overline{RD}$ Width	TRLRH	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	2TCLCL - 75	-	ns
$\overline{WR}$ Width	TWLWH	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	2TCLCL - 60	-	ns
Address Valid to ALE Low	TAVLL	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	TCLCH - 60	-	ns
Output Rise Time	TOLOH	VDD = 4.75V From 0.8V to 2.0V	9, 10, 11	-35°C, +25°C, +125°C	-	20	ns
Output Fall Time	TOHOL	VDD = 4.75V From 2.0V to 0.8V	9, 10, 11	-35°C, +25°C, +125°C	-	20	ns

NOTES:

1. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
2. Applies only to T2 State (8ns into T3).

TABLE 2B. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (MAX MODE)

ACs tested at worst case VDD, ACs guaranteed over full operating specifications.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
TIMING REQUIREMENTS							
CLK Cycle Period	TCLCL	VDD = 4.75V VDD = 5.25V	9, 10, 11	-35°C, +25°C, +125°C	200	-	ns
CLK Low Time	TCLCH	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	118	-	ns
CLK High Time	TCHCL	VDD = 4.75V VDD = 5.25V	9, 10, 11	-35°C, +25°C, +125°C	69	-	ns
Data in Setup Time	TDVCL	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	30	-	ns
Data in Hold Time	TCLDX1	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	10	-	ns
Ready Setup Time into 80C86RH	TRYHCH	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	113	-	ns
Ready Hold Time into 80C86RH	TCHRYX	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	30	-	ns
Ready Inactive to CLK (Note 2)	TRYLCL	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	-8	-	ns
INTR, NMI, Test/Setup Time	TINVCH	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	30	-	ns
$\overline{RQ}$/$\overline{GT}$ Setup Time	TGVCH	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	30	-	ns
$\overline{RQ}$ Hold Time into HS-80C86RH (Note 3)	TCHGX	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	40	TCHCL + 10	ns
MAX MODE TIMING RESPONSES (CL = 100pF)							
Ready Active to Status Passive (Notes 2 and 4)	TRYHSH	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	-	110	ns
Status Active Delay	TCHSV	VDD = 4.75V	9, 10, 11	-35°C, +25°C, +125°C	10	110	ns

TABLE 2B. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (MAX MODE) (Continued)

ACs tested at worst case VDD, ACs guaranteed over full operating specifications.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Status Inactive Delay (Note 4)	TCLSH	VDD = 4.75V	9, 10, 11	-35^{o}C, +25^{o}C, +125^{o}C	10	130	ns
Address Valid Delay	TCLAV	VDD = 4.75V	9, 10, 11	-35^{o}C, +25^{o}C, +125^{o}C	10	110	ns
$\overline{RD}$ Active Delay	TCLRL	VDD = 4.75V	9, 10, 11	-35^{o}C, +25^{o}C, +125^{o}C	10	165	ns
$\overline{RD}$ Inactive Delay	TCLRH	VDD = 4.75V	9, 10, 11	-35^{o}C, +25^{o}C, +125^{o}C	10	150	ns
$\overline{RD}$ Inactive to Next Address Active	TRHAV	VDD = 4.75V	9, 10, 11	-35^{o}C, +25^{o}C, +125^{o}C	TCLCL - 45	-	ns
$\overline{GT}$ Active Delay	TCLGL	VDD = 4.75V	9, 10, 11	-35^{o}C, +25^{o}C, +125^{o}C	0	85	ns
$\overline{GT}$ Inactive Delay	TCLGH	VDD = 4.75V	9, 10, 11	-35^{o}C, +25^{o}C, +125^{o}C	0	85	ns
$\overline{RD}$ Width	TRLRH	VDD = 4.75V	9, 10, 11	-35^{o}C, +25^{o}C, +125^{o}C	2TCLCL - 75	-	ns
Output Rise Time	TOLOH	VDD = 4.75V From 0.8V to 2.0V	9, 10, 11	-35^{o}C, +25^{o}C, +125^{o}C	-	20	ns
Output Fall Time	TOHOL	VDD = 4.75V From 2.0V to 0.8V	9, 10, 11	-35^{o}C, +25^{o}C, +125^{o}C	-	20	ns

NOTES:

1. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
2. Applies only to T2 State (8ns into T3).
3. The HS-80C86RH actively pulls the RQ/GT pin to a logic one on the following clock low time.
4. Status lines return to their inactive (logic one) state after CLK goes low and READY goes high.

TABLE 3A. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
Input Capacitance	CIN	VDD = Open, f = 1MHz (Note 1)	T_A = +25^{o}C	-	15	pF
Output Capacitance	COUT	VDD = Open, f = 1MHz (Note 1)	T_A = +25^{o}C	-	15	pF
I/O Capacitance	CI/O	VDD = Open, f = 1MHz (Note 1)	T_A = +25^{o}C	-	20	pF
TIMING REQUIREMENTS						
CLK Rise Time	TCH1CH2	VDD = 4.75V and 5.25V Min and Max Mode from 1.0V to 3.5V	-35^{o}C < T_A < +125^{o}C	-	15	ns
CLK Fall Time	TCL2CL1	VDD = 4.75V and 5.25V Min and Max Mode from 3.5V to 1.0V	-35^{o}C < T_A < +125^{o}C	-	15	ns
Input Rise Time	TILIH	VDD = 4.75V and 5.25V Min and Max Mode from 0.8V to 2.0V	-35^{o}C < T_A < +125^{o}C	-	25	ns
Input Fall Time	TIHIL	VDD = 4.75V and 5.25V Min and Max Mode from 2.0V to 0.8V	-35^{o}C < T_A < +125^{o}C	-	25	ns

TABLE 3A. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
TIMING RESPONSES						
Address Hold Time	TCLAX	VDD = 4.75V and 5.25V Min and Max Mode	$-35^oC < T_A < +125^oC$	10	-	ns
Address Float Delay (Note 2)	TCLAZ	VDD = 4.75V and 5.25V Min and Max Mode	$-35^oC < T_A < +125^oC$	TCLAX	80	ns
Data Valid Delay	TCLDV	VDD = 4.75V and 5.25V Min and Max Mode	$-35^oC < T_A < +125^oC$	10	110	ns
Data Hold Time	TCLDX2	VDD = 4.75V and 5.25V Min and Max Mode	$-35^oC < T_A < +125^oC$	10	-	ns
Data Hold Time After WR	TWHDX	VDD = 4.75V and 5.25V Min Mode	$-35^oC < T_A < +125^oC$	TCLCL - 30	-	ns
Status Float Delay (Note 2)	TCHSZ	VDD = 4.75V and 5.25V Max Mode	$-35^oC < T_A < +125^oC$	-	80	ns
Address Float to Read Active (Note 2)	TAZRL	VDD = 4.75V and 5.25V Min and Max Mode	$-35^oC < T_A < +125^oC$	0	-	ns

NOTES:

1. All measurements referenced to device ground.
2. Output drivers disabled. Bus hold circuitry still active.
3. The parameters are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

TABLE 3B. ELECTRICAL PERFORMANCE CHARACTERISTICS

Timing Signals at HS-82C85RH or 82C88 for Reference Only.

PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
RDY Setup Time into HS-82C85RH (Note 1)	TR1VCL	Min and Max Mode	$-35^oC < T_A < +125^oC$	35	-	ns
RDY Hold Time into HS-82C85RH (Note 1)	TCLR1X	Min and Max Mode	$-35^oC < T_A < +125^oC$	0	-	ns
Command Active Delay	TCLML	Max Mode Only	$-35^oC < T_A < +125^oC$	5	35	ns
Command Inactive	TCLMH	Max Mode Only	$-35^oC < T_A < +125^oC$	5	35	ns
Status Valid to ALE High	TSVLH	Max Mode Only	$-35^oC < T_A < +125^oC$	-	20	ns
Status Valid to MCE High	TSVMCH	Max Mode Only	$-35^oC < T_A < +125^oC$	-	30	ns
CLK Low to ALE Valid	TCLLH	Max Mode Only	$-35^oC < T_A < +125^oC$	-	20	ns
CLK Low to MCE High	TCLMCH	Max Mode Only	$-35^oC < T_A < +125^oC$	-	25	ns
ALE Inactive Delay	TCHLL	Max Mode Only	$-35^oC < T_A < +125^oC$	4	18	ns
MCE Inactive Delay	TCLMCL	Max Mode Only	$-35^oC < T_A < +125^oC$	-	15	ns
Control Active Delay	TCVNV	Max Mode Only	$-35^oC < T_A < +125^oC$	5	45	ns
Control Inactive Delay	TCVNX	Max Mode Only	$-35^oC < T_A < +125^oC$	10	45	ns

NOTE:

1. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.

TABLE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: See 25^oC limits in Table 1 and Table 2 for Post RAD limits (Subgroups 1, 7 and 9).

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMITS
Standby Power Supply Current	IDDSB	±100µA
Output Leakage Current	IOZL, IOZH	±2µA
Input Leakage Current	IIH, IIL	±200nA
Low Level Output Voltage	VOL	±80mV
TTL High Level Output Voltage	VOH1	±600mV
CMOS High Level Output Voltage	VOH2	±150mV

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS			
		TESTED FOR -Q	RECORDED FOR -Q	TESTED FOR -8	RECORDED FOR -8
Initial Test	100%/5004	1, 7, 9	1 (Note 2)	1, 7, 9	
Interim Test 1	100%/5004	1, 7, 9, Δ	1, Δ (Note 2)	1, 7, 9	
PDA 1	100%/5004	1, 7, Δ		1, 7	
Interim Test 2	100%/5004	1, 7, 9, Δ	1, Δ (Note 2)	N/A	
PDA 2	100%/5004	1, 7, Δ		N/A	
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11		2, 3, 8A, 8B, 10, 11	
Group A (Note 1)	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11		1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Subgroup B5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3 (Note 2)	N/A	
Subgroup B6	Sample 5005	1, 7, 9		N/A	
Group C	Sample 5005	N/A	N/A	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group D	Sample 5005	1, 7, 9		1, 7, 9	
Group E, Subgroup 2	Sample 5005	1, 7, 9		1, 7, 9	

NOTES:

1. Alternate Group A testing in accordance with MIL-STD-883 method 5005 may be exercised.
2. Table 5 parameters only.

Functional Description

Static Operation

All HS-80C86RH circuitry is of static design. Internal registers, counters and latches are static and require no refresh as with dynamic circuit design. This eliminates the minimum operating frequency restriction placed on other microprocessors. The CMOS HS-80C86RH can operate from DC to 5MHz. The processor clock may be stopped in either state (HIGH/LOW) and held there indefinitely. This type of operation is especially useful for system debug or power critical applications.

The HS-80C86RH can be single stepped using only the CPU clock. This state can be maintained as long as is necessary. Single step clock operation allows simple interface circuitry to provide critical information for bringing up your system.

Static design also allows very low frequency operation (down to DC). In a power critical situation, this can provide extremely low power operation since HS-80C86RH power dissipation is directly related to operating frequency. As the system frequency is reduced, so is the operating power until, ultimately, at a DC input frequency, the HS-80C86RH power requirement is the standby current, (500µA maximum).

Internal Architecture

The internal functions of the HS-80C86RH processor are partitioned logically into two processing units. The first is the Bus Interface Unit (BIU) and the second is the Execution Unit (EU) as shown in the CPU functional diagram.

These units can interact directly but for the most part perform as separate asynchronous operational processors. The bus interface unit provides the functions related to instruction fetching and queuing, operand fetch and store, and address relocation. This unit also provides the basic bus control. The overlap of instruction pre-fetching provided by this unit serves to increase processor performance through improved bus bandwidth utilization. Up to 6 bytes of the instruction stream can be queued while waiting for decoding and execution.

The instruction stream queuing mechanism allows the BIU to keep the memory utilized very efficiently. Whenever there is space for at least 2 bytes in the queue, the BIU will attempt a word fetch memory cycle. This greatly reduces “dead-time” on the memory bus. The queue acts as a First-In-First-Out (FIFO) buffer, from which the EU extracts instruction bytes as required. If the queue is empty (following a branch instruction, for example), the first byte into the queue immediately becomes available to the EU.

The execution unit receives pre-fetched instructions from the BIU queue and provides un-relocated operand addresses to the BIU. Memory operands are passed through the BIU for processing by the EU, which passes results to the BIU for storage.

Memory Organization

The processor provides a 20-bit address to memory, which locates the byte being referenced. The memory is organized as a linear array of up to 1 million bytes, addressed as 00000(H) to FFFFF(H). The memory is logically divided into code, data, extra and stack segments of up to 64K bytes each, with each segment falling on 16 byte boundaries. (See Figure 1).

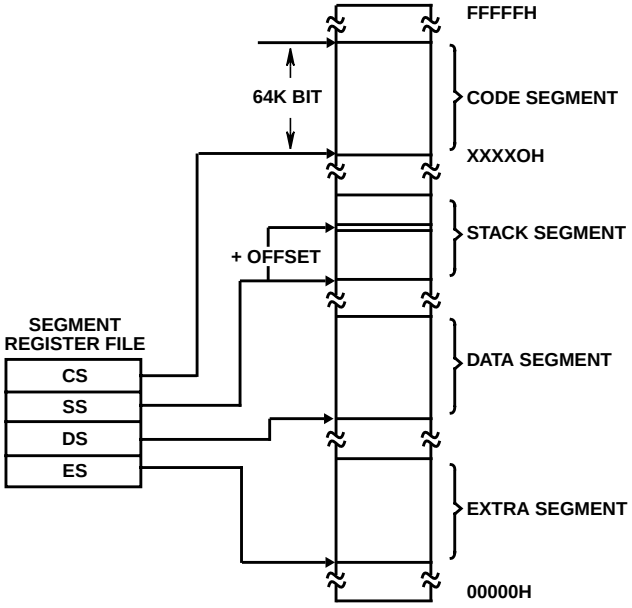


FIGURE 1. HS-80C86RH MEMORY ORGANIZATION

TABLE 7.

TYPE OF MEMORY REFERENCE	DEFAULT SEGMENT BASE	ALTERNATE SEGMENT BASE	OFFSET
Instruction Fetch	CS	None	IP
Stack Operation	SS	None	SP
Variable (Except Following)	DS	CS, ES, SS	Effective Address
String Source	DS	CS, ES, SS	SI
String Destination	ES	None	DI
BP Used as Base Register	SS	CS, DS, ES	Effective Address

All memory references are made relative to base addresses contained in high speed segment registers. The segment types were chosen based on the addressing needs of programs. The segment register to be selected is automatically chosen according to the specific rules of Table 7. All information in one segment type share the same logical attributes (e.g. code or data). By structuring memory into relocatable areas of similar characteristics and by automatically selecting segment registers, programs are shorter, faster and more structured. (See Table 7).

Word (16-bit) operands can be located on even or odd address boundaries and are thus not constrained to even boundaries as is the case in many 16-bit computers. For address and data operands, the least significant byte of the word is stored in the lower valued address location and the most significant byte in the next higher address location. The BIU automatically performs the proper number of memory accesses, one if the word operand is on an even byte boundary and two if it is on an odd byte boundary. Except for the performance penalty, this double access is transparent to the software. The performance penalty does not occur for instruction fetches; only word operands.

Physically, the memory is organized as a high bank (D15-D6) and a low bank (D7-D0) of 512K bytes addressed in parallel by the processor’s address lines.

Byte data with even addresses is transferred on the D7-D0 bus lines while odd addressed byte data (A0 HIGH) is transferred on the D15-D6 bus lines. The processor provides two enable signals, $\overline{BHE}$ and A0, to selectively allow reading from or writing into either an odd byte location, even byte location, or both. The instruction stream is fetched from memory as words and is addressed internally by the processor at the byte level as necessary.

In referencing word data, the BIU requires one or two memory cycles depending on whether the starting byte of the word is on an even or odd address, respectively. Consequently, in referencing word operands performance can be optimized by locating data on even address boundaries. This is an especially useful technique for using the stack, since odd address references to the stack may adversely affect the context switching time for interrupt processing or task multiplexing.

Certain locations in memory are reserved for specific CPU operations (See Figure 2). Locations from address FFFF0H through FFFFFH are reserved for operations including a jump to the initial program loading routine. Following RESET, the CPU will always begin execution at location FFFF0H where the jump must be located. Locations 00000H through 003FFH are reserved for interrupt operations. Each of the 256 possible interrupt service routines is accessed through its own pair of 16-bit pointers - segment address pointer and offset address pointer. The first pointer, used as the offset address, is loaded into the 1P and the second pointer, which designates the base address is loaded into the CS. At this point program control is transferred to the interrupt routine. The pointer elements are assumed to have been stored at the respective places in reserved memory prior to occurrence of interrupts.

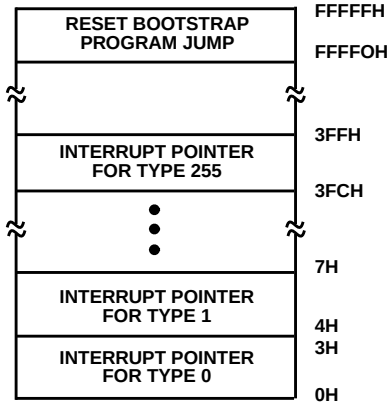


FIGURE 2. RESERVED MEMORY LOCATIONS

Minimum and Maximum Operation Modes

The requirements for supporting minimum and maximum HS-80C86RH systems are sufficiently different that they cannot be met efficiently using 40 uniquely defined pins. Consequently, the HS-80C86RH is equipped with a strap pin (MN/$\overline{MX}$) which defines the system configuration. The definition of a certain subset of the pins changes, dependent on the condition of the strap pin. When the MN/$\overline{MX}$ pin is strapped to GND, the HS-80C86RH defines pins 24 through 31 and 34 in maximum mode. When the MN/$\overline{MX}$ pin is strapped to VDD, the HS-80C86RH generates bus control signals itself on pins 24 through 31 and 34.

Bus Operation

The HS-80C86RH has a combined address and data bus commonly referred to as a time multiplexed bus. This technique provides the most efficient use of pins on the processor while permitting the use of a standard 40-lead package. This “local bus” can be buffered directly and used throughout the system with address latching provided on memory and I/O modules. In addition, the bus can also be demultiplexed at the processor with a single set of 82C82 latches if a standard non-multiplexed bus is desired for the system.

Each processor bus cycle consists of at least four CLK cycles. These are referred to as T1, T2, T3 and T4 (see Figure 3). The address is emitted from the processor during T1 and data transfer occurs on the bus during T3 and T4. T2 is used primarily for changing the direction of the bus during read operations. In the event that a “NOT READY” indication is given by the addressed device, “Wait” states (TW) are inserted between T3 and T4. Each inserted wait state is the same duration as a CLK cycle. Idle periods occur between HS-80C86RH driven bus cycles whenever the processor performs internal processing.

During T1 of any bus cycle, the ALE (Address Latch Enable) signal is emitted (by either the processor or the 82C88 bus controller, depending on the MN/$\overline{MX}$ strap). At the trailing edge of this pulse, a valid address and certain status information for the cycle may be latched.

Status bits $\overline{S0}$, $\overline{S1}$ and $\overline{S2}$ are used by the bus controller, in maximum mode, to identify the type of bus transaction according to Table 8.

TABLE 8.

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	CHARACTERISTICS
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O Port
0	1	0	Write I/O Port
0	1	1	Halt
1	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

Status bits S3 through S7 are time multiplexed with high order address bits and the $\overline{BHE}$ signal, and are therefore valid during T2 through T4. S3 and S4 indicate which segment register (see Instruction Set Description) was used for this bus cycle in forming the address, according to Table 9.

TABLE 9.

S4	S3	CHARACTERISTICS
0 (Low)	0	Alternate Data (extra segment)
0	1	Stack
1 (High)	0	Code or None
1	1	Data

S5 is a reflection of the PSW interrupt enable bit. S6 is always zero and S7 is a spare status bit.

I/O Addressing

In the HS-80C86RH, I/O operations can address up to a maximum of 64K I/O byte registers or 32K I/O word registers. The I/O address appears in the same format as the memory address on bus lines A15-A0. The address lines A19-A16 are zero in I/O operations. The variable I/O instructions which use register DX as a pointer have full address capability while the direct I/O instructions directly address one or two of the 256 I/O byte locations in page 0 of the I/O address space.

I/O ports are addressed in the same manner as memory locations. Even addressed bytes are transferred on the D7-D0 bus lines and odd addressed bytes on D15-D8. Care must be taken to ensure that each register within an 8-bit peripheral located on the lower portion of the bus be addressed as even.

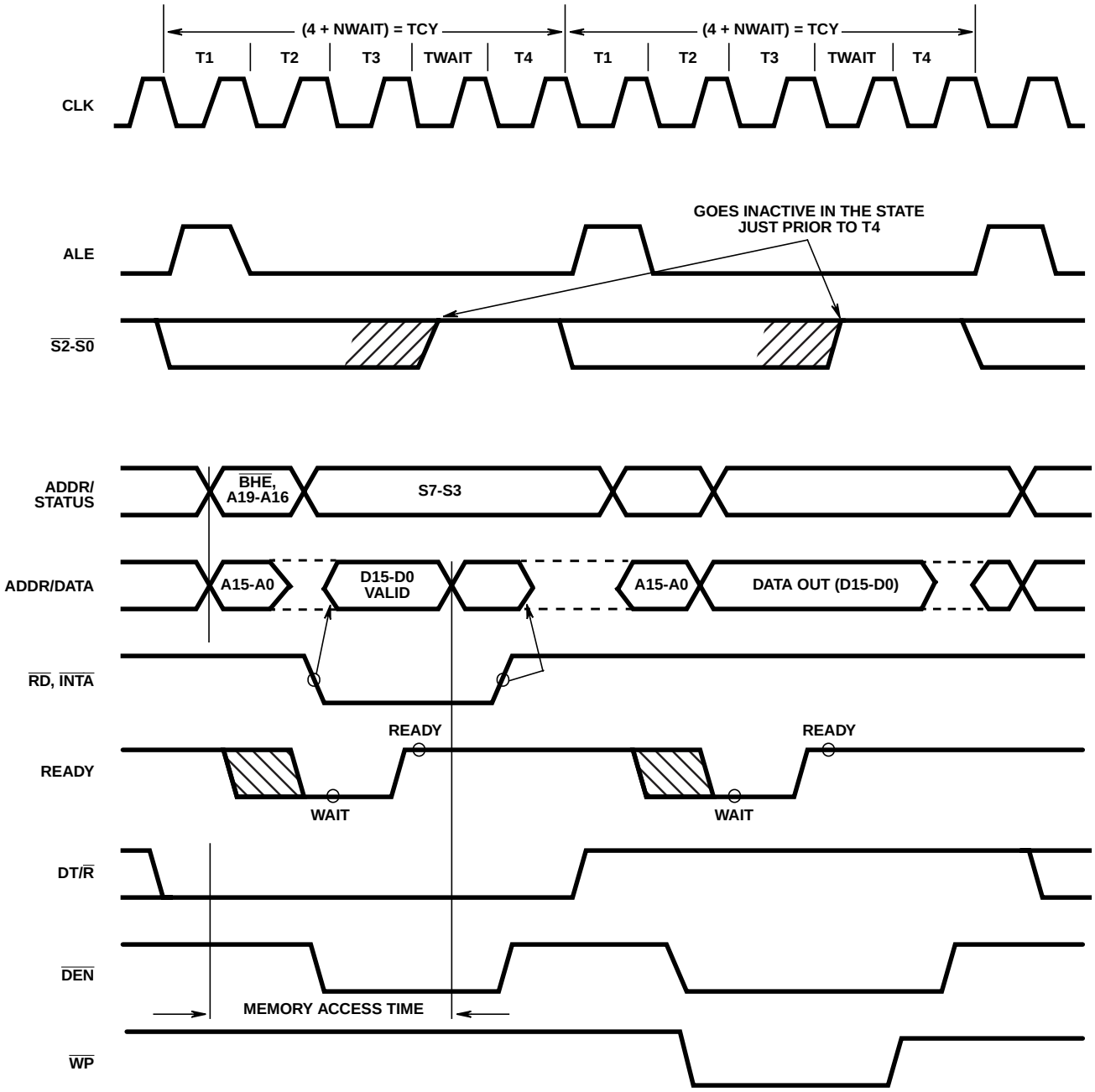


FIGURE 3. BASIC SYSTEM TIMING

External Interface

Processor RESET and Initialization

Processor initialization or start up is accomplished with activation (HIGH) of the RESET pin. The HS-80C86RH RESET is required to be HIGH for greater than 4 CLK cycles. The HS-80C86RH will terminate operations on the high-going edge of RESET and will remain dormant as long as RESET is HIGH. The low-going transition of RESET triggers an internal reset sequence for approximately 7 CLK cycles. After this interval, the HS-80C86RH operates normally beginning with the instruction in absolute location FFFFOH. (See Figure 2). The RESET input is internally synchronized to the processor clock. At initialization, the HIGH-to-LOW transition of RESET must occur no sooner than 50µs (or 4 CLK cycles, whichever is greater) after power-up, to allow complete initialization of the HS-80C86RH.

NMI will not be recognized prior to the second clock cycle following the end of RESET. If NMI is asserted sooner than 9 CLK cycles after the end of RESET, the processor may execute one instruction before responding to the interrupt.

Bus Hold Circuitry

To avoid high current conditions caused by floating inputs to CMOS devices and to eliminate need for pull- up/down resistors, “bus-hold” circuitry has been used on the HS-80C86RH pins 2-16, 26-32 and 34-39. (See Figure 4A and 4B). These circuits will maintain the last valid logic state if no driving source is present (i.e. an unconnected pin or a driving source which goes to a high impedance state). To overdrive the “bus hold” circuits, an external driver must be capable of supplying approximately 400µA minimum sink or source current at valid input voltage levels. Since this “bus hold” circuitry is active and not a “resistive” type element, the associated power supply current is negligible and power dissipation is significantly reduced when compared to the use of passive pull-up resistors.

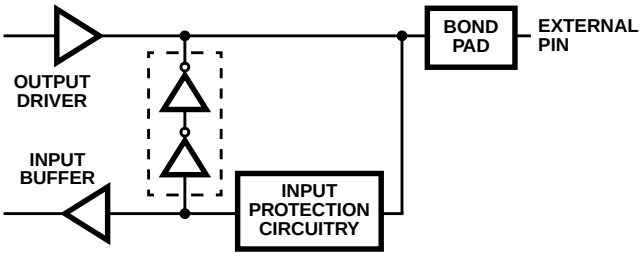


FIGURE 4A. BUS HOLD CIRCUITRY PIN 2-16, 34-39

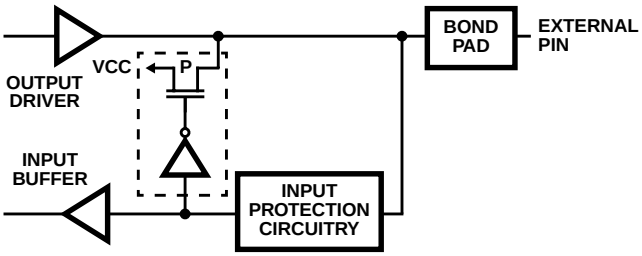


FIGURE 4B. BUS HOLD CIRCUITRY PIN 26-32

Interrupt Operations

Interrupt operations fall into two classes: software or hardware initiated. The software initiated interrupts and software aspects of hardware interrupts are specified in the Instruction Set Description. Hardware interrupts can be classified as non-maskable or maskable.

Interrupts result in a transfer of control to a new program location. A 256-element table containing address pointers to the interrupt service routine locations resides in absolute locations 0 through 3FFH, which are reserved for this purpose. Each element in the table is 4 bytes in size and corresponds to an interrupt “type”. An interrupting device supplies an 8-bit type number during the interrupt acknowledge sequence, which is used to “vector” through the appropriate element to the interrupt service routine location. All flags and both the Code Segment and Instruction Pointer register are saved as part of the $\overline{\text{INTA}}$ sequence. These are restored upon execution of an Interrupt Return (IRET) instruction.

Non-Maskable Interrupt (NMI)

The processor provides a single non-maskable interrupt pin (NMI) which has higher priority than the maskable interrupt request pin (INTR). A typical use would be to activate a power failure routine. The NMI is edge-triggered on a LOW-to-HIGH transition. The activation of this pin causes a type 2 interrupt.

NMI is required to have a duration in the HIGH state of greater than 2 CLK cycles, but is not required to be synchronized to the clock. Any positive transition of NMI is latched on-chip and will be serviced at the end of the current instruction or between whole moves of a block-type instruction. Worst case response to NMI would be for multiply, divide, and variable shift instructions. There is no specification on the occurrence of the low-going edge; it may occur before, during or after the servicing of NMI. Another positive edge triggers another response if it occurs after the start of the NMI procedure. The signal must be free of logical spikes in general and be free of bounces on the low-going edge to avoid triggering extraneous responses.

Maskable Interrupt (INTR)

The HS-80C86RH provides a single interrupt request input (INTR) which can be masked internally by software with the resetting of the interrupt enable flag (IF) status bit. The interrupt request signal is level triggered. It is internally synchronized during each clock cycle on the high-going edge of CLK. To be responded to, INTR must be present (HIGH) during the clock period preceding the end of the current instruction or the end of a whole move for a block- type instruction. INTR may be removed anytime after the falling edge of the first $\overline{\text{INTA}}$ signal. During the interrupt response sequence further interrupts are disabled. The enable bit is reset as part of the response to any interrupt (INTR, NMI, software interrupt or single-step), although the FLAGS register which is automatically pushed onto the stack reflects the state of the processor prior to the interrupt. Until the old FLAGS register is restored the enable bit will be zero unless specifically set by an instruction.

During the response sequence (Figure 5) the processor executes two successive (back-to-back) interrupt acknowledge cycles. The HS-80C86RH emits the $\overline{LOCK}$ signal (Max mode only) from T2 of the first bus cycle until T2 of the second. A local bus "hold" request will not be honored until the end of the second bus cycle. In the second bus cycle, a byte is supplied to the HS-80C86RH by the HS-82C89ARH Interrupt Controller, which identifies the source (type) of the interrupt. This byte is multiplied by four and used as a pointer into the interrupt vector lookup table. An INTR signal left HIGH will be continually responded to within the limitations of the enable bit and sample period. The INTERRUPT RETURN instruction includes a FLAGS pop which returns the status of the original interrupt enable bit when it restores the FLAGS.

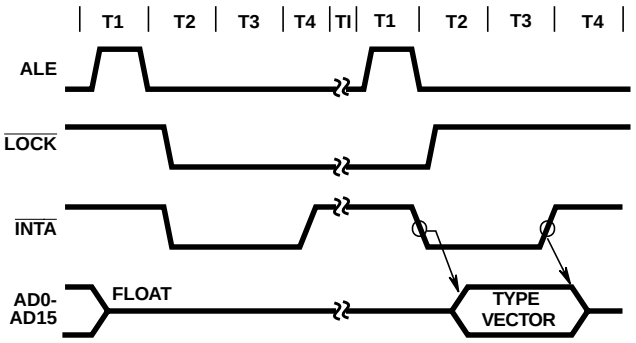


FIGURE 5. INTERRUPT ACKNOWLEDGE SEQUENCE

Halt

When a software "HALT" instruction is executed the pro- cessor indicates that it is entering the "HALT" state in one of two ways depending upon which mode is strapped. In minimum mode, the processor issues one ALE with no qualifying bus control signals. In maximum mode the processor issues appropriate HALT status on $\overline{S2}$, $\overline{S1}$, $\overline{S0}$ and the 82C88 bus controller issues one ALE. The HS-80C86RH will not leave the "HALT" state when a local bus "hold" is entered while in "HALT". In this case, the processor reissues the HALT indicator at the end of the local bus hold. An NMI or interrupt request (when interrupts enabled) or RESET will force the HS-80C86RH out of the "HALT" state.

Read/Modify/Write (Semaphore)

Operations Via $\overline{Lock}$

The $\overline{LOCK}$ status information is provided by the processor when consecutive bus cycles are required during the execution of an instruction. This gives the processor the capability of performing read/modify/write operations on memory (via the Exchange Register With Memory instruction, for example) without another system bus master receiving intervening memory cycles. This is useful in multiprocessor system configurations to accomplish "test and set lock" operations. The $\overline{LOCK}$ signal is activated (forced LOW) in the clock cycle following decoding of the software "LOCK" prefix instruction. It is deactivated at the end of the last bus cycle of the instruction following the "LOCK" prefix instruction. While $\overline{LOCK}$ is active a request on a $\overline{RQ}/\overline{GT}$ pin will be recorded and then honored at the end of the $\overline{LOCK}$.

External Synchronization Via TEST

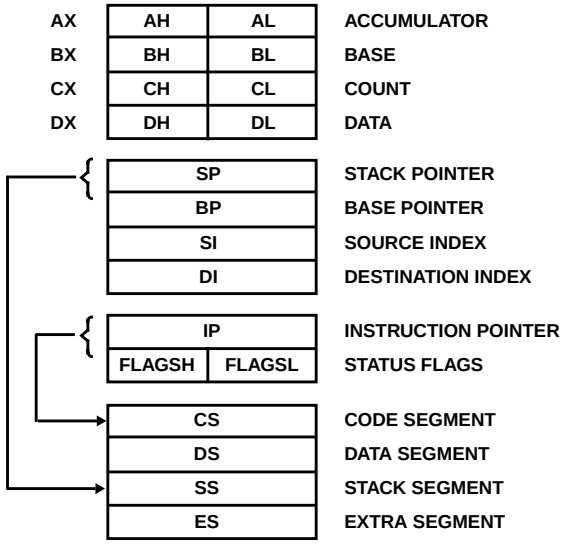
As an alternative to interrupts, the HS-80C86RH provides a single software-testable input pin ($\overline{TEST}$). This input is utilized by executing a WAIT instruction. The single WAIT instruction is repeatedly executed until the $\overline{TEST}$ input goes active (LOW). The execution of WAIT does not consume bus cycles once the queue is full.

If a local bus request occurs during WAIT execution, the HS-80C86RH three-states all output drivers while inputs and I/O pins are held at valid logic levels by internal bus-hold circuits. If interrupts are enabled, the HS-80C86RH will recognize interrupts and process them when it regains control of the bus. The WAIT instruction is then refetched, and reexecuted.

Basic System Timing

Typical system configurations for the processor operating in minimum mode and in maximum mode are shown in Figures 6A and 6B, respectively. In minimum mode, the MN/$\overline{MX}$ pin is strapped to VDD and the processor emits bus control signals (e.g. $\overline{RD}$, $\overline{WR}$, etc.) directly. In maximum mode, the MN/$\overline{MX}$ pin is strapped to GND and the processor emits coded status information which the 82C88 bus controller used to generate MULTIBUS™ compatible bus control signals. Figure 3 shows the signal timing relationships.

TABLE 10. HS-80C86RH REGISTER MODEL



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System Timing - Minimum System

The read cycle begins in T1 with the assertion of the Address Latch Enable (ALE) signal. The trailing (low-going) edge of this signal is used to latch the address information, which is valid on the address/data bus (AD0-AD15) at this time, into the 82C82 latches. The $\overline{BHE}$ and A0 signals address the low, high or both bytes. From T1 to T4 the M/$\overline{IO}$ signal indicates a memory or I/O operation. At T2, the address is removed from the address/data bus and the bus is held at the last valid logic state by internal bus hold devices. The read control signal is also asserted at T2. The read ($\overline{RD}$) signal causes the addressed device to enable its data bus drivers to the local bus. Some time later, valid data

will be available on the bus and the addressed device will drive the READY line HIGH. When the processor returns the read signal to a HIGH level, the addressed device will three-state its bus drivers. If a transceiver is required to buffer the HS-80C86RH local bus, signals DT/R and DEN are provided by the HS-80C86RH.

A write cycle also begins with the assertion of ALE and the emission of the address. The M/$\overline{IO}$ signal is again asserted to indicate a memory or I/O write operation. In T2, immediately following the address emission, the processor emits the data to be written into the addressed location. This data remains valid until at least the middle of T4. During T2, T3 and TW, the processor asserts the write control signal. The write ($\overline{WR}$) signal becomes active at the beginning of T2 as opposed to the read which is delayed somewhat into T2 to provide time for output drivers to become inactive.

The BHE and A0 signals are used to select the proper byte(s) of the memory/IO word to be read or written according to Table 11.

TABLE 11.

BHE	A0	CHARACTERISTICS
0	0	Whole word
0	1	Upper byte from/to odd address
1	0	Lower byte from/to even address
1	1	None

I/O ports are addressed in the same manner as memory location. Even addressed bytes are transferred on the D7-D0 bus lines and odd address bytes on D15-D6.

The basic difference between the interrupt acknowledge cycle and a read cycle is that the interrupt acknowledge signal ($\overline{INTA}$) is asserted in place of the read ($\overline{RD}$) signal and the address bus is held at the last valid logic state by internal bus hold devices. (See Figure 4). In the second of two successive $\overline{INTA}$ cycles a byte of information is read from the data bus (D7-D0) as supplied by the interrupt system logic (i.e. HS-82CS9ARH Priority Interrupt Controller). This byte identifies the source (type) of the interrupt. It is multiplied by four and used as a pointer into an interrupt vector Iookup table, as described earlier.

Bus Timing - Medium and Large Size Systems

For medium complexity systems the MN/$\overline{MX}$ pin is connected to GND and the 82C88 Bus Controller is added to the system as well as three 82C82 latches for latching the system address, and a transceiver to allow for bus loading greater than the HS-80C86RH is capable of handling. Bus control signals are generated by the 82C88 instead of the processor in this configuration, although their timing remains relatively the same. The HS-80C86RH status outputs ($\overline{S2}$, $\overline{S1}$, and $\overline{S0}$) provide type-of-cycle information and become 82C88 inputs. This bus cycle information specifies read (code, data or I/O), write (data or I/O), interrupt acknowledge, or software halt. The 82C88 issues control signals specifying memory read or write, I/O read or write, or interrupt acknowledge. The 82C88 provides two types of write strobes, normal and advanced, to be applied as required. The normal write strobes have data valid at the leading edge of write. The advanced write strobes have the same timing as read strobes, and hence, data is not valid at the leading edge of write. The transceiver receives the usual T and 0E inputs from the 82C88 DT/$\overline{R}$ and DEN signals.

For large multiple processor systems, the 82C89 bus arbiter must be added to the system to provide system bus management. In this case, the pointer into the interrupt vector table, which is passed during the second $\overline{INTA}$ cycle, can be derived from an HS-82C59ARH located on either the local bus or the system bus. The processor's $\overline{INTA}$ output should drive the SYSB/$\overline{RESB}$ input of the 82C89 to the proper state when reading the interrupt vector number from the HS-82C59ARH during the interrupt acknowledge sequence and software “poll”.

A Note on Radiation Hardened Product Availability

There are no immediate plans to develop the 82C88 Bus Controller or the 82C89 Arbiter as radiation hardened integrated circuits.

A Note on SEU Capability of the HS-80C86RH

Previous heavy ion testing of the HS-80C86RH has indicated that the SEU threshold of this part is about 6 MEV/mg/cm^2. Based upon these results and other analysis, a deep space galactic cosmic-ray environment will result in an SEU rate of about 0.08 upsets/day.

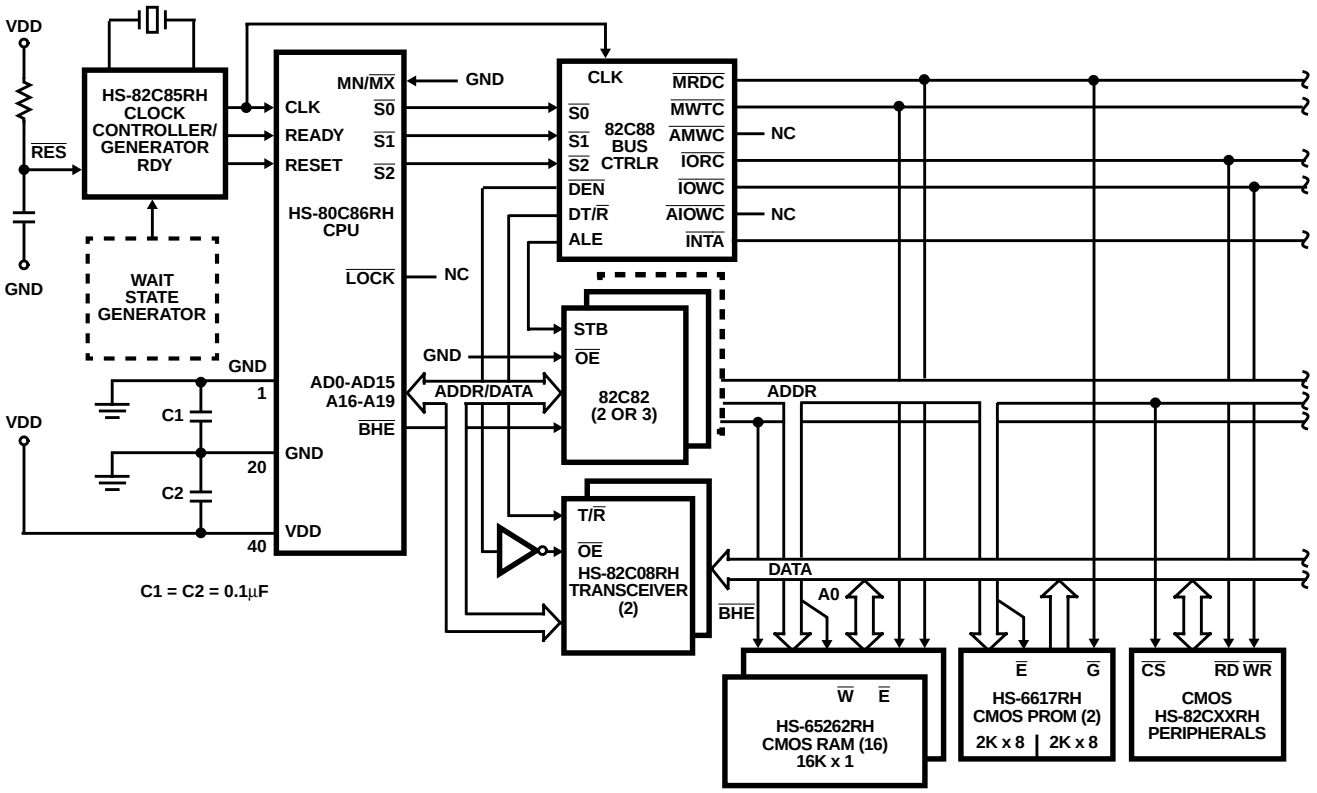


FIGURE 6A. MAXIMUM MODE HS-80C86RH TYPICAL CONFIGURATION

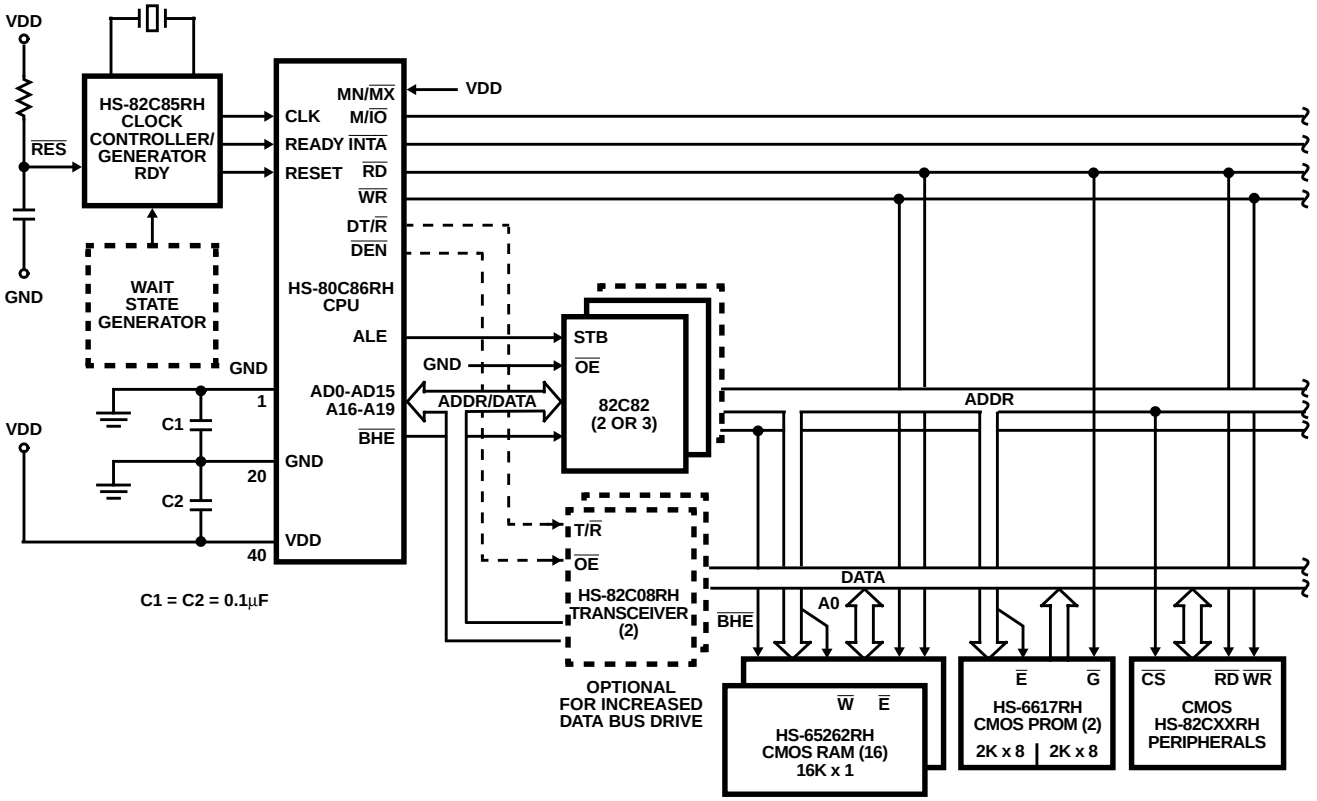


FIGURE 6B. MINIMUM MODE HS-80C86RH TYPICAL CONFIGURATION

Waveforms

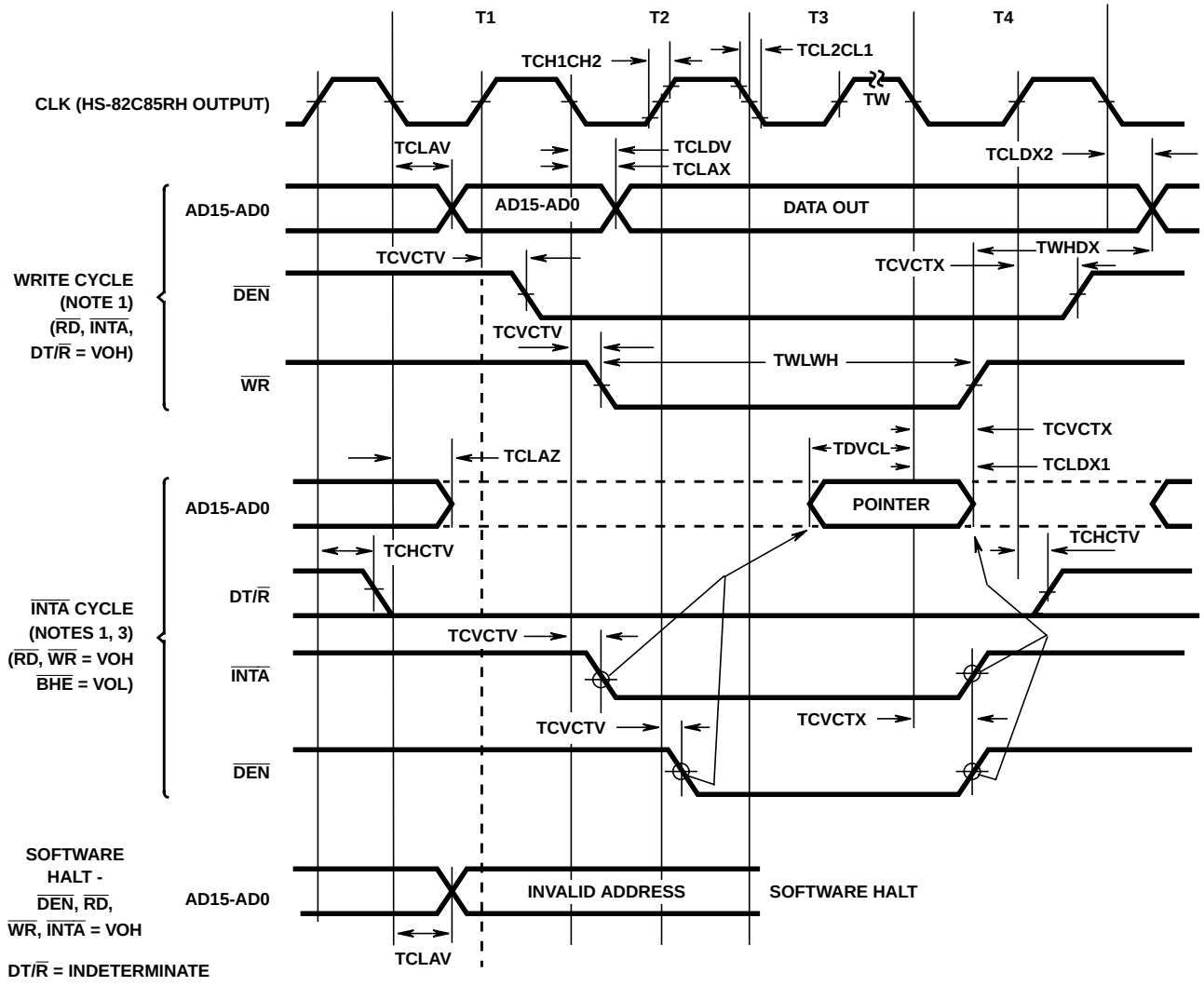


FIGURE 7. BUS TIMING - MINIMUM MODE SYSTEM

NOTES:

1. All signals switch between VOH and VOL unless otherwise specified.
2. RDY is sampled near the end of T2, T3, TW to determine if TW machines states are to be inserted.
3. Two $\overline{\text{INTA}}$ cycles run back-to-back. The HS-80C86RH local ADDR/DATA bus is inactive during both $\overline{\text{INTA}}$ cycles. Control signals are shown for the second $\overline{\text{INTA}}$ cycle.
4. Signals at HS-82C85RH are shown for reference only.
5. All timing measurements are made at 1.5V unless otherwise noted.

Waveforms (Continued)

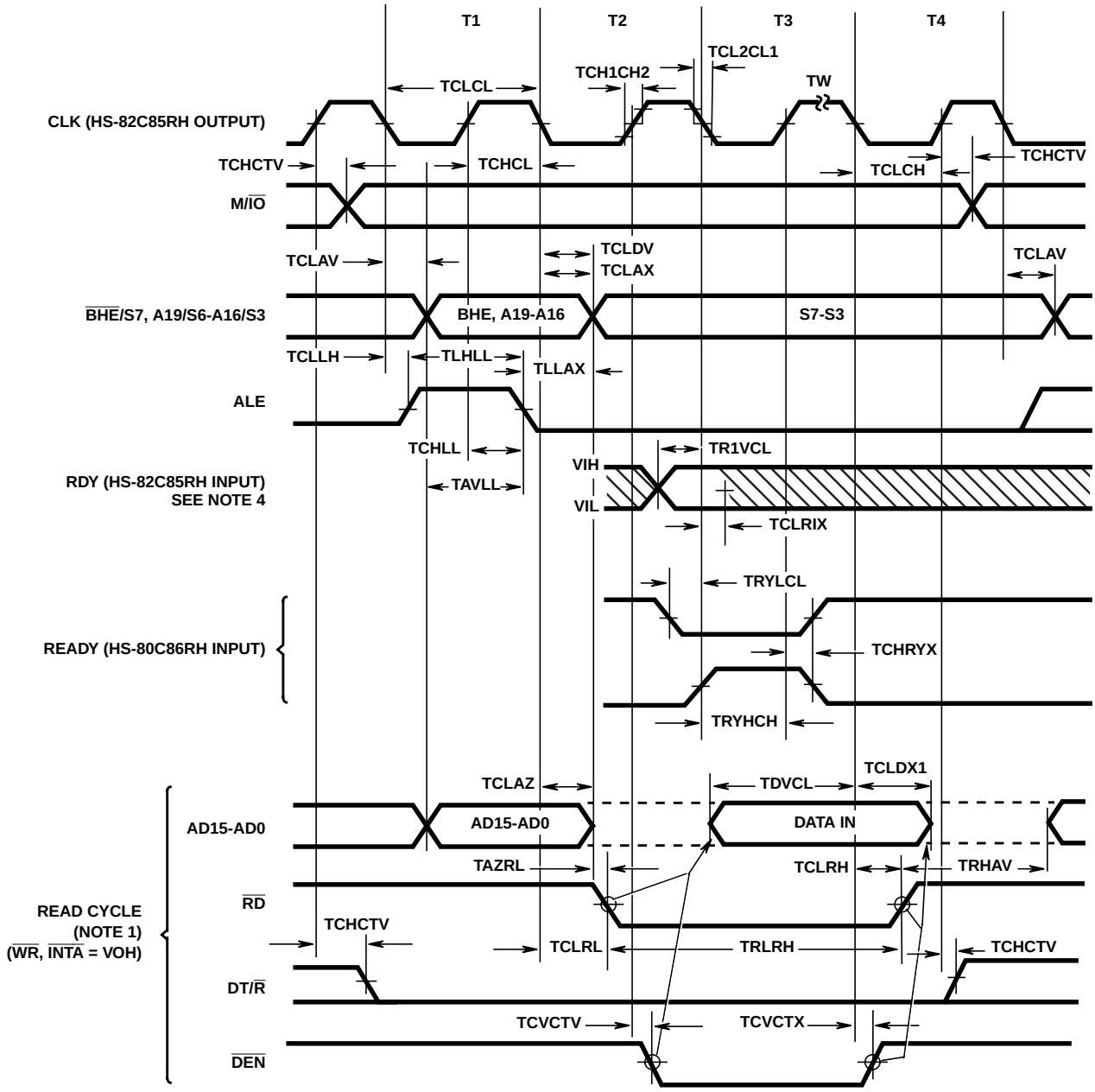


FIGURE 8. BUS TIMING - MINIMUM MODE SYSTEM

NOTES:

1. All signals switch between VOH and VOL unless otherwise specified.
2. RDY is sampled near the end of T2, T3, TW to determine if TW machines states are to be inserted.
3. Two $\overline{\text{INTA}}$ cycles run back-to-back. The HS-80C86RH local ADDR/DATA bus is inactive during both $\overline{\text{INTA}}$ cycles. Control signals are shown for the second $\overline{\text{INTA}}$ cycle.
4. Signals at HS-82C85RH are shown for reference only.
5. All timing measurements are made at 1.5V unless otherwise noted.

Waveforms (Continued)

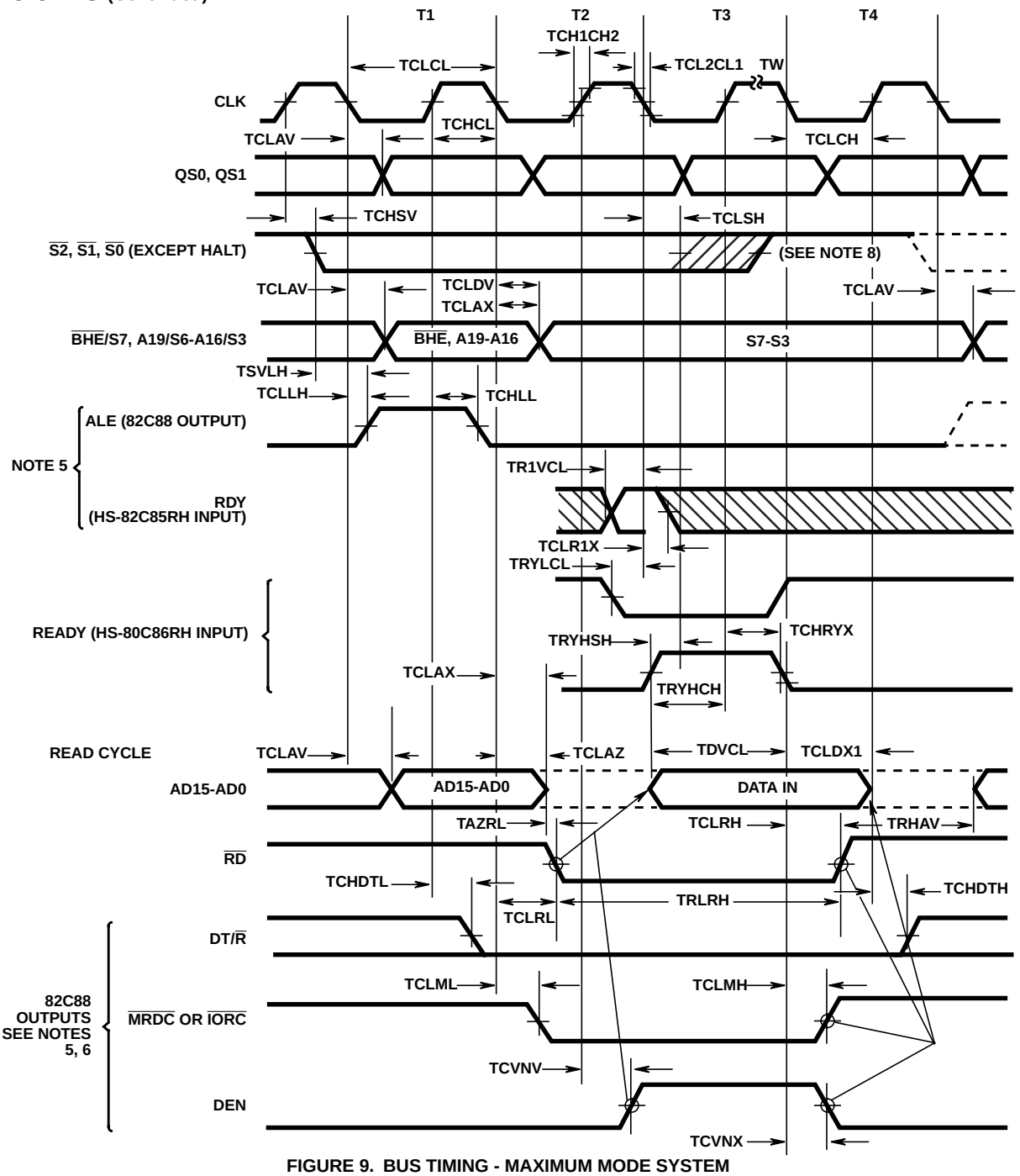


FIGURE 9. BUS TIMING - MAXIMUM MODE SYSTEM

NOTES:

1. All signals switch between VOH and VOL unless otherwise specified.
2. RDY is sampled near the end of T2, T3, TW to determine if TW machines states are to be inserted.
3. Cascade address is valid between first and second $\overline{\text{INTA}}$ cycle.
4. Two $\overline{\text{INTA}}$ cycles run back-to-back. The HS-80C86RH local ADDR/DATA bus is inactive during both $\overline{\text{INTA}}$ cycles. Control for pointer address is shown for the second $\overline{\text{INTA}}$ cycle.
5. Signals at HS-82C85RH or 82C88 are shown for reference only.
6. The issuance of the 82C88 command and control signals ($\overline{\text{MRDC}}$, $\overline{\text{MWTC}}$, $\overline{\text{AMWC}}$, $\overline{\text{IORC}}$, $\overline{\text{IOWC}}$, $\overline{\text{AIOWC}}$, $\overline{\text{INTA}}$ and DEN) lags the active high 82C88 CEN.
7. All timing measurements are made at 1.5V unless otherwise noted.
8. Status inactive in state just prior to T4.

Waveforms (Continued)

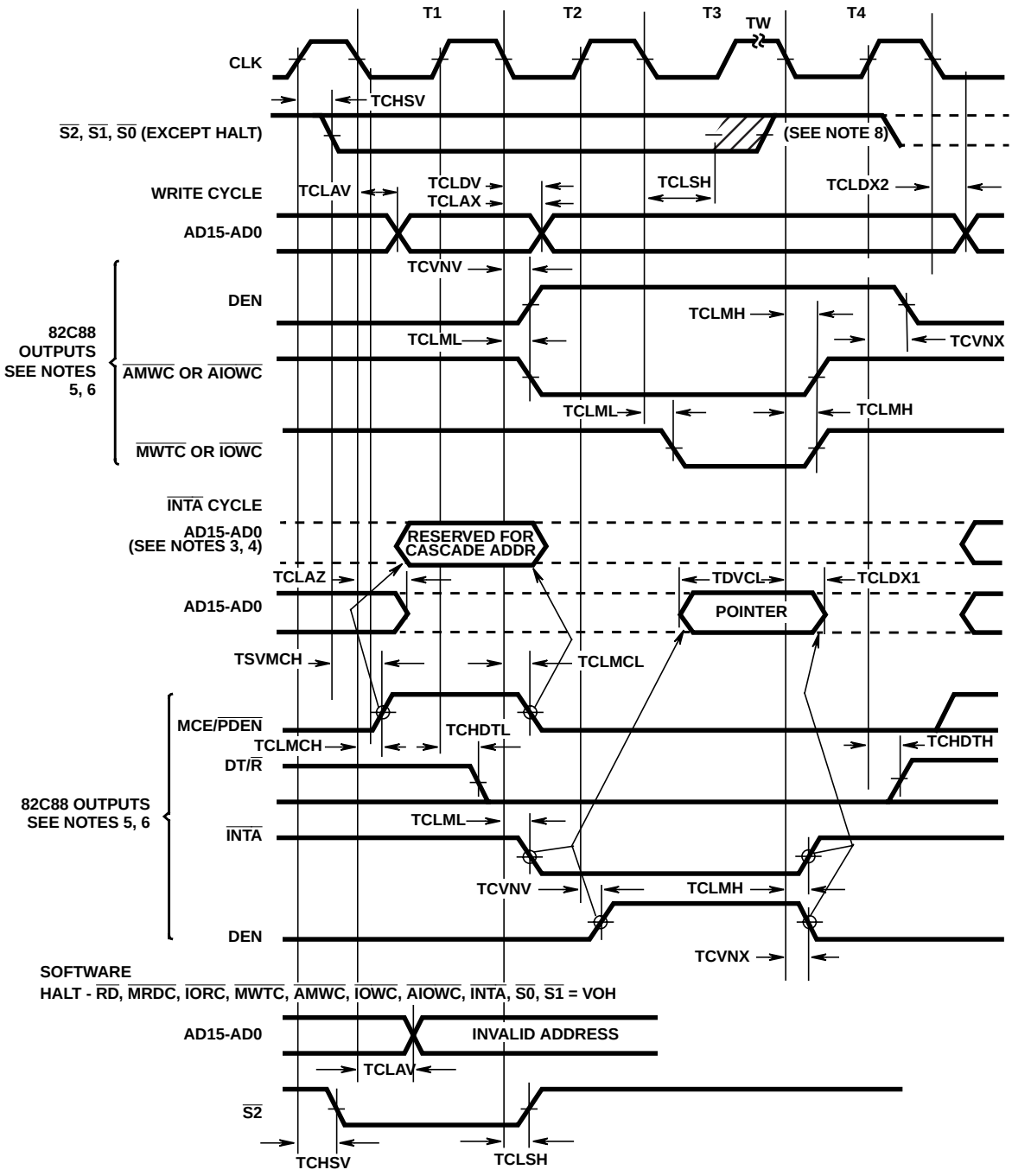
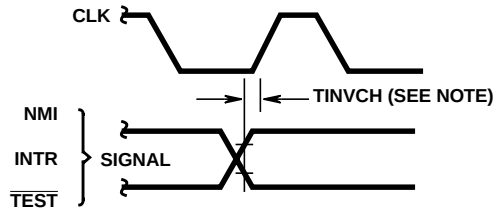


FIGURE 10. BUS TIMING - MAXIMUM MODE SYSTEM (USING 82C88)

NOTES:

1. All signals switch between VOH and VOL unless otherwise specified.
2. RDY is sampled near the end of T2, T3, TW to determine if TW machines states are to be inserted.
3. Cascade address is valid between first and second $\overline{\text{INTA}}$ cycle.
4. Two $\overline{\text{INTA}}$ cycles run back-to-back. The HS-80C86RH local ADDR/DATA bus is inactive during both $\overline{\text{INTA}}$ cycles. Control for pointer address is shown for the second $\overline{\text{INTA}}$ cycle.
5. Signals at HS-82C85RH or 82C88 are shown for reference only.
6. The issuance of the 82C88 command and control signals ($\overline{\text{MRDC}}$, $\overline{\text{MWTC}}$, $\overline{\text{AMWC}}$, $\overline{\text{IORC}}$, $\overline{\text{IOWC}}$, $\overline{\text{AIOWC}}$, $\overline{\text{INTA}}$ and DEN) lags the active high 82C88 CEN.
7. All timing measurements are made at 1.5V unless otherwise noted.
8. Status inactive in state just prior to T4.

Waveforms (Continued)



NOTE: Setup Requirements for asynchronous signals only to guarantee recognition at next CLK.

FIGURE 11. ASYNCHRONOUS SIGNAL RECOGNITION

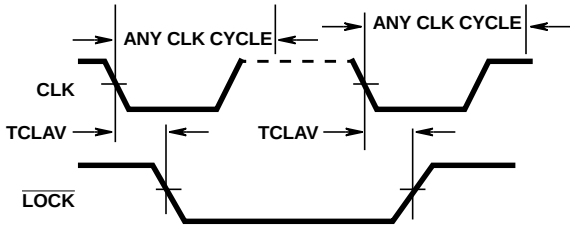


FIGURE 12. BUS LOCK SIGNAL TIMING (MAXIMUM MODE ONLY)

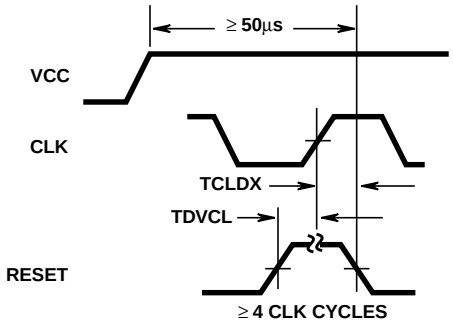
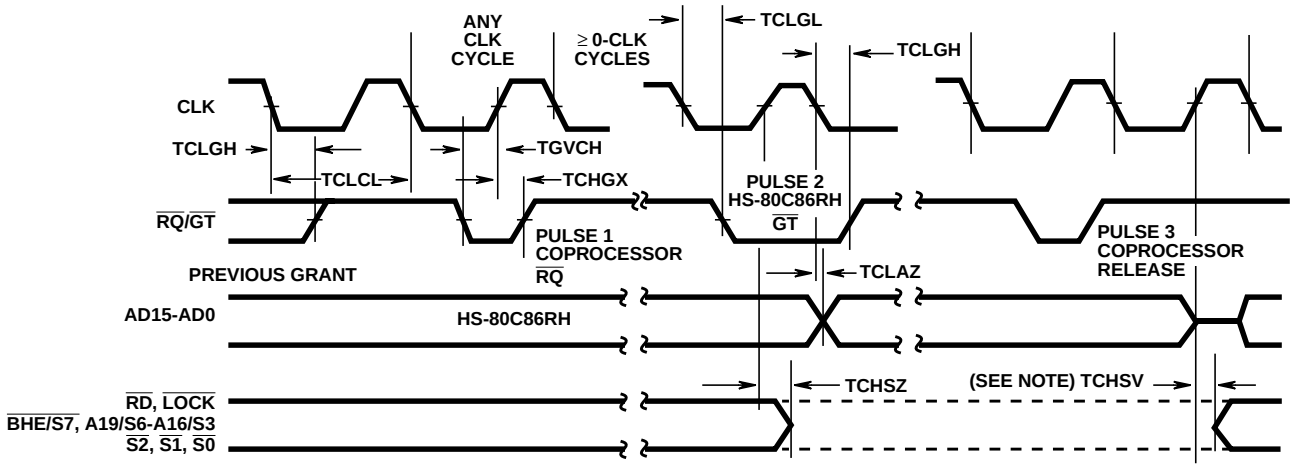


FIGURE 13. RESET TIMING



NOTE: The coprocessor may not drive the buses outside the region shown without risking contention.

FIGURE 14. REQUEST/GRANT SEQUENCE TIMING (MAXIMUM MODE ONLY)

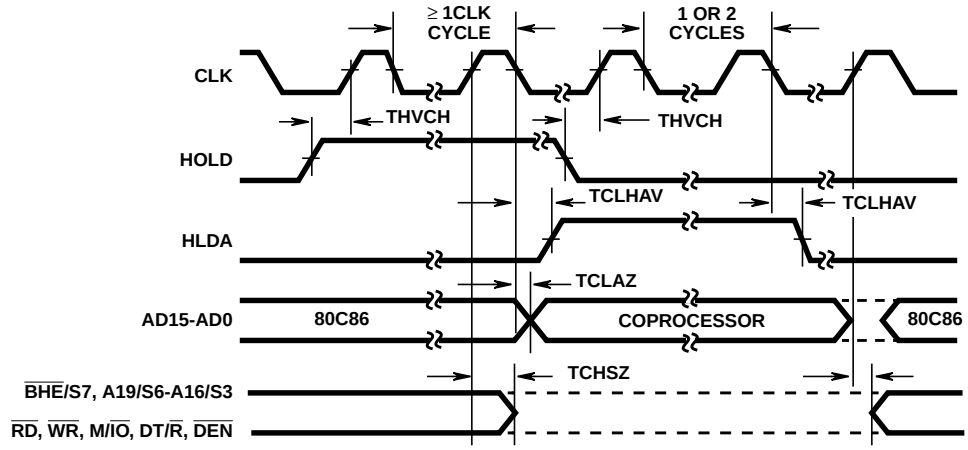
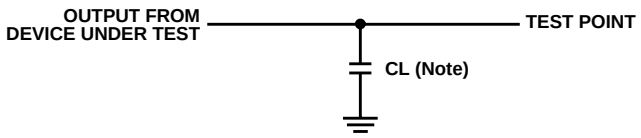


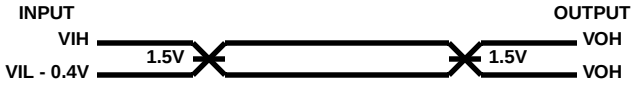
FIGURE 15. HOLD/HOLD ACKNOWLEDGE TIMING (MINIMUM MODE ONLY)

AC Test Circuit



NOTE: Includes stray and jig capacitance.

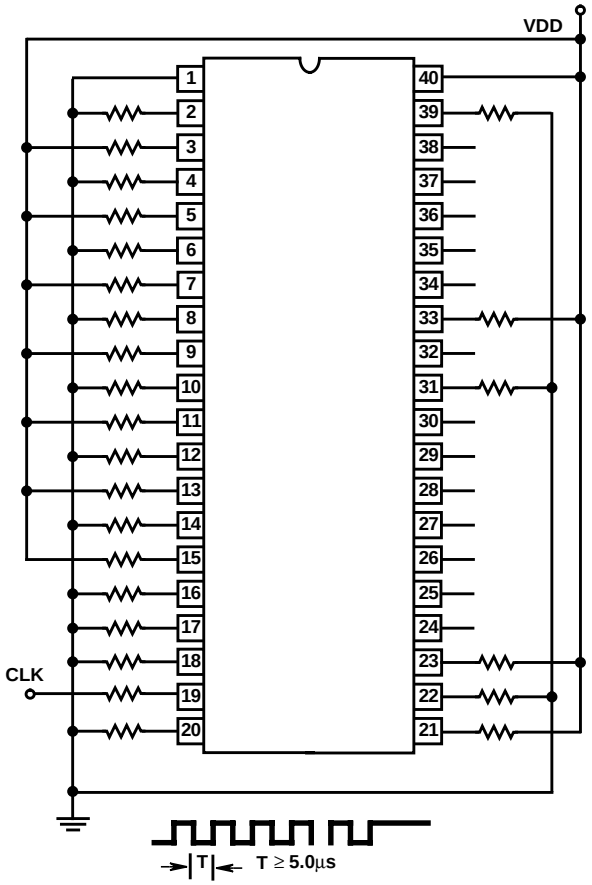
AC Testing Input, Output Waveform



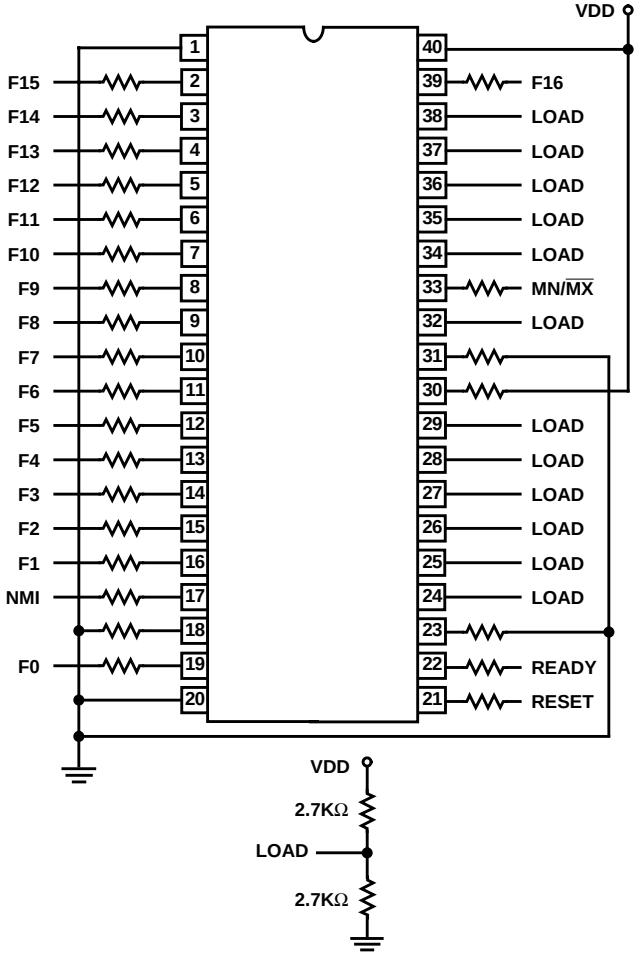
NOTE: All inputs signals (other than CLK) must switch between VIL Max -0.4V and VIH Min +0.4. CLK must switch between 0.4V and VDD -0.4V. TR and TF must be less than or equal to 15ns. CLK TR and TF must be less than or equal to 10ns.

Burn-In Circuits

HS-80C86RH 40 PIN DIP



HS-80C86RH 40 PIN DIP



STATIC

VDD = +6.5V ±10%
TA = +125°C Minimum
Part is Static Sensitive
Voltages Must Be Ramped
Package: 40 Lead DIP

Resistors:
10kΩ ±10%
(Pins 17, 18, 21-23, 31, 33)
2.7kΩ ±5% (Pins 2-16, 39)
1.0kΩ ±5% 1/10W Min (Pin 19)
Minimum of 5 CLK Pulses
After Initial Pulses, CLK is Left High
Pulses are 50% Duty Cycle Square Wave

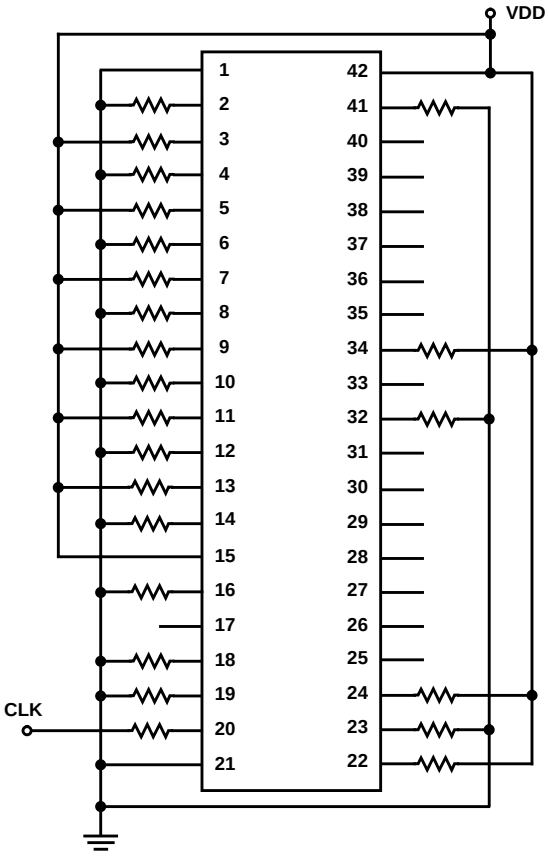
DYNAMIC

VDD = 6.5V ±5% (Burn-In)
VDD = 6.0V ±5% (Life Test)
TA = +125°C
Package: 40 Lead DIP
Part is Static Sensitive
Voltage Must Be Ramped

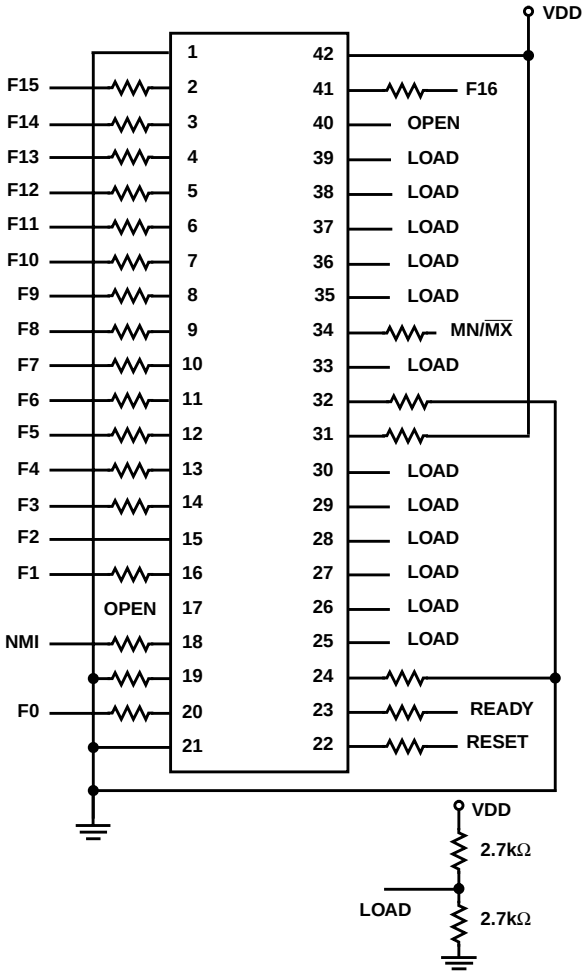
Resistors:
10kΩ (Pins 17, 18, 21, 22, 23, 33)
3.3kΩ (Pins 2-16, 19, 30, 31, 39)
2.7kΩ Loads As Indicated
All Resistors Are At Least 1/8W, ±10%
F0 = 100kHz, F1 = F0/2, F2 = F1/2 . . .
RESET, NMI low after initialization.
READY pulsed low every 320ms
MN/MX changes state every 5.24s

Burn-In Circuits (Continued)

HS-80C86RH 42 LEAD FLATPACK



HS-80C86RH 42 LEAD FLATPACK



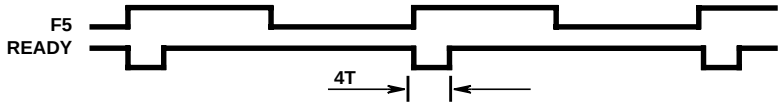
STATIC

VDD = +6.5V ±10%	Resistors:
TA = +125°C Minimum	10kΩ ±10%
Part is Static Sensitive	(Pins 18, 19, 22-24, 32, 34)
Voltages Must Be Ramped	2.7kΩ ±5% (Pins 2-16, 41)
Package: 42 Lead Flatpack	1.0kΩ ±5% 1/10W Min (Pin 20)
	Minimum of 5 CLK Pulses
	After Initial Pulses, CLK is Left High
	Pulses are 50% Duty Cycle Square Wave

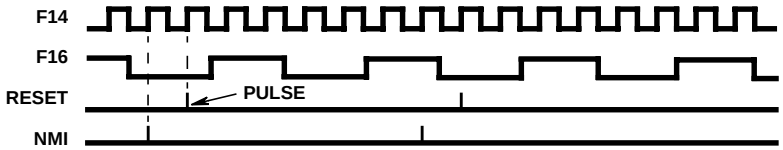
DYNAMIC

VDD = 6.5V ±5% (Burn-In)	Resistors:
VDD = 6.0V ±5% (Life Test)	10kΩ (Pins 17, 18, 19, 22, 23, 24, 34)
TA = +125°C	3.3kΩ (Pins 2-16, 20, 31, 32, 41)
Package: 42 Lead Flatpack	2.7kΩ Loads As Indicated
Part is Static Sensitive	All Resistors Are At Least 1/8W, ±10%
Voltage Must Be Ramped	F0 = 100kHz, F1 = F0/2, F2 = F1/2 . . .
	RESET, NMI low after initialization.
	READY pulsed low every 320µs
	MN/$\overline{MX}$ changes state every 5.24s

Timing Diagrams



READY TIMING AS COMPARED TO F5



RESET, NMI, AND MN/$\overline{MX}$ TIMING AS COMPARED TO F14 AND F16

F0 = 100kHz, 50% duty cycle square wave.
F1 = F0/2, F2 = F1/2 . . . F16 = F15/2.

READY, RESET, and NMI timing are as shown below:
T = 10µs.

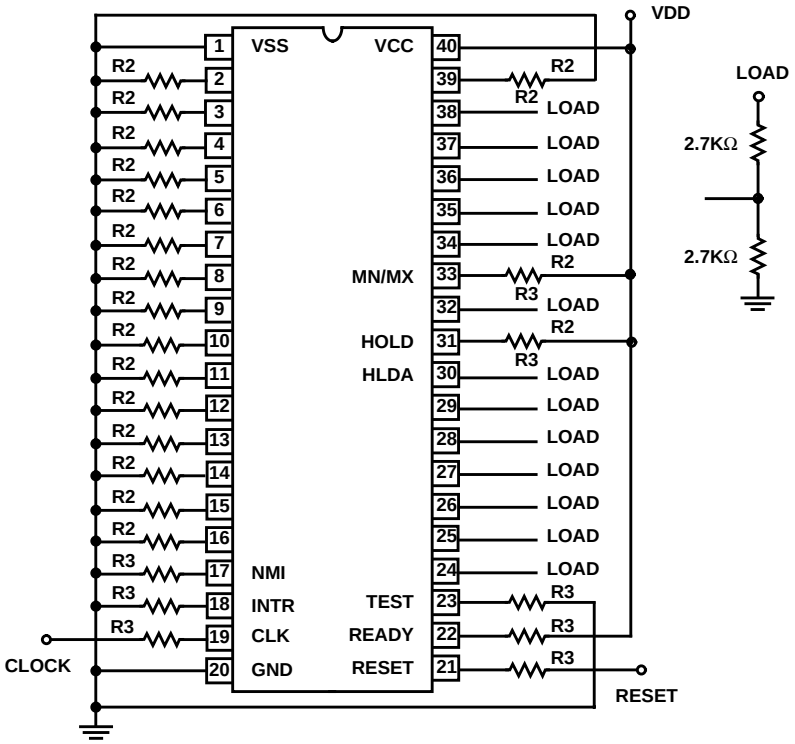
All signals have rise/fall time limits:
100ns < t-rise, t-fall < 500ns

RESET has a pulse width = 8T and occurs every two cycles of F16.

NMI has a pulse width = 4T and occurs every two cycles of F16.

MN/$\overline{MX}$ is a 50% duty cycle square wave and changes every eight cycles of F16.

Irradiation Circuit



NOTES:

1. VDD = 5.0V ± 0.5V
2. R2 = 3.3kΩ, R3 = 47kΩ
3. Pins Tied to GND: 1-18, 20, 23, 39
   Pins Tied to VCC: 22, 31, 33, 40
   Pins With Loads: 24-29, 30, 32, 34-38
   Pins Brought Out: 19 (Clock), 21 (Reset)
4. Clock and reset should be brought out separately so they can be toggled before irradiation.
5. Group E Sample Size is 2 Die/Wafer.

Intersil Space Level Product Flow - Q

All Lots - Wafer Lot Acceptance (Including SEM) Method 5007

Each Wafer - GAMMA Radiation Verification, Two samples/wafer, 0 rejects, Method 1019

100% Nondestructive Bond Pull, Method 2023

Sample - Wire Bond Pull Monitor, Method 2011

Sample - Die Shear Monitor, Method 2019 or 2027

100% Internal Visual Inspection, Method 2010, Condition A

100% Temperature Cycle - Method 1010, Condition C, 10 cycles

100% Constant Acceleration, Method 2001, Condition Per Method 5004

100% PIND - Method 2020, Condition A

100% External Visual

100% Serialization

100% Initial Electrical Test (T0)

100% Static Burn-In 1, Method 1015, Condition A or B, 72 Hours Minimum, 125^{o}C minimum

100% Interim Electrical Test 1 (T1)

100% Delta Calculation (T0-T1)

100% PDA 1, Method 5004 (Note 1)

100% Dynamic Burn-In, Condition D, 240 hours, +125^{o}C or Equivalent Per Method 1015

100% Interim Electrical Test 2 (T2)

100% Delta Calculation (T0-T2)

100% PDA 2, Method 5004 (Note 2)

100% Final Electric Test (T3)

100% Fine/Gross Leak, Method 1014

100% Radiographic, Method 2012 (Note 3)

100% External Visual, Method 2009

Sample - Group A, Method 5005 (Note 4)

Sample - Group B, Method 5005 (Note 5)

Sample - Group D, Method 5005 (Notes 5, 6)

100% Data Package Generation (Note 6)

NOTES:

1. Modified SEM Inspection, not compliant to MIL-STD-883, Method 2018. This device does not meet the Class S minimum metal step coverage of 50%. The metal does meet the current density requirement of <2 E^5 A/cm^2. Data provided upon request.
2. Failures from subgroups 1, 7 and deltas are used for calculating PDA. The maximum allowable PDA = 5% with no more than 3% of the failures from subgroup 7.
3. Radiographic (X-Ray) inspection may be performed at any point after serialization as allowed by Method 5004.
4. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
5. Group B and D inspections are optional and will not be performed unless required by the P.O. When required, the P.O. should include separate line items for Group B test, Group B samples, Group D tests and Group D samples.
6. Group D Generic Data, as defined by MIL-I-38535, is optional and will not be supplied unless required by the P.O. When required, the P.O. should include separate line items for Group D generic data. Generic Data is not guaranteed to be available and is therefore not available in all cases.
7. Data Package Contents:
   - Cover Sheet (Intersil Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Intersil Part Number, Lot Number, Quantity). Wafer Lot Acceptance Report (Method 5007) to include reproductions of SEM photos with percent of step coverage.
   - GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, test package used, specification numbers, test equipment, etc. Radiation Read and Record data on file at Intersil.
   - X-Ray Report and Film, including penetrameter measurements.
   - Lot Serial Number Sheet (Good Unit(s) Serial Number and Lot Number).
   - Variables Data (All Delta operations). Data is identified by serial number. Data header includes lot number and date of test.
   - Group B and D attributes and/or Generic data is included when required by P.O.
   - The Certificate of Conformance is a part of the shipping invoice and is not part of Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

Intersil Space Level Product Flow - 8

Each Wafer - GAMMA Radiation Verification, 2 samples/wafer, 0 rejects, Method 1019

100% Die Attach

Periodic - Wire Bond Pull Monitor, Method 2011

Periodic - Die Shear Monitor, Method 2019 or 2027

100% Internal Visual Inspection, Method 2010, Condition B

CSI and/or GSI PreCap (Note 5)

100% Temperature Cycle, Method 1010, Condition C, 10 cycles

100% Constant Acceleration, Method 2001, Condition Per Method 5004

100% External Visual

100% Initial Electrical Test

100% Dynamic Burn-In, Condition D, 160 hours, +125^{o}C, or Equivalent, Per Method 1015

100% Interim Electrical Test

100% PDA, Method 5004 (Note 1)

100% Final Electric Test

100% Fine/Gross Leak, Method 1014

100% External Visual, Method 2009

Sample - Group A, Method 5005 (Note 2)

Sample - Group B, Method 5005 (Note 3)

Sample - Group C, Method 5005 (Notes 3, 4)

Sample - Group D, Method 5005 (Notes 3, 4)

100% Data Package Generation (Note 6)

CSI and/or GSI Final (Note 5)

NOTES:

1. Failures from subgroups 1, 7 are used for calculating PDA. The maximum allowable PDA = 5%.
2. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005 may be performed.
3. Group B, C, and D inspections are optional and will not be performed unless required by the P.O. When required, the P.O. should include separate line items for Group B Test, Group C Test, Group C Samples, Group D Test and Group D Samples.
4. Group C and/or Group D Generic Data, as defined by MIL-I-38535, is optional and will not be supplied unless required by the P.O. When required, the P.O. should include separate line items for Group D generic data. Generic Data is not guaranteed to be available and is therefore not available in all cases.
5. CSI and /or GSI inspections are optional and will not be performed unless required by the P.O. When required, the P.O. should include separate line items for CSI PreCap inspection, CSI final inspection, GSI PreCap inspection, and/or GSI final inspection.
6. Data Package Contents:
   - Cover Sheet (Intersil Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Intersil Part Number, Lot Number, Quantity).
   - GAMMA Radiation Report. Contains Cover page, disposition, RAD Dose, Lot Number, test package used, specification numbers, test equipment, etc. Radiation Read and Record data on file at Intersil.
   - Screening, Electrical, and Group A attributes (Screening attributes begins at Initial Electrical Test).
   - Group B, C and D attributes and/or Generic data is included when required by P.O.
   - Variables Data (All Delta operations) Data is identified by serial number. Data header includes lot number and date of test.
   - Group B and D attributes and/or Generic data is included when required by P.O.
   - The Certificate of Conformance is a part of the shipping invoice and is not part of Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

Metallization Topology

DIE DIMENSIONS:
6370µm x 7420µm x 485µm

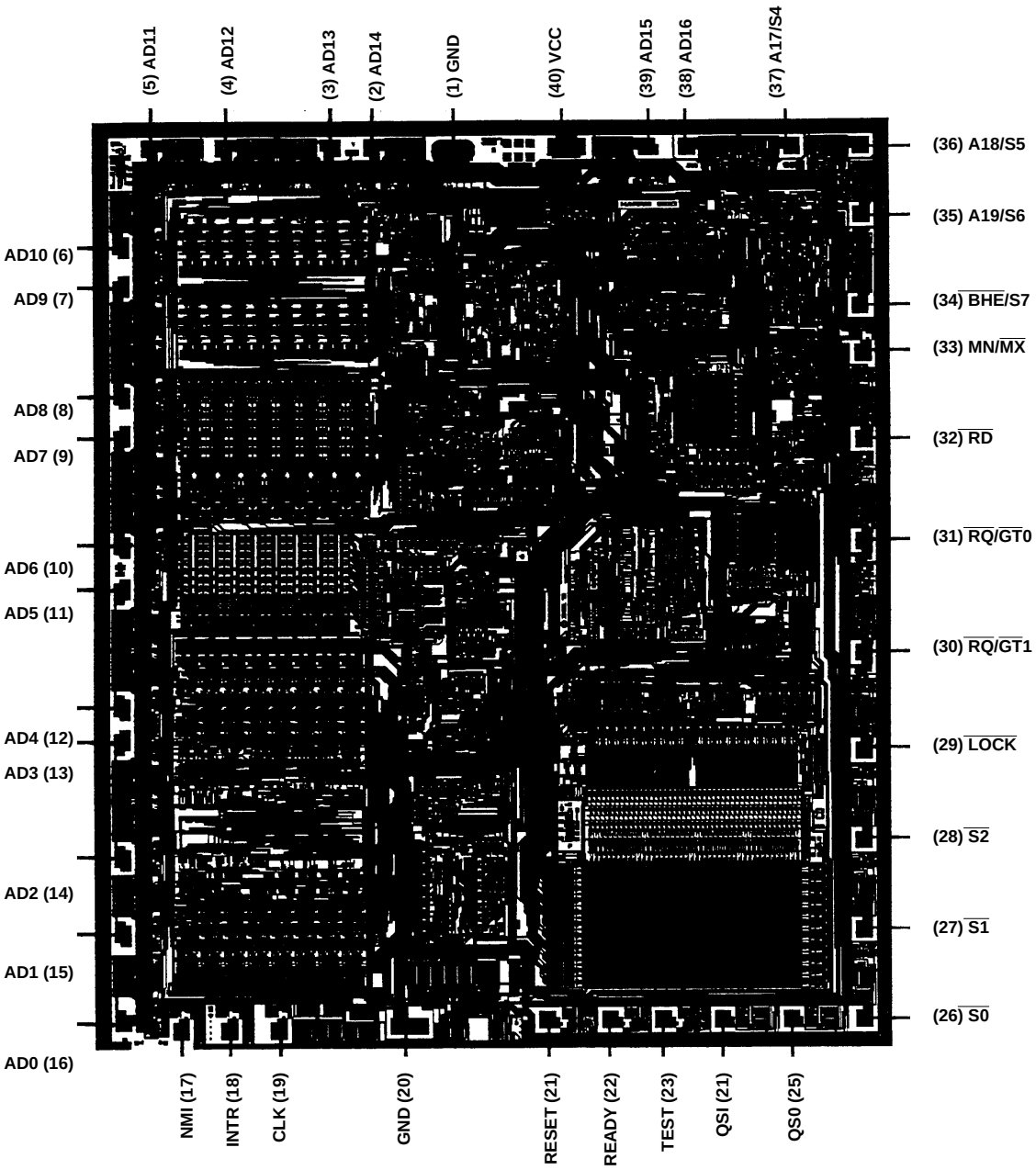
METALLIZATION:
Type: Al/S
Thickness: 11kÅ ±2kÅ

GLASSIVATION:
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:
<2 x 10^5A/cm^2

Metallization Mask Layout

HS-80C86RH



Instruction Set Summary

MNEMONIC AND DESCRIPTION	INSTRUCTION CODE			
	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
DATA TRANSFER				
MOV = MOVE:				
Register/Memory to/from Register	1 0 0 0 1 0 d w	mod reg r/m		
Immediate to Register/Memory	1 1 0 0 0 1 1 w	mod 0 0 0 r/m	data	data if w 1
Immediate to Register	1 0 1 1 w reg	data	data if w 1	
Memory to Accumulator	1 0 1 0 0 0 0 w	addr-low	addr-high	
Accumulator to Memory	1 0 1 0 0 0 1 w	addr-low	addr-high	
Register/Memory to Segment Register ††	1 0 0 0 1 1 1 0	mod 0 reg r/m		
Segment Register to Register/Memory	1 0 0 0 1 1 0 0	mod 0 reg r/m		
PUSH = Push:				
Register/Memory	1 1 1 1 1 1 1 1	mod 1 1 0 r/m		
Register	0 1 0 1 0 reg			
Segment Register	0 0 0 reg 1 1 0			
POP = Pop:				
Register/Memory	1 0 0 0 1 1 1 1	mod 0 0 0 r/m		
Register	0 1 0 1 1 reg			
Segment Register	0 0 0 reg 1 1 1			
XCHG = Exchange:				
Register/Memory with Register	1 0 0 0 0 1 1 w	mod reg r/m		
Register with Accumulator	1 0 0 1 0 reg			
IN = Input from:				
Fixed Port	1 1 1 0 0 1 0 w	port		
Variable Port	1 1 1 0 1 1 0 w			
OUT = Output to:				
Fixed Port	1 1 1 0 0 1 1 w	port		
Variable Port	1 1 1 0 1 1 1 w			
XLAT = Translate Byte to AL	1 1 0 1 0 1 1 1			
LEA = Load EA to Register2	1 0 0 0 1 1 0 1	mod reg r/m		
LDS = Load Pointer to DS	1 1 0 0 0 1 0 1	mod reg r/m		
LES = Load Pointer to ES	1 1 0 0 0 1 0 0	mod reg r/m		
LAHF = Load AH with Flags	1 0 0 1 1 1 1 1			
SAHF = Store AH into Flags	1 0 0 1 1 1 1 0			
PUSHF = Push Flags	1 0 0 1 1 1 0 0			
POPF = Pop Flags	1 0 0 1 1 1 0 1			

Instruction Set Summary (Continued)

MNEMONIC AND DESCRIPTION	INSTRUCTION CODE			
	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
ARITHMETIC				
ADD = Add:				
Register/Memory with Register to Either	0 0 0 0 0 0 d w	mod reg r/m		
Immediate to Register/Memory	1 0 0 0 0 0 s w	mod 0 0 0 r/m	data	data if s:w = 01
Immediate to Accumulator	0 0 0 0 0 1 0 w	data	data if w = 1	
ADC = Add with Carry:				
Register/Memory with Register to Either	0 0 0 1 0 0 d w	mod reg r/m		
Immediate to Register/Memory	1 0 0 0 0 0 s w	mod 0 1 0 r/m	data	data if s:w = 01
Immediate to Accumulator	0 0 0 1 0 1 0 w	data	data if w = 1	
INC = Increment:				
Register/Memory	1 1 1 1 1 1 1 w	mod 0 0 0 r/m		
Register	0 1 0 0 0 reg			
AAA = ASCII Adjust for Add	0 0 1 1 0 1 1 1			
DAA = Decimal Adjust for Add	0 0 1 0 0 1 1 1			
SUB = Subtract:				
Register/Memory and Register to Either	0 0 1 0 1 0 d w	mod reg r/m		
Immediate from Register/Memory	1 0 0 0 0 0 s w	mod 1 0 1 r/m	data	data if s:w = 01
Immediate from Accumulator	0 0 1 0 1 1 0 w	data	data if w = 1	
SBB = Subtract with Borrow				
Register/Memory and Register to Either	0 0 0 1 1 0 d w	mod reg r/m		
Immediate from Register/Memory	1 0 0 0 0 0 s w	mod 0 1 1 r/m	data	data if s:w = 01
Immediate from Accumulator	0 0 0 1 1 1 0 w	data	data if w = 1	
DEC = Decrement:				
Register/Memory	1 1 1 1 1 1 1 w	mod 0 0 1 r/m		
Register	0 1 0 0 1 reg			
NEG = Change Sign	1 1 1 1 0 1 1 w	mod 0 1 1 r/m		
CMP = Compare:				
Register/Memory and Register	0 0 1 1 1 0 d w	mod reg r/m		
Immediate with Register/Memory	1 0 0 0 0 0 s w	mod 1 1 1 r/m	data	data if s:w = 01
Immediate with Accumulator	0 0 1 1 1 1 0 w	data	data if w = 1	
AAS = ASCII Adjust for Subtract	0 0 1 1 1 1 1 1			
DAS = Decimal Adjust for Subtract	0 0 1 0 1 1 1 1			
MUL = Multiply (Unsigned)	1 1 1 1 0 1 1 w	mod 1 0 0 r/m		
IMUL = Integer Multiply (Signed)	1 1 1 1 0 1 1 w	mod 1 0 1 r/m		
AAM = ASCII Adjust for Multiply	1 1 0 1 0 1 0 0	0 0 0 0 1 0 1 0		
DIV = Divide (Unsigned)	1 1 1 1 0 1 1 w	mod 1 1 0 r/m		
IDIV = Integer Divide (Signed)	1 1 1 1 0 1 1 w	mod 1 1 1 r/m		
AAD = ASCII Adjust for Divide	1 1 0 1 0 1 0 1	0 0 0 0 1 0 1 0		
CBW = Convert Byte to Word	1 0 0 1 1 0 0 0			
CWD = Convert Word to Double Word	1 0 0 1 1 0 0 1			

Instruction Set Summary (Continued)

MNEMONIC AND DESCRIPTION	INSTRUCTION CODE			
	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
LOGIC				
NOT = Invert	1 1 1 1 0 1 1 w	mod 0 1 0 r/m		
SHL/SAL = Shift Logical/Arithmetic Left	1 1 0 1 0 0 v w	mod 1 0 0 r/m		
SHR = Shift Logical Right	1 1 0 1 0 0 v w	mod 1 0 1 r/m		
SAR = Shift Arithmetic Right	1 1 0 1 0 0 v w	mod 1 1 1 r/m		
ROL = Rotate Left	1 1 0 1 0 0 v w	mod 0 0 0 r/m		
ROR = Rotate Right	1 1 0 1 0 0 v w	mod 0 0 1 r/m		
RCL = Rotate Through Carry Flag Left	1 1 0 1 0 0 v w	mod 0 1 0 r/m		
RCR = Rotate Through Carry Right	1 1 0 1 0 0 v w	mod 0 1 1 r/m		
AND = And:				
Reg./Memory and Register to Either	0 0 1 0 0 0 0 d w	mod reg r/m		
Immediate to Register/Memory	1 0 0 0 0 0 0 w	mod 1 0 0 r/m	data	data if w = 1
Immediate to Accumulator	0 0 1 0 0 1 0 w	data	data if w = 1	
TEST = And Function to Flags, No Result:				
Register/Memory and Register	1 0 0 0 0 1 0 w	mod reg r/m		
Immediate Data and Register/Memory	1 1 1 1 0 1 1 w	mod 0 0 0 r/m	data	data if w = 1
Immediate Data and Accumulator	1 0 1 0 1 0 0 w	data	data if w = 1	
OR = Or:				
Register/Memory and Register to Either	0 0 0 0 1 0 d w	mod reg r/m		
Immediate to Register/Memory	1 0 0 0 0 0 0 w	mod 1 0 1 r/m	data	data if w = 1
Immediate to Accumulator	0 0 0 0 1 1 0 w	data	data if w = 1	
XOR = Exclusive or:				
Register/Memory and Register to Either	0 0 1 1 0 0 d w	mod reg r/m		
Immediate to Register/Memory	1 0 0 0 0 0 0 w	mod 1 1 0 r/m	data	data if w = 1
Immediate to Accumulator	0 0 1 1 0 1 0 w	data	data if w = 1	
STRING MANIPULATION				
REP = Repeat	1 1 1 1 0 0 1 z			
MOVS = Move Byte/Word	1 0 1 0 0 1 0 w			
CMPS = Compare Byte/Word	1 0 1 0 0 1 1 w			
SCAS = Scan Byte/Word	1 0 1 0 1 1 1 w			
LODS = Load Byte/Word to AL/AX	1 0 1 0 1 1 0 w			
STOS = Stor Byte/Word from AL/A	1 0 1 0 1 0 1 w			
CONTROL TRANSFER				
CALL = Call:				
Direct Within Segment	1 1 1 0 1 0 0 0	disp-low	disp-high	
Indirect Within Segment	1 1 1 1 1 1 1 1	mod 0 1 0 r/m		
Direct Intersegment	1 0 0 1 1 0 1 0	offset-low	offset-high	
		seg-low	seg-high	
Indirect Intersegment	1 1 1 1 1 1 1 1	mod 0 1 1 r/m		

Instruction Set Summary (Continued)

MNEMONIC AND DESCRIPTION	INSTRUCTION CODE			
	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
JMP = Unconditional Jump:				
Direct Within Segment	1 1 1 0 1 0 0 1	disp-low	disp-high	
Direct Within Segment-Short	1 1 1 0 1 0 1 1	disp		
Indirect Within Segment	1 1 1 1 1 1 1 1	mod 1 0 0 r/m		
Direct Intersegment	1 1 1 0 1 0 1 0	offset-low	offset-high	
Direct Intersegment	1 1 1 0 1 0 1 0	offset-low	offset-high	
		seg-low	seg-high	
Indirect Intersegment	1 1 1 1 1 1 1 1	mod 1 0 1 r/m		
RET = Return from CALL:				
Within Segment	1 1 0 0 0 0 1 1			
Within Seg Adding Immed to SP	1 1 0 0 0 0 1 0	data-low	data-high	
Intersegment	1 1 0 0 1 0 1 1			
Intersegment Adding Immediate to SP	1 1 0 0 1 0 1 0	data-low	data-high	
JE/JZ = Jump on Equal/Zero	0 1 1 1 0 1 0 0	disp		
JL/JNGE = Jump on Less/Not Greater or Equal	0 1 1 1 1 1 0 0	disp		
JLE/JNG = Jump on Less or Equal/ Not Greater	0 1 1 1 1 1 1 0	disp		
JB/JNAE = Jump on Below/Not Above or Equal	0 1 1 1 0 0 1 0	disp		
JBE/JNA = Jump on Below or Equal/Not Above	0 1 1 1 0 1 1 0	disp		
JP/JPE = Jump on Parity/Parity Even	0 1 1 1 1 0 1 0	disp		
JO = Jump on Overtlow	0 1 1 1 0 0 0 0	disp		
JS = Jump on Sign	0 1 1 1 1 0 0 0	disp		
JNE/JNZ = Jump on Not Equal/Not Zero	0 1 1 1 0 1 0 1	disp		
JNL/JGE = Jump on Not Less/Greater or Equal	0 1 1 1 1 1 0 1	disp		
JNLE/JG = Jump on Not Less or Equal/Greater	0 1 1 1 1 1 1 1	disp		
JNB/JAE = Jump on Not Below/Above or Equal	0 1 1 1 0 0 1 1	disp		
JNBE/JA = Jump on Not Below or Equal/Above	0 1 1 1 0 1 1 1	disp		
JNP/JPO = Jump on Not Par/Par Odd	0 1 1 1 1 0 1 1	disp		
JNO = Jump on Not Overflow	0 1 1 1 0 0 0 1	disp		
JNS = Jump on Not Sign	0 1 1 1 1 0 0 1	disp		
LOOP = Loop CX Times	1 1 1 0 0 0 1 0	disp		
LOOPZ/LOOPE = Loop While Zero/Equal	1 1 1 0 0 0 0 1	disp		
LOOPNZ/LOOPNE = Loop While Not Zero/Equal	1 1 1 0 0 0 0 0	disp		
JCXZ = Jump on CX Zero	1 1 1 0 0 0 1 1	disp		
INT = Interrupt				
Type Specified	1 1 0 0 1 1 0 1	type		
Type 3	1 1 0 0 1 1 0 0			
INTO = Interrupt on Overflow	1 1 0 0 1 1 1 0			
IRET = Interrupt Return	1 1 0 0 1 1 1 1			

Instruction Set Summary (Continued)

MNEMONIC AND DESCRIPTION	INSTRUCTION CODE			
	76543210	76543210	76543210	76543210
PROCESSOR CONTROL				
CLC = Clear Carry	11111000			
CMC = Complement Carry	11110101			
STC = Set Carry	11111001			
CLD = Clear Direction	11111100			
STD = Set Direction	11111101			
CLI = Clear Interrupt	11111010			
ST = Set Interrupt	11111011			
HLT = Halt	11110100			
WAIT = Wait	10011011			
ESC = Escape (to External Device)	11011xxx	mod x x x r/m		
LOCK = Bus Lock Prefix	11110000			

NOTES:
AL = 8-bit accumulator
AX = 16-bit accumulator
CX = Count register
DS= Data segment
ES = Extra segment
Above/below refers to unsigned value.
Greater = more positive;
Less = less positive (more negative) signed values
if d = 1 then “to” reg; if d = 0 then “from” reg
if w = 1 then word instruction; if w = 0 then byte instruction
if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = O†, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high:disp-low
if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP †
if r/m = 111 then EA = (BX) + DISP
DISP follows 2nd byte of instruction (before data if required)
† except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.
†† MOV CS, REG/MEMORY not allowed.

if s:w = 01 then 16 bits of immediate data form the operand.
if s:w. = 11 then an immediate data byte is sign extended to form the 16-bit operand.
if v = 0 then “count” = 1; if v = 1 then “count” in (CL)
x = don't care
z is used for string primitives for comparison with ZF FLAG.

SEGMENT OVERRIDE PREFIX

001 reg 11 0

REG is assigned according to the following table:

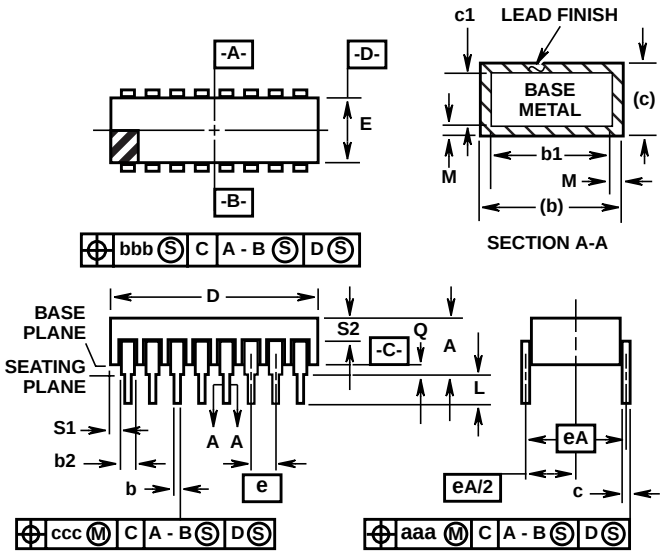
16-BIT (w = 1)	8-BIT (w = 0)	SEGMENT
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	00 ES
101 BP	101 CH	00 ES
110 SI	110 DH	00 ES
111 DI	111 BH	00 ES

Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:

FLAGS =

X:X:X:X:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



D40.6 MIL-STD-1835 CDIP2-T40 (D-5, CONFIGURATION C)
40 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

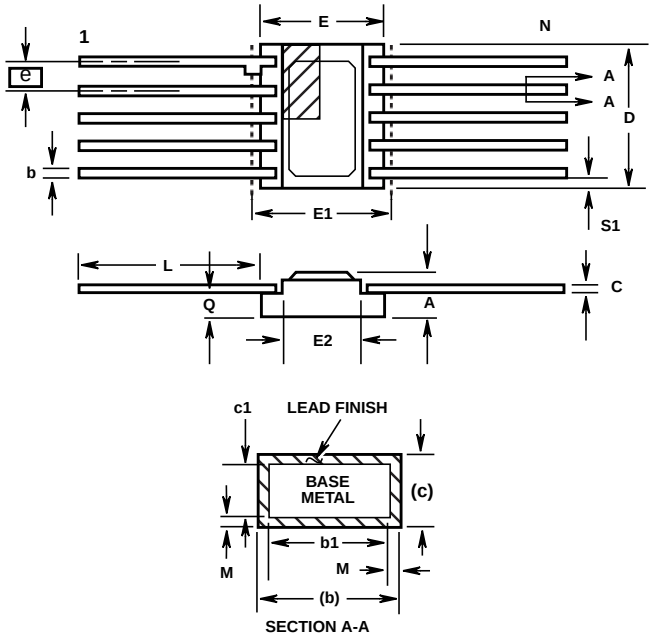
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.225	-	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	2.096	-	53.24	4
E	0.510	0.620	12.95	15.75	4
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.070	0.38	1.78	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	40		40		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

Ceramic Metal Seal Flatpack Packages (Flatpack)



K42.A TOP BRAZED
42 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.100	-	2.54	-
b	0.017	0.025	0.43	0.64	-
b1	0.017	0.023	0.43	0.58	-
c	0.007	0.013	0.18	0.33	-
c1	0.007	0.010	0.18	0.25	-
D	1.045	1.075	26.54	27.31	3
E	0.630	0.650	16.00	16.51	-
E1	-	0.680	-	17.27	3
E2	0.530	0.550	13.46	13.97	-
e	0.050 BSC		1.27 BSC		11
k	-	-	-	-	-
L	0.320	0.350	8.13	8.89	-
Q	0.045	0.065	1.14	1.65	8
S1	0.000	-	0.00	-	6
M	-	0.0015	-	0.04	-
N	42		42		-

Rev. 0 6/17/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.
11. The basic lead spacing is 0.050 inch (1.27mm) between center lines. Each lead centerline shall be located within ±0.005 inch (0.13mm) of its exact longitudinal position relative to lead 1 and the highest numbered (N) lead.

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