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Preliminary

Mobile Pentium® Processor with MMX™ Technology

SmartDie® Product Specification

- **Support for MMX™ Technology**
- **Compatible with Large Software Base**
  - **MS-DOS*, Windows*, OS/2*, UNIX***
- **32-Bit Processor with 64-Bit Data Bus**
- **Superscalar Architecture**
  - **Enhanced Pipelines**
  - **Two Pipelined Integer Units Are Capable of Two Instructions/Clock**
  - **Pipelined MMX Unit**
  - **Pipelined Floating Point Unit**
- **Separate Code and Data Caches**
  - **16 Kbyte Code, 16 Kbyte Writeback Data**
  - **MESI Cache Protocol**
- **Advanced Design Features**
  - **Deeper Write Buffers**
  - **Enhanced Branch Prediction Feature**
  - **Virtual Mode Extensions**
- **Low Voltage CMOS Silicon Technology**
- **4 Mbyte Pages for Increased TLB Hit Rate**
- **IEEE 1149.1 Boundary Scan**
- **Internal Error Detection Features**
- **Power Management Features**
  - **System Management Mode**
  - **Clock Control**
- **Voltage Reduction Technology**
  - **2.45 V V_{CC} for Core Supply**
  - **3.3 V V_{CC} for I/O Buffer Supply**
- **Fractional Bus Operation**
  - **150-MHz Core/60-MHz Bus**
  - **166-MHz Core/66-MHz Bus**
- **Intel SmartDie® Product**
  - **Full AC/DC Testing at Die Level**
  - **0°C to 105°C (Junction) Temperature Range**

NOTICE: This document contains preliminary information on new products in production. It is valid for the devices indicated in "DEVICE NOMENCLATURE" on page 18. This specification is subject to change without notice. Verify with your local Intel sales office that you have the latest product specification before finalizing a design.

REFERENCE INFORMATION: The information in this document is provided as a supplement to the standard package datasheet on a specific product. Please refer to the standard package datasheet (order number 243292) for product information and specifications not found in this document.

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February 1997 **Order Number:** 272998-001

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The Mobile Pentium® Processor with MMX™ Technology may contain design defects or errors known as errata. Current characterized errata are available on request.

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Mobile Pentium® Processor with MMX™ Technology

SmartDie® Product Specification

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1.0 DIE SPECIFICATIONS

The die photo in Figure 1 and the plot in Figure 2 indicate the orientation of the die in the GEL-PAK* (shipping container). Die are aligned as shown relative to a 45° notch which is in one corner of the GEL-PAK. An Intel internal manufacturing name "80P55C" appears on the die. Table 1 describes the bond pad number and pad center data for each signal.

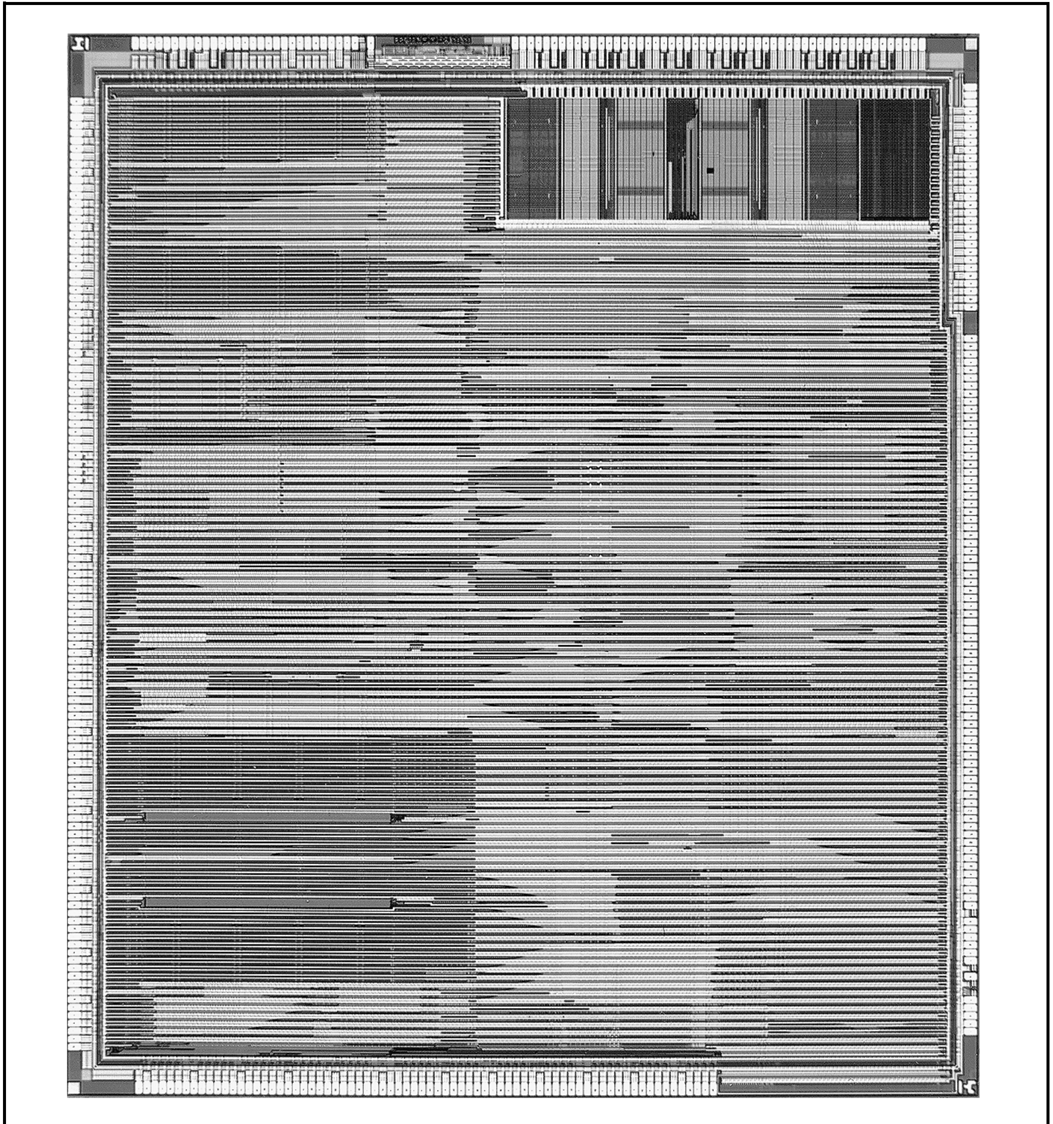

Figure 1. Mobile Pentium® Processor with MMX™ Technology Die Photo

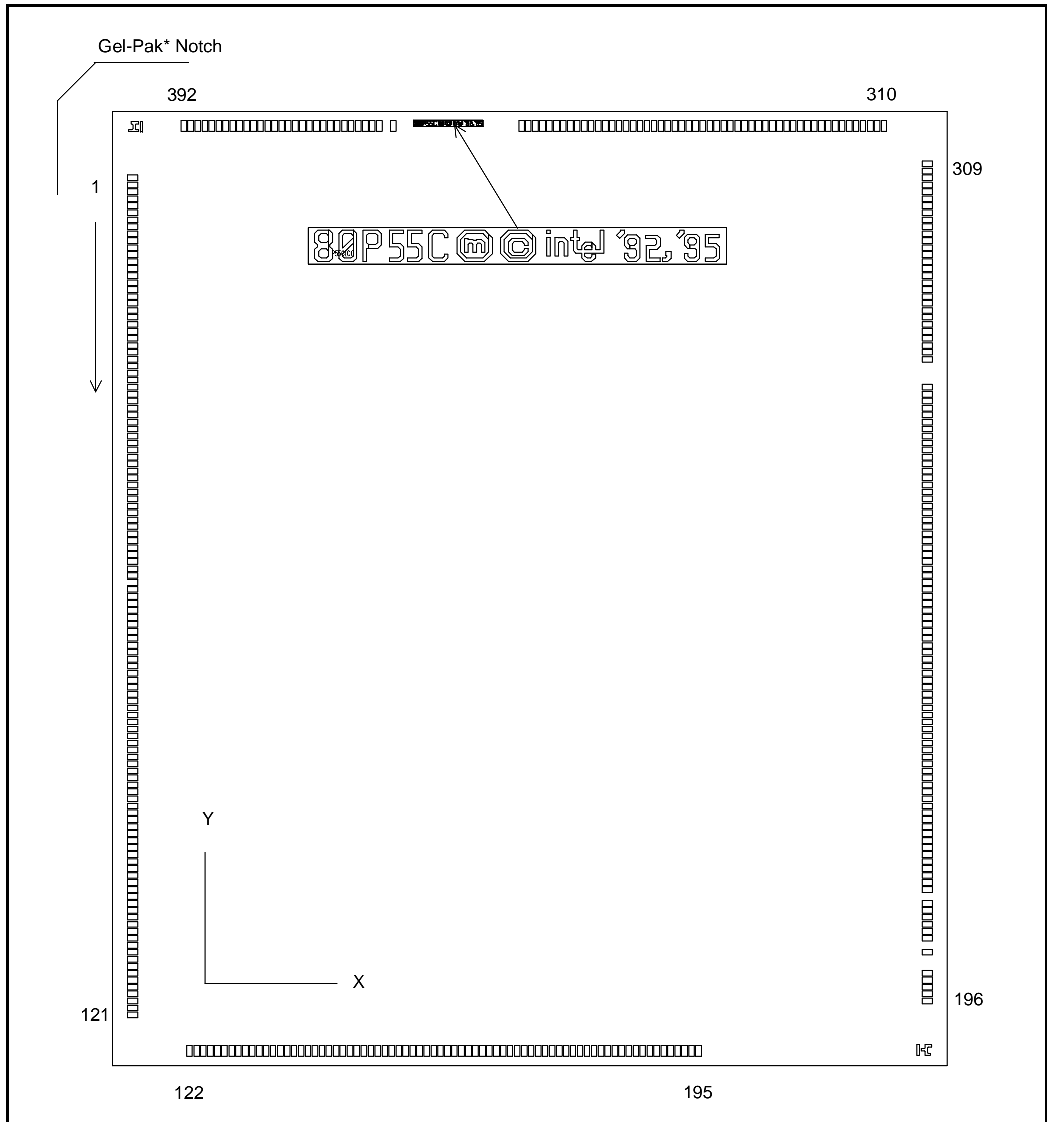

Figure 2. Mobile Pentium® Processor with MMX™ Technology Die/Bond Pad Layout

Table 1. Mobile Pentium® Processor with MMX™ Technology Bond Pad Center Data (Sheet 1 of 13)

PAD#	SIGNAL(2,3,5)	Pad Center(1)			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
001	N.C.	-210.9	217.8	-5358	5533
002	VSS	-210.9	214.1	-5358	5439
003	VCC2	-210.9	210.4	-5358	5345
004	VCC3	-210.9	206.7	-5358	5251
005	VSS	-210.9	203.0	-5358	5157
006	LOCK#	-210.9	199.3	-5358	5063
007	VCC2	-210.9	195.6	-5358	4969
008	VSS	-210.9	191.9	-5358	4875
009	VCC3	-210.9	188.2	-5358	4781
010	VSS	-210.9	184.5	-5358	4687
011	AP	-210.9	180.8	-5358	4593
012	VCC2	-210.9	177.1	-5358	4499
013	VSS	-210.9	173.4	-5358	4405
014	HLDA	-210.9	169.7	-5358	4311
015	BREQ	-210.9	166.0	-5358	4217
016	VCC3	-210.9	162.3	-5358	4123
017	VSS	-210.9	158.6	-5358	4029
018	APCHK#	-210.9	154.9	-5358	3935
019	PCHK#	-210.9	151.2	-5358	3841
020	PRDY	-210.9	147.5	-5358	3747
021	SMIACT#	-210.9	143.8	-5358	3653
022	VSS	-210.9	140.1	-5358	3559
023	VCC2	-210.9	136.4	-5358	3465
024	VCC2	-210.9	132.7	-5358	3371
025	VSS	-210.9	129.0	-5358	3277
026	N.C.	-210.9	125.3	-5358	3183
027	VCC3	-210.9	121.6	-5358	3089
028	VSS	-210.9	117.9	-5358	2995
029	N.C.	-210.9	114.2	-5358	2901
030	N.C.	-210.9	110.5	-5358	2807

NOTES:
1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol “#” is used to denote active low signals.
4. Boundary Scan (JTAG) is implemented through the following pads:
   208 (TDO), 207 (TCK), 209 (TDI), 210 (TMS), 215 (TRST#)
5. FRCMC# - Can use an external pull-up for compatibility with other Pentium processors.

Table 1. Mobile Pentium® Processor with MMX™ Technology Bond Pad Center Data (Sheet 2 of 13)

PAD#	SIGNAL(2,3,5)	Pad Center(1)			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
031	N.C.	-210.9	106.8	-5358	2713
032	HOLD	-210.9	103.1	-5358	2619
033	WB/WT#	-210.9	99.4	-5358	2525
034	VSS	-210.9	95.7	-5358	2431
035	VCC2	-210.9	92.0	-5358	2337
036	VCC2	-210.9	88.3	-5358	2243
037	VSS	-210.9	84.6	-5358	2149
038	NA#	-210.9	80.9	-5358	2055
039	BOFF#	-210.9	77.2	-5358	1961
040	N.C.	-210.9	73.5	-5358	1867
041	BRDY#	-210.9	69.8	-5358	1773
042	VSS	-210.9	66.1	-5358	1679
043	VCC2	-210.9	62.4	-5358	1585
044	VCC2	-210.9	58.7	-5358	1491
045	VSS	-210.9	55.0	-5358	1397
046	KEN#	-210.9	51.3	-5358	1303
047	AHOLD	-210.9	47.6	-5358	1209
048	INV	-210.9	43.9	-5358	1115
049	EWBE#	-210.9	40.2	-5358	1021
050	VSS	-210.9	36.5	-5358	927
051	VCC2	-210.9	32.8	-5358	833
052	VCC2	-210.9	29.1	-5358	739
053	VSS	-210.9	25.4	-5358	645
054	VCC3	-210.9	21.7	-5358	551
055	VSS	-210.9	18.0	-5358	457
056	CACHE#	-210.9	14.3	-5358	363
057	M/IO#	-210.9	10.6	-5358	269
058	VCC3	-210.9	6.9	-5358	175
059	VSS	-210.9	3.2	-5358	81
060	BP3	-210.9	-0.5	-5358	-13
061	BP2	-210.9	-4.2	-5358	-107

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol “#” is used to denote active low signals.
4. Boundary Scan (JTAG) is implemented through the following pads:
   208 (TDO), 207 (TCK), 209 (TDI), 210 (TMS), 215 (TRST#)
5. FRCMC# - Can use an external pull-up for compatibility with other Pentium processors.

Table 1. Mobile Pentium® Processor with MMX™ Technology Bond Pad Center Data (Sheet 3 of 13)

PAD#	SIGNAL(2,3,5)	Pad Center(1)			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
062	PM1/BP1	-210.9	-7.9	-5358	-201
063	PM0/BP0	-210.9	-11.6	-5358	-295
064	FERR#	-210.9	-15.3	-5358	-389
065	VSS	-210.9	-19.0	-5358	-483
066	VCC2	-210.9	-22.7	-5358	-577
067	VCC2	-210.9	-26.4	-5358	-671
068	VSS	-210.9	-30.1	-5358	-765
069	IERR#	-210.9	-33.8	-5358	-859
070	VCC3	-210.9	-37.5	-5358	-953
071	VSS	-210.9	-41.2	-5358	-1047
072	DP7	-210.9	-44.9	-5358	-1141
073	D63	-210.9	-48.6	-5358	-1235
074	D62	-210.9	-52.3	-5358	-1329
075	D61	-210.9	-56.0	-5358	-1423
076	VSS	-210.9	-59.7	-5358	-1517
077	VCC2	-210.9	-63.4	-5358	-1611
078	VCC2	-210.9	-67.1	-5358	-1705
079	VSS	-210.9	-70.8	-5358	-1799
080	VCC3	-210.9	-74.5	-5358	-1893
081	VSS	-210.9	-78.2	-5358	-1987
082	D60	-210.9	-81.9	-5358	-2081
083	D59	-210.9	-85.6	-5358	-2175
084	D58	-210.9	-89.3	-5358	-2269
085	D57	-210.9	-93.0	-5358	-2363
086	VSS	-210.9	-96.7	-5358	-2457
087	VCC2	-210.9	-100.4	-5358	-2551
088	VCC2	-210.9	-104.1	-5358	-2645
089	VSS	-210.9	-107.8	-5358	-2739
090	VCC3	-210.9	-111.5	-5358	-2833
091	VSS	-210.9	-115.2	-5358	-2927
092	D56	-210.9	-118.9	5358	-3021

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol "#" is used to denote active low signals.
4. Boundary Scan (JTAG) is implemented through the following pads:
   208 (TDO), 207 (TCK), 209 (TDI), 210 (TMS), 215 (TRST#)
5. FRCMC# - Can use an external pull-up for compatibility with other Pentium processors.

Table 1. Mobile Pentium® Processor with MMX™ Technology Bond Pad Center Data (Sheet 4 of 13)

PAD#	SIGNAL(2,3,5)	Pad Center(1)			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
093	DP6	-210.9	-122.6	-5358	-3115
094	D55	-210.9	-126.3	-5358	-3209
095	D54	-210.9	-130.0	-5358	-3303
096	VSS	-210.9	-133.7	-5358	-3397
097	VCC2	-210.9	-137.4	-5358	-3491
098	VCC2	-210.9	-141.1	-5358	-3585
099	VSS	-210.9	-144.8	-5358	-3679
100	VCC3	-210.9	-148.5	-5358	-3773
101	VSS	-210.9	-152.2	-5358	-3867
102	D53	-210.9	-155.9	-5358	-3961
103	D52	-210.9	-159.6	-5358	-4055
104	D51	-210.9	-163.3	-5358	-4149
105	D50	-210.9	-167.0	-5358	-4243
106	VCC2	-210.9	-170.7	-5358	-4337
107	VSS	-210.9	-174.4	-5358	-4431
108	VCC3	-210.9	-178.1	-5358	-4525
109	VSS	-210.9	-181.8	-5358	-4619
110	D49	-210.9	-185.5	-5358	-4713
111	D48	-210.9	-189.3	-5358	-4807
112	DP5	-210.9	-193.0	-5358	-4901
113	D47	-210.9	-196.7	-5358	-4995
114	VCC3	-210.9	-200.4	-5358	-5089
115	VSS	-210.9	-204.1	-5358	-5183
116	D46	-210.9	-207.8	-5358	-5277
117	D45	-210.9	-211.5	-5358	-5371
118	D44	-210.9	-215.2	-5358	-5465
119	D43	-210.9	-218.9	-5358	-5559
120	VSS	-210.9	-222.6	-5358	-5653
121	VCC2	-210.9	-226.3	-5358	-5747
122	VCC3	-180.6	-245.4	-4588	-6232
123	VSS	-176.9	-245.4	-4494	-6232

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol "#" is used to denote active low signals.
4. Boundary Scan (JTAG) is implemented through the following pads:
   208 (TDO), 207 (TCK), 209 (TDI), 210 (TMS), 215 (TRST#)
5. FRCMC# - Can use an external pull-up for compatibility with other Pentium processors.

Table 1. Mobile Pentium® Processor with MMX™ Technology Bond Pad Center Data (Sheet 5 of 13)

PAD#	SIGNAL(2,3,5)	Pad Center(1)			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
124	D42	-173.2	-245.4	-4400	-6232
125	D41	-169.5	-245.4	-4306	-6232
126	D40	-165.8	-245.4	-4212	-6232
127	DP4	-162.1	-245.4	-4118	-6232
128	VCC3	-158.4	-245.4	-4024	-6232
129	VSS	-154.7	-245.4	-3930	-6232
130	D39	-151.0	-245.4	-3836	-6232
131	D38	-147.3	-245.4	-3742	-6232
132	D37	-143.6	-245.4	-3648	-6232
133	D36	-139.9	-245.4	-3554	-6232
134	VCC3	-136.2	-245.4	-3460	-6232
135	VSS	-132.5	-245.4	-3366	-6232
136	D35	-128.8	-245.4	-3272	-6232
137	D34	-125.1	-245.4	-3178	-6232
138	D33	-121.4	-245.4	-3084	-6232
139	D32	-117.7	-245.4	-2990	-6232
140	VCC3	-114.0	-245.4	-2896	-6232
141	VSS	-110.3	-245.4	-2802	-6232
142	DP3	-106.6	-245.4	-2708	-6232
143	D31	-102.9	-245.4	-2614	-6232
144	D30	-99.2	-245.4	-2520	-6232
145	D29	-95.5	-245.4	-2426	-6232
146	VCC3	-91.8	-245.4	-2332	-6232
147	VSS	-88.1	-245.4	-2238	-6232
148	D28	-84.4	-245.4	-2144	-6232
149	D27	-80.7	-245.4	-2050	-6232
150	D26	-77.0	-245.4	-1956	-6232
151	D25	-73.3	-245.4	-1862	-6232
152	VCC3	-69.6	-245.4	-1768	-6232
153	VSS	-65.9	-245.4	-1674	-6232
154	VCC2	-62.2	-245.4	-1580	-6232

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol "#" is used to denote active low signals.
4. Boundary Scan (JTAG) is implemented through the following pads:
   208 (TDO), 207 (TCK), 209 (TDI), 210 (TMS), 215 (TRST#)
5. FRCMC# - Can use an external pull-up for compatibility with other Pentium processors.

Table 1. Mobile Pentium® Processor with MMX™ Technology Bond Pad Center Data (Sheet 6 of 13)

PAD#	SIGNAL(2,3,5)	Pad Center(1)			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
155	VSS	-58.5	-245.4	-1486	-6232
156	D24	-54.8	-245.4	-1392	-6232
157	DP2	-51.1	-245.4	-1298	-6232
158	D23	-47.4	-245.4	-1204	-6232
159	D22	-43.7	-245.4	-1110	-6232
160	VCC3	-40.0	-245.4	-1016	-6232
161	VSS	-36.3	-245.4	-922	-6232
162	D21	-32.6	-245.4	-828	-6232
163	D20	-28.9	-245.4	-734	-6232
164	D19	-25.2	-245.4	-640	-6232
165	D18	-21.5	-245.4	-546	-6232
166	VCC3	-17.8	-245.4	-452	-6232
167	VSS	-14.1	-245.4	-358	-6232
168	D17	-10.4	-245.4	-264	-6232
169	D16	-6.7	-245.4	-170	-6232
170	DP1	-3.0	-245.4	-76	-6232
171	D15	0.7	-245.4	18	-6232
172	VCC3	4.4	-245.4	112	-6232
173	VSS	8.1	-245.4	206	-6232
174	D14	11.8	-245.4	300	-6232
175	D13	15.5	-245.4	394	-6232
176	D12	19.2	-245.4	488	-6232
177	D11	22.9	-245.4	582	-6232
178	VCC3	26.6	-245.4	676	-6232
179	VSS	30.3	-245.4	770	-6232
180	D10	34.0	-245.4	864	-6232
181	D9	37.7	-245.4	958	-6232
182	D8	41.4	-245.4	1052	-6232
183	DP0	45.1	-245.4	1146	-6232
184	VCC3	48.8	-245.4	1240	-6232
185	VSS	52.5	-245.4	1334	-6232

NOTES:
1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol "#" is used to denote active low signals.
4. Boundary Scan (JTAG) is implemented through the following pads: 208 (TDO), 207 (TCK), 209 (TDI), 210 (TMS), 215 (TRST#)
5. FRCMC# - Can use an external pull-up for compatibility with other Pentium processors.

Table 1. Mobile Pentium® Processor with MMX™ Technology Bond Pad Center Data (Sheet 7 of 13)

PAD#	SIGNAL(2,3,5)	Pad Center(1)			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
186	D7	56.2	-245.4	1428	-6232
187	D6	59.9	-245.4	1522	-6232
188	D5	63.6	-245.4	1616	-6232
189	D4	67.3	-245.4	1710	-6232
190	VCC3	71.0	-245.4	1804	-6232
191	VSS	74.7	-245.4	1898	-6232
192	D3	78.4	-245.4	1992	-6232
193	D2	82.1	-245.4	2086	-6232
194	D1	85.8	-245.4	2180	-6232
195	D0	89.5	-245.4	2274	-6232
196	VSS	210.9	-218.9	5358	-5559
197	VCC2	210.9	-215.2	5358	-5465
198	VCC2	210.9	-211.5	5358	-5371
199	VSS	210.9	-207.8	5358	-5277
200	PICCLK	210.9	-204.1	5358	-5183
201	PICD0	210.9	-193.0	5358	-4901
202	PICD1	210.9	-185.5	5358	-4713
203	VCC2	210.9	-181.8	5358	-4619
204	VSS	210.9	-178.1	5358	-4525
205	VSS	210.9	-174.4	5358	-4431
206	VCC3	210.9	-170.7	5358	-4337
207(4)	TCK	210.9	-167.0	5358	-4243
208(4)	TDO	210.9	-159.6	5358	-4055
209(4)	TDI	210.9	-155.9	5358	-3961
210(4)	TMS	210.9	-152.2	5358	-3867
211	VCC2	210.9	-148.5	5358	-3773
212	VSS	210.9	-144.8	5358	-3679
213	VSS	210.9	-141.1	5358	-3585
214	VCC2	210.9	-137.4	5358	-3491
215(4)	TRST#	210.9	-133.7	5358	-3397
216	VSS	210.9	-130.0	5358	-3303

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol “#” is used to denote active low signals.
4. Boundary Scan (JTAG) is implemented through the following pads:
   208 (TDO), 207 (TCK), 209 (TDI), 210 (TMS), 215 (TRST#)
5. FRCMC# - Can use an external pull-up for compatibility with other Pentium processors.

Table 1. Mobile Pentium® Processor with MMX™ Technology Bond Pad Center Data (Sheet 8 of 13)

PAD#	SIGNAL(2,3,5)	Pad Center(1)			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
217	VCC2	210.9	-126.3	5358	-3209
218	VCC2	210.9	-122.6	5358	-3115
219	VSS	210.9	-118.9	5358	-3021
220	N.C.	210.9	-115.2	5358	-2927
221	N.C.	210.9	-111.5	5358	-2833
222	VSS	210.9	-107.8	5358	-2739
223	VCC2	210.9	-104.1	5358	-2645
224	VCC2	210.9	-100.4	5358	-2551
225	VSS	210.9	-96.7	5358	-2457
226	N.C.	210.9	-93.0	5358	-2363
227	N.C.	210.9	-89.3	5358	-2269
228	VSS	210.9	-85.6	5358	-2175
229	VCC2	210.9	-81.9	5358	-2081
230	VCC2	210.9	-78.2	5358	-1987
231	VSS	210.9	-74.5	5358	-1893
232	VSS	210.9	-70.8	5358	-1799
233	VSS	210.9	-67.1	5358	-1705
234	VCC2	210.9	-63.4	5358	-1611
235	VCC2	210.9	-59.7	5358	-1517
236	VSS	210.9	-56.0	5358	-1423
237	N.C.	210.9	-52.3	5358	-1329
238	N.C.	210.9	-48.6	5358	-1235
239	VSS	210.9	-44.9	5358	-1141
240	VCC2	210.9	-41.2	5358	-1047
241	VCC2	210.9	-37.5	5358	-953
242	VSS	210.9	-33.8	5358	-859
243	N.C.	210.9	-30.1	5358	-765
244	N.C.	210.9	-26.4	5358	-671
245	VCC3	210.9	-22.7	5358	-577
246	VSS	210.9	-19.0	5358	-483
247	VCC2	210.9	-15.3	5358	-389

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol “#” is used to denote active low signals.
4. Boundary Scan (JTAG) is implemented through the following pads:
   208 (TDO), 207 (TCK), 209 (TDI), 210 (TMS), 215 (TRST#)
5. FRCMC# - Can use an external pull-up for compatibility with other Pentium processors.

Table 1. Mobile Pentium® Processor with MMX™ Technology Bond Pad Center Data (Sheet 9 of 13)

PAD#	SIGNAL(2,3,5)	Pad Center(1)			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
248	VCC2	210.9	-11.6	5358	-295
249	VSS	210.9	-7.9	5358	-201
250	STPCLK#	210.9	-4.2	5358	-107
251	N.C.	210.9	-0.5	5358	-13
252	VSS	210.9	3.2	5358	81
253	VCC2	210.9	6.9	5358	175
254	VCC2	210.9	10.6	5358	269
255	VSS	210.9	14.3	5358	363
256	N.C.	210.9	18.0	5358	457
257	BF1	210.9	21.7	5358	551
258	BF0	210.9	25.4	5358	645
259	VSS	210.9	29.1	5358	739
260	VCC2	210.9	32.8	5358	833
261	VCC2	210.9	36.5	5358	927
262	VSS	210.9	40.2	5358	1021
263	N.C.	210.9	43.9	5358	1115
264	N.C.	210.9	47.6	5358	1209
265	VSS	210.9	51.3	5358	1303
266	VCC2	210.9	55.0	5358	1397
267	VCC2	210.9	58.7	5358	1491
268	VSS	210.9	62.4	5358	1585
269	N.C.[5]	210.9	66.1	5358	1679
270	PEN#	210.9	69.8	5358	1773
271	INIT	210.9	73.5	5358	1867
272	IGNNE#	210.9	77.2	5358	1961
273	VSS	210.9	80.9	5358	2055
274	VCC2	210.9	84.6	5358	2149
275	VCC2	210.9	88.3	5358	2243
276	VSS	210.9	92.0	5358	2337
277	SMI#	210.9	95.7	5358	2431
278	INTR/LINT0	210.9	99.4	5358	2525

NOTES:
1. X-Y coordinates represent pad centers and are relative to center of die.
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4. Boundary Scan (JTAG) is implemented through the following pads:
   208 (TDO), 207 (TCK), 209 (TDI), 210 (TMS), 215 (TRST#)
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Table 1. Mobile Pentium® Processor with MMX™ Technology Bond Pad Center Data (Sheet 10 of 13)

PAD#	SIGNAL[2,3,5]	Pad Center[1]			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
279	R/S#	210.9	103.1	5358	2619
280	NMI/LINT1	210.9	106.8	5358	2713
281	N.C.	210.9	121.6	5358	3089
282	A21	210.9	125.3	5358	3183
283	A22	210.9	129.0	5358	3277
284	A23	210.9	132.7	5358	3371
285	VSS	210.9	136.4	5358	3465
286	VCC3	210.9	140.1	5358	3559
287	VSS	210.9	143.8	5358	3653
288	VCC2	210.9	147.5	5358	3747
289	VCC2	210.9	151.2	5358	3841
290	VSS	210.9	154.9	5358	3935
291	A24	210.9	158.6	5358	4029
292	A25	210.9	162.3	5358	4123
293	A26	210.9	166.0	5358	4217
294	A27	210.9	169.7	5358	4311
295	VSS	210.9	173.4	5358	4405
296	VCC3	210.9	177.1	5358	4499
297	A28	210.9	180.8	5358	4593
298	A29	210.9	184.5	5358	4687
299	A30	210.9	188.2	5358	4781
300	A31	210.9	191.9	5358	4875
301	VSS	210.9	195.6	5358	4969
302	VCC3	210.9	199.3	5358	5063
303	VCC2	210.9	203.0	5358	5157
304	VSS	210.9	206.7	5358	5251
305	VCC2	210.9	210.4	5358	5345
306	VSS	210.9	214.1	5358	5439
307	VSS	210.9	217.8	5358	5533
308	N.C.	210.9	221.5	5358	5627
309	N.C.	210.9	225.2	5358	5721

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
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3. The symbol “#” is used to denote active low signals.
4. Boundary Scan (JTAG) is implemented through the following pads:
   208 (TDO), 207 (TCK), 209 (TDI), 210 (TMS), 215 (TRST#)
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Table 1. Mobile Pentium® Processor with MMX™ Technology Bond Pad Center Data (Sheet 11 of 13)

PAD#	SIGNAL(2,3,5)	Pad Center(1)			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
310	VSS	188.0	245.4	4775	6232
311	VCC2	184.3	245.4	4681	6232
312	VCC2	180.6	245.4	4587	6232
313	VSS	176.9	245.4	4493	6232
314	A3	173.2	245.4	4399	6232
315	VSS	169.5	245.4	4305	6232
316	VCC3	165.8	245.4	4211	6232
317	A4	162.1	245.4	4117	6232
318	A5	158.4	245.4	4023	6232
319	VSS	154.7	245.4	3929	6232
320	VCC3	151.0	245.4	3835	6232
321	A6	147.3	245.4	3741	6232
322	A7	143.6	245.4	3647	6232
323	VSS	139.9	245.4	3553	6232
324	VCC3	136.2	245.4	3459	6232
325	A8	132.5	245.4	3365	6232
326	VSS	128.8	245.4	3271	6232
327	VCC2	125.1	245.4	3177	6232
328	VCC2	121.4	245.4	3083	6232
329	VSS	117.7	245.4	2989	6232
330	A9	114.0	245.4	2895	6232
331	VSS	110.3	245.4	2801	6232
332	VCC3	106.6	245.4	2707	6232
333	A10	102.9	245.4	2613	6232
334	A11	99.2	245.4	2519	6232
335	VSS	95.5	245.4	2425	6232
336	VCC3	91.8	245.4	2331	6232
337	A12	88.1	245.4	2237	6232
338	VCC2	84.4	245.4	2143	6232
339	VSS	80.7	245.4	2049	6232
340	A13	77.0	245.4	1955	6232

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
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3. The symbol "#" is used to denote active low signals.
4. Boundary Scan (JTAG) is implemented through the following pads:
   208 (TDO), 207 (TCK), 209 (TDI), 210 (TMS), 215 (TRST#)
5. FRCMC# - Can use an external pull-up for compatibility with other Pentium processors.

Table 1. Mobile Pentium® Processor with MMX™ Technology Bond Pad Center Data (Sheet 12 of 13)

PAD#	SIGNAL[2,3,5]	Pad Center[1]			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
341	VSS	73.3	245.4	1861	6232
342	VCC3	69.6	245.4	1767	6232
343	A14	65.9	245.4	1673	6232
344	VCC2	62.2	245.4	1579	6232
345	VSS	58.5	245.4	1485	6232
346	A15	54.8	245.4	1391	6232
347	VSS	51.1	245.4	1297	6232
348	VCC3	47.4	245.4	1203	6232
349	A16	43.7	245.4	1109	6232
350	A17	40.0	245.4	1015	6232
351	VSS	36.3	245.4	921	6232
352	VCC3	32.5	245.4	827	6232
353	A18	28.8	245.4	733	6232
354	VCC2	25.1	245.4	639	6232
355	VSS	21.4	245.4	545	6232
356	A19	17.7	245.4	451	6232
357	VSS	14.0	245.4	357	6232
358	VCC3	10.3	245.4	263	6232
359	A20	6.6	245.4	169	6232
360	VCC2	2.9	245.4	75	6232
361	VSS	-0.8	245.4	-19	6232
362	RESET	-4.5	245.4	-113	6232
363	N.C.	-72.6	245.4	-1844	6232
364	CLK	-80.0	245.4	-2032	6232
365	SCYC	-83.7	245.4	-2126	6232
366	VSS	-87.4	245.4	-2220	6232
367	VCC3	-91.1	245.4	-2314	6232
368	BE7#	-94.8	245.4	-2408	6232
369	BE6#	-98.5	245.4	-2502	6232
370	BE5#	-102.2	245.4	-2596	6232
371	BE4#	-105.9	245.4	-2690	6232

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol “#” is used to denote active low signals.
4. Boundary Scan (JTAG) is implemented through the following pads:
   208 (TDO), 207 (TCK), 209 (TDI), 210 (TMS), 215 (TRST#)
5. FRCMC# - Can use an external pull-up for compatibility with other Pentium processors.

Table 1. Mobile Pentium® Processor with MMX™ Technology Bond Pad Center Data (Sheet 13 of 13)

PAD#	SIGNAL(2,3,5)	Pad Center(1)			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
372	VSS	-109.6	245.4	-2784	6232
373	VCC3	-113.3	245.4	-2878	6232
374	BE3#	-117.0	245.4	-2972	6232
375	BE2#	-120.7	245.4	-3066	6232
376	BE1#	-124.4	245.4	-3160	6232
377	BE0#	-128.1	245.4	-3254	6232
378	A20M#	-131.8	245.4	-3348	6232
379	FLUSH#	-135.5	245.4	-3442	6232
380	BUSCHK#	-139.2	245.4	-3536	6232
381	W/R#	-142.9	245.4	-3630	6232
382	VSS	-146.6	245.4	-3724	6232
383	VCC3	-150.3	245.4	-3818	6232
384	HIT#	-154.0	245.4	-3912	6232
385	HITM#	-157.7	245.4	-4006	6232
386	VSS	-161.4	245.4	-4100	6232
387	VCC3	-165.1	245.4	-4194	6232
388	ADS#	-168.8	245.4	-4288	6232
389	EADS#	-172.5	245.4	-4382	6232
390	D/C#	-176.2	245.4	-4476	6232
391	PWT	-179.9	245.4	-4570	6232
392	PCD	-183.6	245.4	-4664	6232

NOTES:

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3. The symbol “#” is used to denote active low signals.
4. Boundary Scan (JTAG) is implemented through the following pads:
   208 (TDO), 207 (TCK), 209 (TDI), 210 (TMS), 215 (TRST#)
5. FRCMC# - Can use an external pull-up for compatibility with other Pentium processors.

2.0 INTEL DIE PRODUCTS PROCESSING

2.1 Wafer Probe

Wafer probing is performed on every wafer produced in Intel Fabs. The process consists of specific electrical tests and device-specific functionality tests.

At the wafer level, built-in test structures are probed to verify that device electrical characteristics are in control and meet specifications. Measurements are made of transistor threshold voltages and current characteristics; poly and contact resistance; gate oxide and junction integrity; and specific parameters critical to the particular technology and device type. Wafer-to-wafer, across-the-wafer run-to-run variation and conformance to spec limits are checked.

The actual devices on each wafer are then probed for both functionality and performance to specifications. Additional reliability tests are also included in the probe steps.

2.2 Wafer Saw

Probed wafers are transferred to Intel's assembly sites to be sawed. The saw cuts completely through the wafer.

2.3 Test Procedure

Intel has instituted full-speed functional testing and burn-in at the die level for SmartDie products. This level of testing is ordinarily performed only after assembly into a package. Each die is tested and burned-in to the same electrical limits as the equivalent packaged unit.

2.4 Die Inspection

Upon completion of test and burn-in, the die undergo visual inspection. This process is the same visual inspection as standard packaged product. The compliant die are then transferred to GEL-PAKs for shipment.

2.5 Packing Procedure

Intel will ship all Intel die products in GEL-PAKs. GEL-PAKs eliminate the die edge damage usually associated with die cavity plates or chip trays.

The backside of each die adheres to the gel membrane in the GEL-PAK, eliminating the risk of damage to the active die surface. A simple vacuum release mechanism allows for pick and place removal at the customer's site.

Only die from the same wafer lot are packaged together in a GEL-PAK, and all die are placed in the GEL-PAKs with a consistent orientation. The GEL-PAKs are then sealed and labeled with the following information:

- Intel SmartDie
- Intel Part Number
- Assembly Process Order / Spec
- ROM Code (if applicable)
- Customer Part Number (if applicable)
- Assembly Lot Traveler Number
- Finished Product Order Number
- Quantity
- Seal Date
- Country of Origin

NOTE:

GEL-PAKs require a Vacuum Release Station. Contact Vichem* Corporation for more information.

2.6 Inspection Steps

Multiple inspection steps are performed during the die fabrication and packing flow. These steps are performed according to the same specifications and criteria established for Intel's standard packaged product. Specific inspection steps include a wafer saw visual as well as a final die visual just before die are sealed in moisture barrier bags.

2.7 Storage Requirements

Intel die products will be shipped in GEL-PAKs and sealed in a moisture-barrier anti-static bag with a desiccant. No special storage procedures are required while the bag is still unopened. Once opened, the GEL-PAK should be stored in a dry, inert atmosphere to prevent corrosion of the bond pads.

2.8 Electro-Static Discharge (ESD)

Components are ESD sensitive.

3.0 SPECIFICATIONS

Specifications within this document are specific to a particular die revision and are subject to change without notice. Verify with your local Intel Sales Office that you have the latest data before finalizing a design.

3.1 Physical Specifications

Table 2 defines Mobile Pentium® Processor with MMX™ Technology physical specifications.

Table 2. Mobile Pentium® Processor with MMX™ Technology Physical Specifications

Die Revision:	A-Step
Post-Saw Die Dimensions:	Mils: X = 442 ± 0.5, Y= 505 ± 0.5 See associated Die/Bond Pad Layout for X, Y orientation.
Die Thickness:	17 ± 1 mils
Minimum Pad Pitch:	94 microns (3.7 mils)
Pad Passivation Opening Size:	Mils: 3.0 x 5.6 (single pads) Microns: 75 x 141 (single pads)
Bond Pad Metallization: (outermost layer first)	16,800 Angstroms Aluminum (0.5% Copper), 1000 Angstroms Titanium
Pads per Die:	392
Die Backside Material: (outermost layer first)	1600 Angstroms Gold, 345 Angstroms Titanium
Passivation: (outermost layer first)	3.3 microns polyimide, 0.75 microns nitride
Intel Fabrication Process:	CMOS (min. feature size 0.4 microns)

NOTE: The die specifications provided are valid for A-step die only.

3.2 DC Specifications

ABSOLUTE MAXIMUM RATINGS†

GEL-PAK Storage Temperature .... 0°C to +70°C
Junction Temperature Under Bias .... -65°C to +110°C
3 V Supply Voltage wrt. V_{SS} .... -0.5 V to +4.6 V
2.9 V Supply Voltage wrt. V_{SS} .... -0.5 V to +3.7 V
3 V Only Buffer DC Input Voltage ...... -0.5 V to V_{CC3} + 0.5 V; to exceed V_{CC3} max

OPERATING CONDITIONS†

V_{CC3} (I/O Supply Voltage) .... 3.3 V ± 5%
V_{CC2} (Core Supply Voltage) ....2.45 V + 0.215/-0.165
T_J (Junction Temperature Under Bias) .... 0°C to 105°C(1)
Substrate Bias..............................Float (Self Biasing to V_{SS}), Alternative is to Drive V_{SS}
Core Operating Frequency .... 150, 166 MHz (60, 66 MHz Bus)

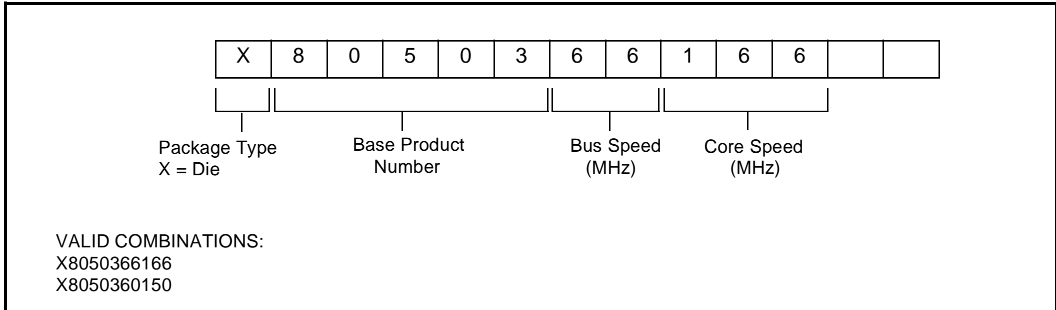
NOTES:

1. Average die surface temperature

NOTICE: This datasheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice. Verify with your local Intel Sales Office that you have the latest data before finalizing a design.

†***WARNING:*** *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

4.0 DEVICE NOMENCLATURE



5.0 REFERENCE INFORMATION

Document Title	Order #
Mobile Pentium® Processor with MMX™ Technology datasheet	243292

6.0 REVISION HISTORY

Revision	Date	Description
001	1/97	Initial Release