Pentium® Processor Specification Update

Release Date: March 1998

Order Number: 242480-035

The Pentium® processor may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

CONTENTS

REVISION HISTORY

Date of Revision	Version	Description
February 1995	–001	This document consolidates information previously contained in various versions of stepping information, notably the B-, C- and D- stepping of Pentium® processor at iCOMP® index (510\60, 567\66) and the B- and C-stepping of Pentium processor at iCOMP index (610\75, 735\90, 815\100).
March 1995	–002	Added Errata 22–25 and Spec Clarification 15 to Part I. Added Spec Change 12, Errata 24–27, 8DP–12DP, 11AP, Spec Clarification 3, and Doc Change 6 to Part II.
April 1995	–003	Part II: Added new markings for 120 MHz; added Spec Changes 13, 14, 15, 16, 17, 2TCP, 3TCP; revised Spec Changes 7, 11, 1TCP; added Errata 28 and 29; revised Errata 2TCP.
May 1995	–004	Part I: Added Errata 26 and 27; added Spec Clarifications 17 and 18; added Doc Change 3. Part II: Revised Spec Changes 12 and 17; added Spec Change 18; revised Errata 25 and 4DP and added Errata 30–33; added Spec Clarifications 9–13; added Doc Changes 7 and 8. Part III: New Section — Pentium® OverDrive® Processor
June 1995	–005	Part I: Added Spec Change 5; added Erratum 28; added Spec Clarification 19. Part II: Added Pentium Processor with Voltage Reduction Technology; added 133 MHz; added Spec Changes 19–23; revised Spec Changes 12–17; added S-Specs 1 and 2; added Errata 34, 35 and 13DP; revised Errata 4DP and 9AP; added Spec Clarifications 14–17; revised Spec Clarification 8. Part III: Added Spec Change 3; added Erratum 22; added Spec Clarifications 8–10.
July 1995	–006	Part I: Added Erratum 29. Part II: Added Spec Change 24; revised Spec Changes 7 and 17; added Erratum 36; added Spec Clarification 18. Part III: Added Spec Change 4; added Errata 23 and 24.
August 1995	–007	Part I: Added Errata 30–32; added Spec Clarifications 20 and 21. Part II: Revised Spec Change 21; added S-Spec 3; added Errata 37–41; revised Erratum 9; added Spec Clarifications 19–26. Part III: Added Errata 25–29; added Spec Clarifications 11 and 12.

Date of Revision	Version	Description
September 1995	–008	Removed Spec Changes, Spec Clarifications and Doc Changes which were incorporated into the 1995 *Pentium® Processor Family Developer's Manual* (Order Number 241563-004). Part I: Added Errata 33 and 34; added Doc Changes 1 and 2. Part II: Added Errata 42, 43 and 12AP; added Spec Clarification 13; added Doc Changes 1–6. Part III: Added Erratum 30; added Doc Changes 1 and 2.
October 1995	–009	Part I: Added Spec Changes 1 and 2; added Errata 35–37; added Spec Clarifications 4–7; added Doc Changes 3 and 4. Part II: Added Spec Changes 12 and 13; added Errata 44–48; revised Erratum 11; added Spec Clarifications 14–17; revised Spec Clarification 1; added Doc Changes 7–9; revised Doc Change 3. Part III: Added 83 MHz Pentium OverDrive processor; added Spec Changes 4–6; added Errata 31–33; revised Erratum 7; added Spec Clarifications 6 and 7; added Doc Changes 3 and 4.
November 1995	–010	Part I: Added Errata 38–40; added Spec Clarifications 8–10; added Doc Change 5. Part II: Added 120 MHz Pentium processor with Voltage Reduction Technology; added Spec Changes 14–15; added S-Spec 4; added Errata 49–53, 13AP and 14AP; revised Erratum 10; added Spec Clarifications 18–21; added Doc Change 10. Part III: Added Errata 34–36; revised Erratum 10; added Spec Clarifications 8–9; added Doc Change 5.
December 1995	–011	Part I: Added Errata 41–44; revised Errata 35 and 37; added Spec Clarifications 11 and 12; revised Spec Clarification 5 and 10; added Doc Change 6. Part II: Added Spec Change 16; added Errata 54–58; revised Errata 44 and 46; added Spec Clarifications 22 and 23; revised Spec Clarifications 5, 15 and 20; added Doc Change 11. Part III: Added Errata 37–40; revised Erratum 31; added Spec Clarifications 10–12; revised Spec Clarification 6; added Doc Change 6.
January 1996	–012	Part I: Added Errata 45 and 46; revised Errata 37 and 43; added Spec Clarification 13; added Doc Changes 7 and 8. Part II: Added Pentium Processor 150-MHz and 166-MHz, added Spec Changes 17–20; added Errata 59–64, 14DP, 15AP and 16AP; revised Errata 46, 56, 9AP and 11AP; added Spec Clarifications 24 and 25; revised Spec Clarification 9; added Doc Changes 12 and 13. Part III: Added Spec Change 7; added Errata 41–45; revised Erratum 39; added Spec Clarification 13; added Doc Changes 7 and 8.

Date of Revision	Version	Description
February 1996	–013	Part I: Added Erratum 47. Part II: Added S-Specs 5 and 6; added Errata 65 and 66. Part III: Added Erratum 46.
March 1996	–014	Part I: Revised Erratum 35; added Spec Clarification 14; added Doc Change 9. Part II: Added S-Spec 7; revised Erratum 44; added Spec Clarifications 26–29; added Doc Change 14. Part III: Added 120/133-, 125-, 150- and 166-MHz OverDrive processors; added Spec Change 6; revised Erratum 31; added Errata 47–55; added Spec Clarifications 14–16; added Doc Changes 9 and 10.
April 1996	–016*	Part I: Added Erratum 48; revised Erratum 35; added Spec Clarifications 15–17; revised Spec Clarification 5; added Doc Change 10. Part II: Added Spec change 21; added S-Spec 8; revised S-Spec 4; added Errata 67 and 68; revised Errata 28 and 44; added Spec Clarifications 30–35; revised Spec Clarification 15; added Doc Changes 15 and 16. Part III: Added Errata 56 and 57; revised Errata 19 and 31; added Spec Clarifications 17–19; revised Spec Clarification 6; added Doc Changes 11 and 12.
May 1996	–017	Part I: Added Spec Clarification 18. Part II: Revised Spec Changes 19 and 21; added Errata 15DP, 16DP and 18AP; revised Erratum 17AP; added Spec Clarification 36. Part III: Revised Spec Change 7; added Erratum 58; revised Erratum 57; added Spec Clarification 20.
June 1996	–018	Part I: Added Spec Change 3; added Erratum 49; added Spec Clarification 19. Part II: Added Spec Change 22; revised Spec Change 20; added Erratum 69; added Spec Clarifications 37 and 38; revised Spec Clarifications 5 and 25. Part III: Added Spec Change 8; added Erratum 59; added Spec Clarifications 21 and 22.
July 1996	–019	Part I: Added Erratum 50; revised Erratum 49; revised Spec Clarification 10. Part II: Added Spec Change 23; added Erratum 70; revised Erratum 69; revised Spec Clarification 20. Part III: Added Erratum 60; revised Erratum 59; revised Spec Clarification 10.

Note:

* Revision -015 was issued as revision -016.

Date of Revision	Version	Description
August 1996	–020	Part I: Added Erratum 51; added Spec Clarification 20. Part II: Added Erratum 71; added Spec Clarification 39. Part III: Added Erratum 61; added Spec Clarification 23.
September 1996	–021	Part I: Added Spec Clarification 21; revised Spec Clarification 5. Part II: Added Spec Clarification 40; revised Spec Clarification 15. Part III: Added Spec Clarification 24; revised Spec Clarification 6.
October 1996	–022	Part I: Revised Spec Change 3. Part II: Added Spec Change 24; revised Spec Change 22. Part III: Added Spec Change 9; revised Spec Change 8.
November 1996	–023	Part I: Revised Spec Change 3. Part II: Added Spec Change 24; revised Spec Change 22. Part III: Added Spec Change 9; revised Spec Change 8.
January 1996	–024	Part I: Added Spec Clarifications 22 and 23. Part II: Changed Spec Changes 1, 2, 4-7 to S-Specs 9–14; added S-Specs 15–21; added Errata 72–78 and 19AP; revised Errata 14 and 69; added Spec Clarifications 41–49; added Doc Change 17. Part III: Revised Errata 11 and 59; added Spec Clarifications 25 and 26.
March 1997	–025	Removed Spec Changes, S-Specs, Errata, Spec Clarifications and Doc Changes which were incorporated in the 1997 edition of the *Pentium® Processor Family Developer's Manual* (Order Number 241428) and the *Intel Architecture Software Developer's Manual*, Volume 1 (Order Number 243190) and Volume 2 (Order Number 243191) Part I: This section has been replaced with Part II from January's edition. The old section I has been removed and has been converted into the *Pentium® Processor 60 and 66 MHz Specification Update* (Order Number 243326). Added Erratum 79, added Doc Change 6. Part II: This section has been replaced with Part III from January's edition. Added Erratum 62.
April 1997	–026	Part I: Added Spec Change 3; added Doc Changes 7 and 8. Part II: Added new Pentium OverDrive processor with MMX Technology Stepping oxA3; added Spec Changes 6 and 7; added Errata 63–68; added Spec Clarifications 14 and 15; added Doc Change 5.
May 1997	–027	Part I: Added Spec Clarification 20; added Doc Change 9. Part II: None.

Date of Revision	Version	Description
June 1997	–028	Part I: Added Spec Changes 4–14, Added S-Spec 22; added Doc Change 10. Part II: None.
August 1997	–029	Part I: Added Spec Changes 15 and 16; added Doc Changes 11 and 12. Part II: Added Doc Change 6.
September 1997	–030	Part I: Added Erratum 17DP; Added Spec Clarification 21. Part II: Added Spec Clarification 16.
October 1997	–031	Part I: Added Erratum 80 and revised Erratum 61. Added new mobile Pentium Processor with MMX technology stepping myA0. Part II: Added Erratum 69 and revised Erratum 43.
November 1997	–032	Part II: Added new 200 MHz Pentium OverDrive processor with MMX technology Stepping oxB1.
December 1997	–033	Part I: Added Spec Change 17. Part II: None.
January 1998	–034	Part I: Added Erratum 81 and Spec Change 18. Part II: Added Erratum 70.
March 1998	–035	Part I: Added Erratum 82 and Spec Clarification 22. Part II: Added Erratum 71 and Spec Clarification 17.

PREFACE

This document is an update to the specifications contained in the *Pentium® Processor Family Developer's Manual*, (Order Number 241428) and the *Intel Architecture Software Developer's Manual*, Volume 1 and 2 (Order Numbers 243190 and 243191). It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It contains Specification Changes, S-Specs, Errata, Specification Clarifications and Documentation Changes, and is divided into the following parts:

- Part I: Specification Update for 75/90/100/120/133/150/166/200/233 MHz Pentium® Processors and Pentium Processors with MMX™ Technology
- Part II: Specification Update for Pentium® OverDrive® Processors

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

S-Specs are exceptions to the published specifications and apply only to the units assembled under that s-spec.

Errata are design defects or errors. Errata may cause the Pentium® processor's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Identification Information

The Pentium processor can be identified by the following register contents:

Family (1)	**75/90/100/120/ 133/150/166/200/ 233 MHz Model 2 (2)**	**63- and 83-MHz Model 3 (2)**	**Pentium® Processors with MMX™ Technology Model 4 (2)**	**Pentium Processors with MMX Technology Model 8 (2)**
05h	02h (described in Part I)	03h (described in Part II)	04h (described in Part I)	08h (described in Part I)

NOTES:

1. The Family corresponds to bits [11:8] of the EDX register after RESET, bits [11:8] of the EAX register after the CPUID instruction is executed, and the generation field of the Device ID register accessible through Boundary Scan.
2. The Model corresponds to bits [7:4] of the EDX register after RESET, bits [7:4] of the EAX register after the CPUID instruction is executed, and the model field of the Device ID register accessible through Boundary Scan.

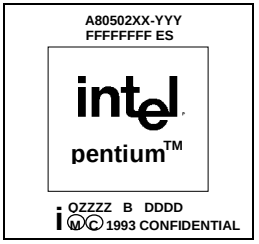
Part I:

Specification Update for 75/90/100/120/133/150/166/ 200/233 MHz Pentium® Processors and Pentium Processors with MMX™ Technology

GENERAL INFORMATION

Top Markings

B-Step Engineering Samples:



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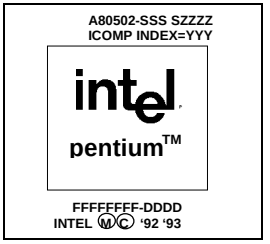

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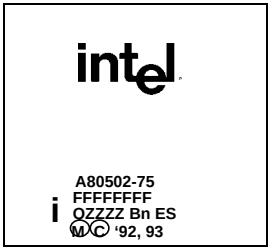

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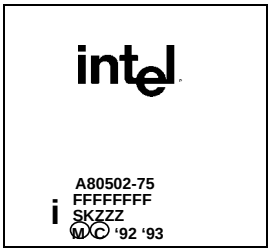

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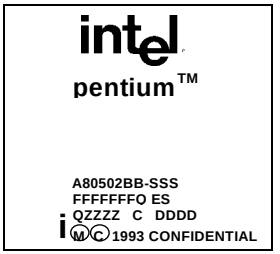

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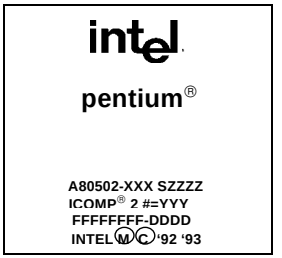

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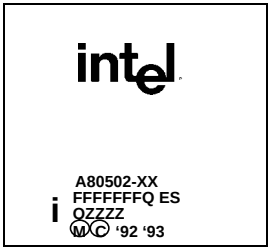

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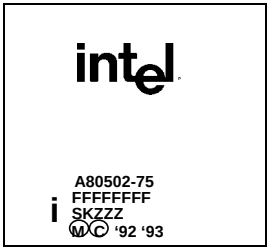

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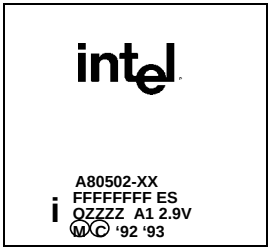

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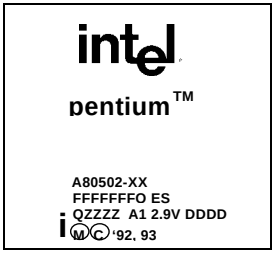

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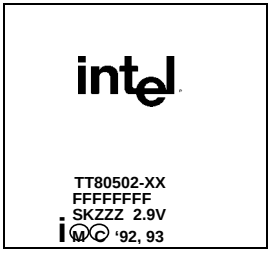

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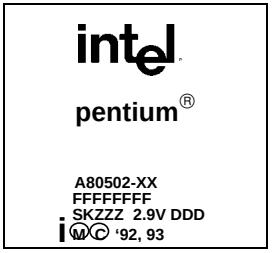

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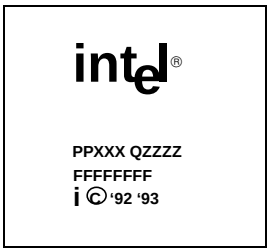

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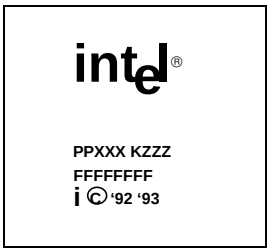

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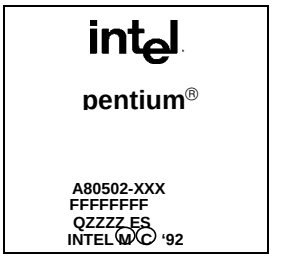

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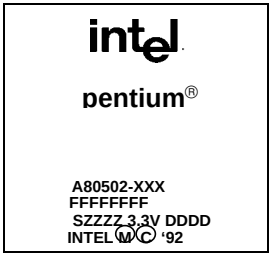

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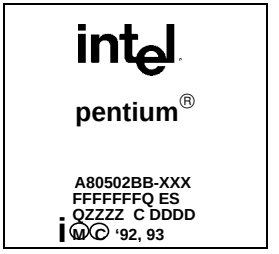
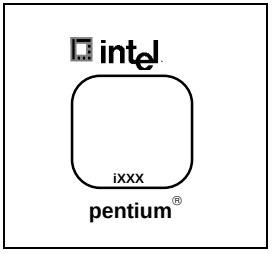


cC0-Step Engineering Sample PPGA Units:



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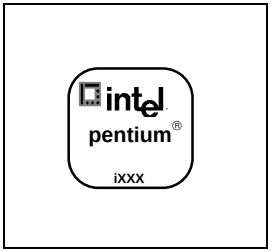
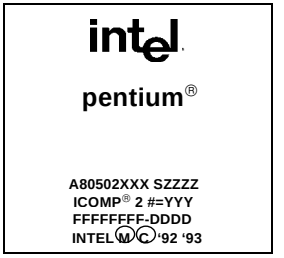


133 MHz cC0-Step Production Units:



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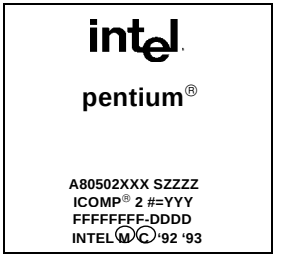

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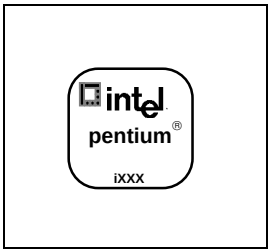

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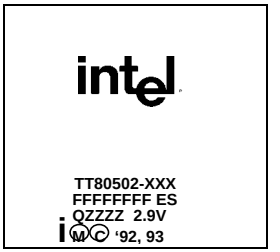

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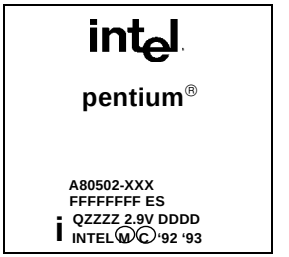

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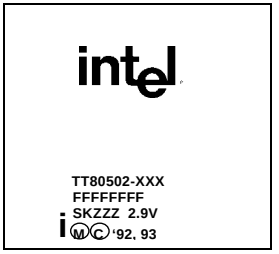

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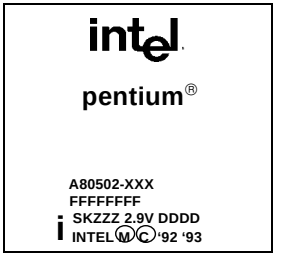

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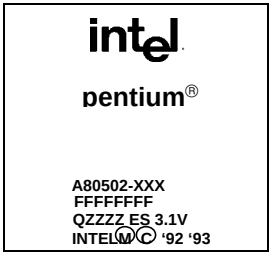

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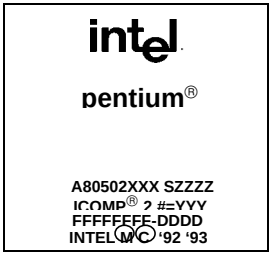

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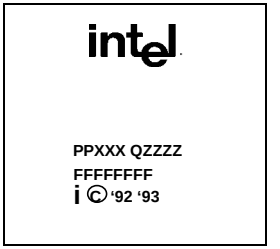

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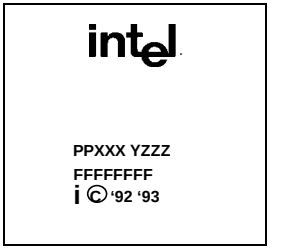
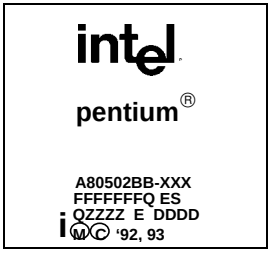


E0-Step Engineering Sample Units:



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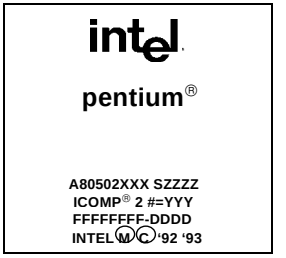
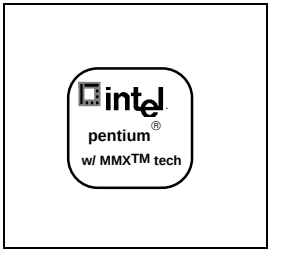
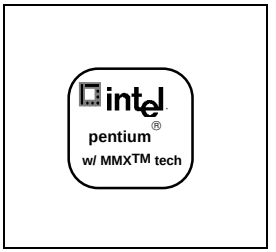


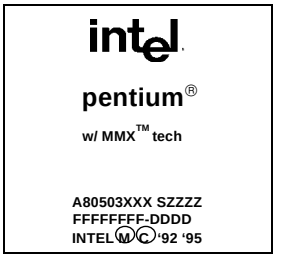
xA3-Step Pentium® Processor w/ MMX™ Technology Engineering Sample PPGA Units:



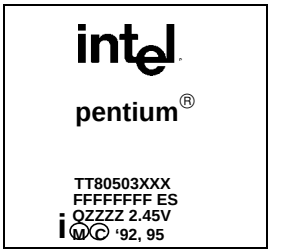
xA3-Step Pentium® Processor w/ MMX™ Technology Production PPGA Units:



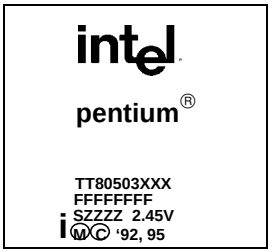
xA3-Step Pentium® Processor w/ MMX™ Technology Production SPGA Units:



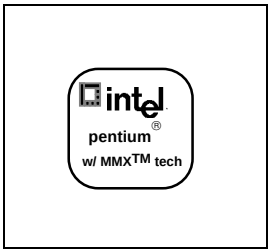
mxA3-Step Pentium® Processor w/ MMX™ Technology Engineering Sample TCP Units:



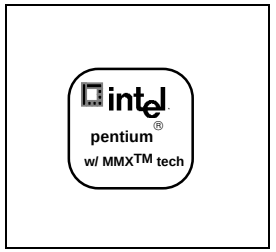
mxA3-Step Pentium® Processor w/ MMX™ Technology Production TCP Units:



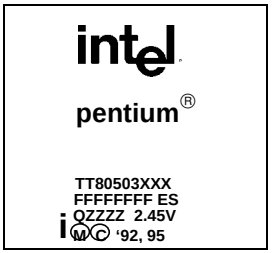
mxA3-Step Pentium® Processor w/ MMX™ Technology Engineering Sample PPGA Units:



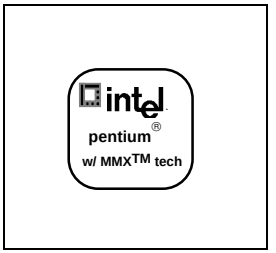
mxA3-Step Pentium® Processor w/ MMX™ Technology Production PPGA Units:



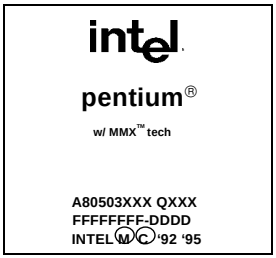
mxB1-Step Pentium® Processor w/ MMX™ Technology Engineering Sample TCP Units:



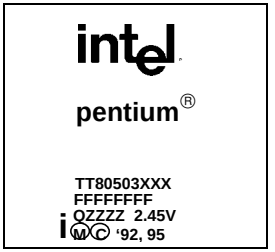
mxB1-Step Pentium® Processor w/ MMX™ Technology Engineering Sample PPGA Units:



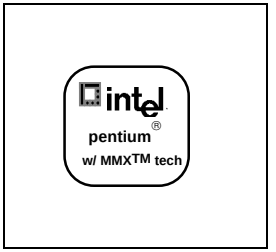
xB1-Step Pentium® Processor w/ MMX™ Technology Engineering Sample SPGA Units:



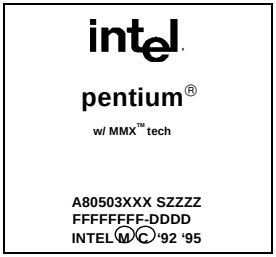
mxB1-Step Pentium® Processor w/ MMX™ Technology Production TCP Units:



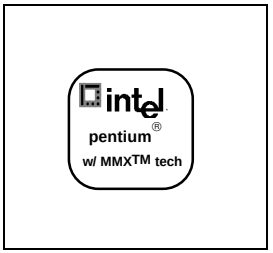
mxB1-Step Pentium® Processor w/ MMX™ Technology Production PPGA Units:



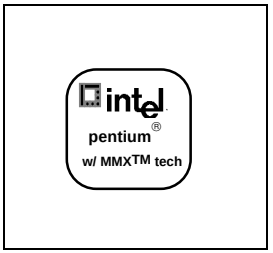
xB1-Step Pentium® Processor w/ MMX™ Technology Production SPGA Units:



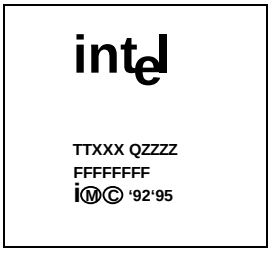
xB1-Step Pentium® Processor w/ MMX™ Technology Engineering Sample PPGA Units:



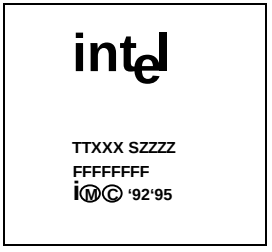
xB1-Step Pentium® Processor w/ MMX™ Technology Production PPGA Units:



myA0-Step Engineering Sample TCP Units:

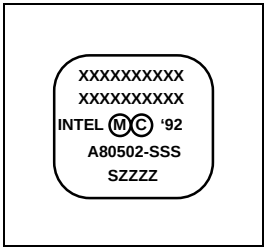


myA0-Step Production TCP Units:

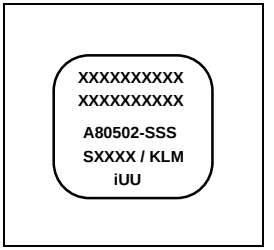


Bottom Markings

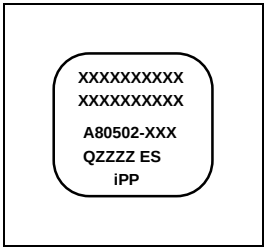
C-Step Production Units: (before 7/95)



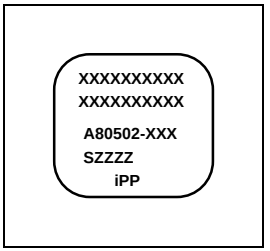
C and cB1-Step Production Units: (after 7/95)



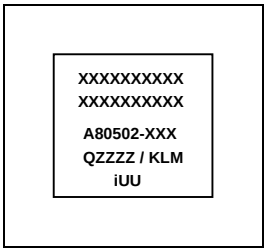
mcB1-Step Engineering Sample SPGA Units:



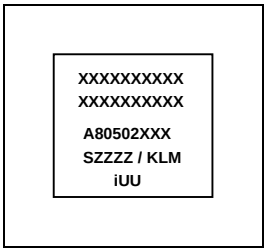
mcB1-Step Production SPGA Units:



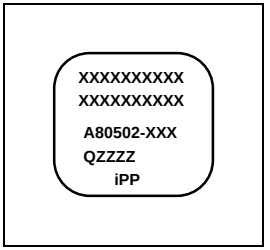
cC0-Step Engineering Sample Units:



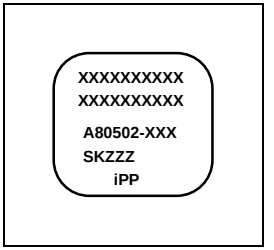
cC0-Step Production Units:



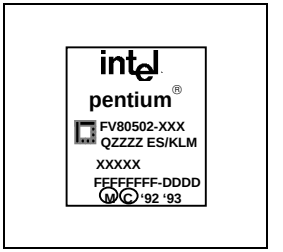
mA4-Step Engineering Sample SPGA Units:



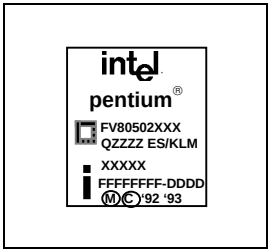
mA4-Step Production SPGA Units:



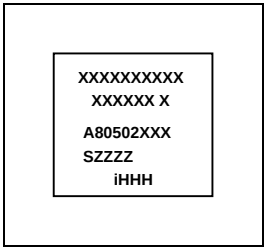
cC0-Step Engineering Sample PPGA Units:



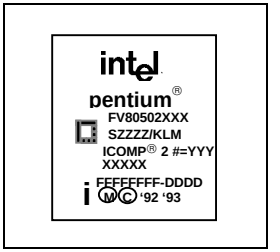
cC0-Step 200 MHz Engineering Sample PPGA Units:



mcC0-Step Production SPGA Units:



cC0-Step Production PPGA Units:



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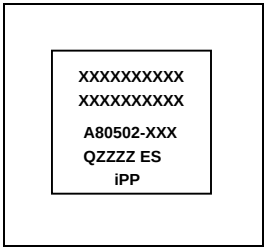
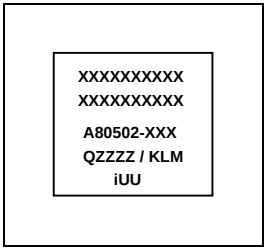
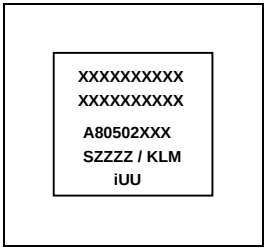


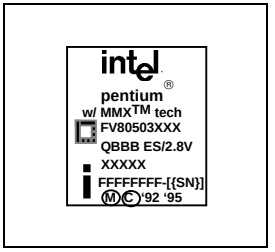
E0-Step Engineering Sample Units:



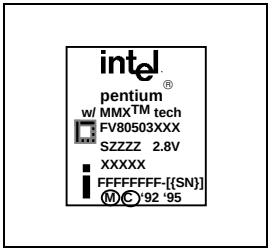
E0-Step Production Units:



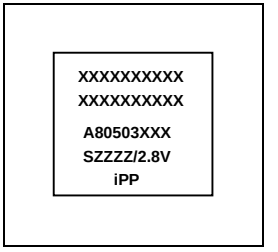
xA3-Step Pentium® Processor w/ MMX™ Technology Engineering Sample PPGA Units:



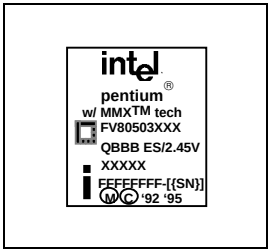
xA3-Step Pentium® Processor w/ MMX™ Technology Production PPGA Units:



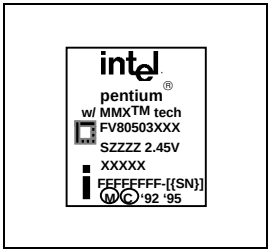
xA3-Step Pentium® Processor w/ MMX™ Technology Production SPGA Units:



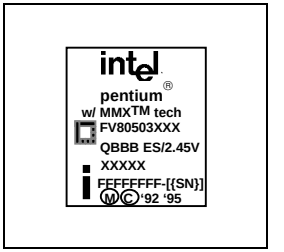
mxA3-Step Pentium® Processor w/ MMX™ Technology Engineering Sample PPGA Units:



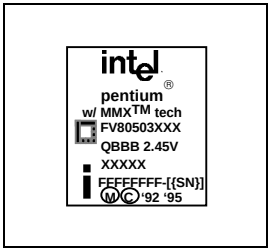
mxA3-Step Pentium® Processor w/ MMX™ Technology Production PPGA Units:



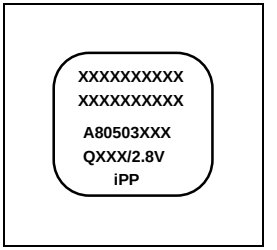
mxB1-Step Pentium® Processor w/ MMX™ Technology Engineering Sample PPGA Units:



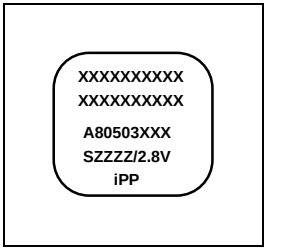
mxB1-Step Pentium® Processor w/ MMX™ Technology Production PPGA Units:



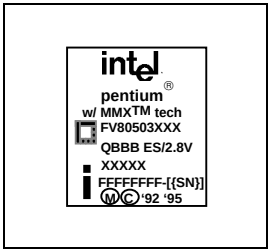
xB1-Step Pentium® Processor w/ MMX™ Technology Engineering Sample SPGA Units:



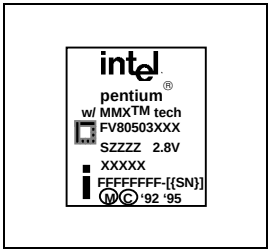
xB1-Step Pentium® Processor w/ MMX™ Technology Production SPGA Units:



xB1-Step Pentium® Processor w/ MMX™ Technology Engineering Sample PPGA Units:



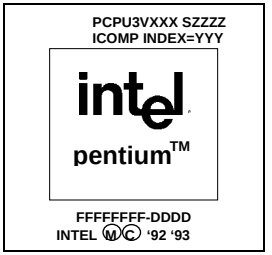
xB1-Step Pentium® Processor w/ MMX™ Technology Production PPGA Units:



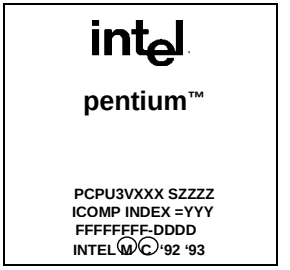
Boxed Pentium® Processors with Unattached Heatsinks

Top Markings

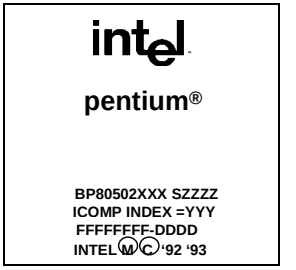
B-Step Boxed Production Units:



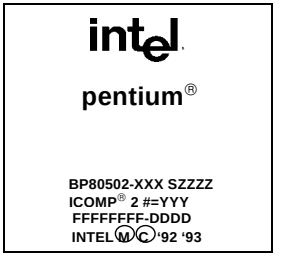
C2-Step Boxed Production Units:



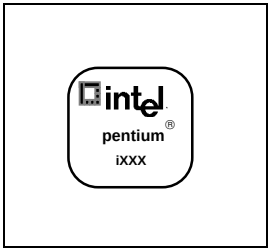
C2-Step Boxed Production Units:



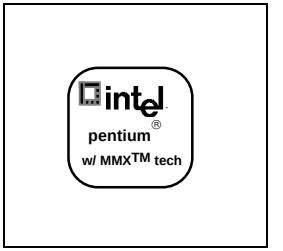
cC0, cB1 and E0-Step Boxed Production Units:



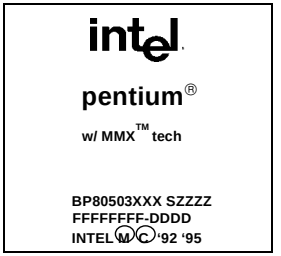
cC0-Step Boxed Production PPGA Units:



xA3 and xB1-Step Boxed Pentium® Processor w/MMX™ Technology Production PPGA Units:



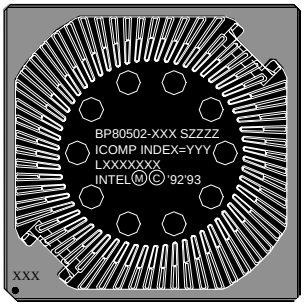
xA3 and xB1-Step Boxed Pentium® Processor w/ MMX™ Technology Production SPGA Units:



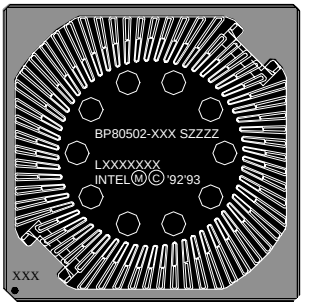
Boxed Pentium® Processors with Attached Heatsinks

Top Markings

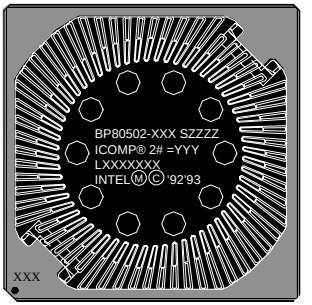
C2, cB1, cC0 and E0-Step Boxed Pentium® Processor Fan Heatsink Base Marking:



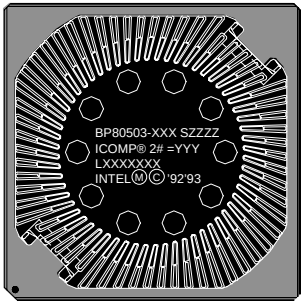
C2, cB1, cC0 and E0-Step Early Boxed Pentium® Processor Fan Heatsink Base Marking:



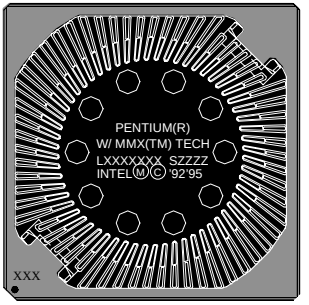
cC0 and E0-Step Boxed Pentium® Processor Fan Heatsink Base Marking:



xA3 and xB1-Step PPGA Boxed Pentium® Processor with MMX™ Technology Fan Heatsink Base Marking:



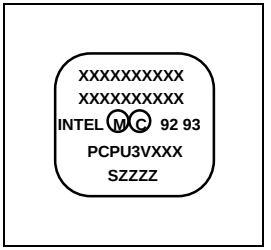
xA3 and xB1-Step SPGA Boxed Pentium® Processor with MMX™ Technology Fan Heatsink Base Marking:



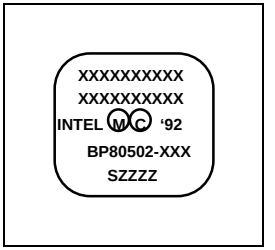
Boxed Pentium® Processors

Bottom Markings

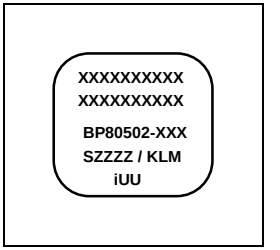
C2-Step Boxed Production Units:



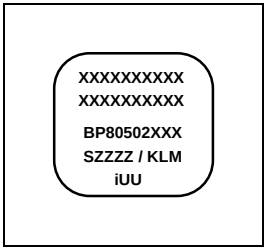
C2-Step Boxed Production Units: (before 7/95)



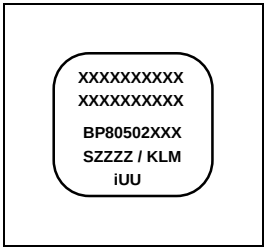
C2 and cB1-Step Boxed Production Units: (after 7/95)



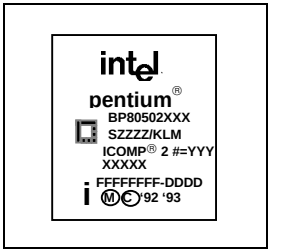
C2 and cB1-Step Boxed Production Units: (after 7/95)



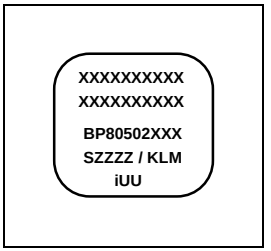
cC0 and E0-Step Boxed Production Units:



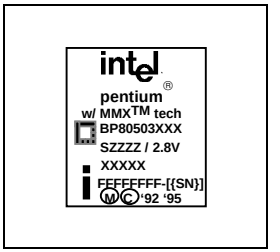
cC0-Step Boxed Production PPGA Units:



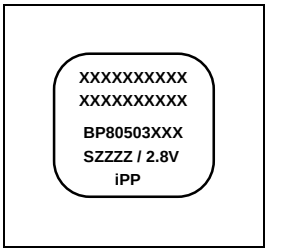
E0-Step Boxed Production Units:



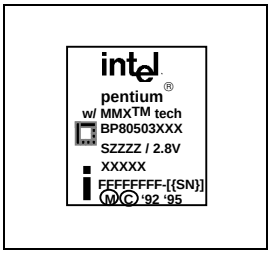
xA3-Step Boxed Pentium® Processor w/ MMX™ Technology Production PPGA Units:



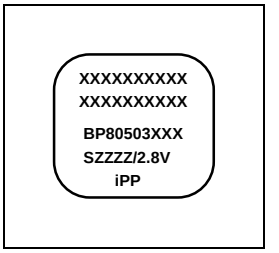
xA3-Step Boxed Pentium® Processor w/ MMX™ Technology Production SPGA Units:



xA3-Step and xB1-Step Boxed Pentium® Processor w/ MMX™ Technology Production PPGA Units:



xA3-Step and xB1-Step Boxed Pentium® Processor w/ MMX™ Technology Production SPGA Units:



NOTES:

- XX or XXX = Core Speed (MHz).
- BB = Bus speed (MHz).
- SZZZZ/SKZZZ = Product S-Spec number.
- FFFFFFFF = FPO # (Test Lot Traceability #).
- For packages with heat spreaders, the inner line box defines the spreader edge.
- Ink Mark = All logo information on the heat spreader.
- Laser Mark = The two lines of information above and below the heat spreader. All bottomside information is laser mark.
- ES = Engineering Sample.
- QZZZZ = Sample Specification number.
- DDDD = Serialization code.
- YYY = iCOMP® index 2.0 OR iCOMP index. Intel is making an enhancement to the current plastic PGA (PPGA) and ceramic PGA (CPGA) desktop and mobile Pentium® processors with the addition of the iCOMP Index 2.0 rating as part of the processor package mark. For PPGA Pentium processors, the iCOMP index 2.0 will be marked on the bottom side (pin side) of the package and for CPGA it will be marked on the top side of the package. The part marking will be: iCOMP 2 # = XXX (67 for 75-MHz, 81 for 90-MHz, 90 for 100-MHz, 100 for 120-MHz, 111 for 133-MHz, 114 for 150-MHz, 127 for 166-MHz, and 142 for 200-MHz). Older parts may be marked with the iCOMP index (610 for 75-MHz and 735 for 90-MHz, 815 for 100-MHz, 1000 for 120-MHz, 1110 for 133-MHz, 1176 for 150-MHz, and 1308 for 166-MHz parts).
- TT = TCP Package, A = SPGA Package, FV = PPGA Package, BP = Boxed Processor in any package.
- The bottom markings on the C and cB1-step production units will replace the existing bottom marking on C-step parts effective 7/95.
- UU = 75 or 133 for 75- or 133-MHz Pentium processors, PP for all other speeds and MPP for mobile Pentium processors.
- K = V for VRE voltage range and S for standard voltage range.
- L = M for min valid MD timings and S for min valid standard timings.
- M = U is not tested for DP, but is tested for UP and MP. S is tested for DP, UP and MP.

Basic 75/90/100/120/133/150/166/200/233 MHz Pentium® Processor and Pentium Processor with MMX™ Technology Identification Information

CPUID				Manufacturing Stepping	Speed (MHz) Core / Bus	S-Spec	Comments
Type	Family	Model	Stepping				
0	5	2	1	B1	75/50	Q0540	ES
2	5	2	1	B1	75/50	Q0541	ES
0	5	2	1	B1	90/60	Q0542	STD
0	5	2	1	B1	90/60	Q0613	VR
2	5	2	1	B1	90/60	Q0543	DP
0	5	2	1	B1	100/66	Q0563	STD
0	5	2	1	B1	100/66	Q0587	VR
0	5	2	1	B1	100/66	Q0614	VR
0	5	2	1	B1	75/50	Q0601	TCP Mobile
0	5	2	1	B1	90/60	SX879	STD
0	5	2	1	B1	90/60	SX885	MD
0	5	2	1	B1	90/60	SX909	VR
2	5	2	1	B1	90/60	SX874	DP, STD
0	5	2	1	B1	100/66	SX886	MD
0	5	2	1	B1	100/66	SX910	VR, MD
0	5	2	2	B3	90/60	Q0628	STD
0 or 2	5	2	2	B3	90/60	Q0611	STD
0 or 2	5	2	2	B3	90/60	Q0612	VR
0	5	2	2	B3	100/66	Q0677	VRE/MD
0	5	2	2	B3	75/50	Q0606	TCP Mobile
0	5	2	2	B3	75/50	SX951	TCP Mobile
0	5	2	2	B3	90/60	SX923	STD
0	5	2	2	B3	90/60	SX922	VR
0	5	2	2	B3	90/60	SX921	MD
2	5	2	2	B3	90/60	SX942	DP, STD
2	5	2	2	B3	90/60	SX943	DP, VR
2	5	2	2	B3	90/60	SX944	DP, MD
0	5	2	2	B3	90/60	SZ951[5]	STD
0	5	2	2	B3	100/66	SX960	VRE/MD

Basic 75/90/100/120/133/150/166/200/233 MHz Pentium® Processor and Pentium Processor with MMX™ Technology Identification Information (Cont'd)

CPUID				Manufacturing Stepping	Speed (MHz) Core / Bus	S-Spec	Comments
Type	Family	Model	Stepping				
0 or 2	5	2	4	B5	75/50	Q0704	TCP Mobile
0 or 2	5	2	4	B5	75/50	Q0666	STD
0 or 2	5	2	4	B5	90/60	Q0653	STD
0 or 2	5	2	4	B5	90/60	Q0654	VR
0 or 2	5	2	4	B5	90/60	Q0655	MD
0 or 2	5	2	4	B5	100/66	Q0656	MD
0 or 2	5	2	4	B5	100/66	Q0657	VR, MD
0 or 2	5	2	4	B5	100/66	Q0658	VRE/MD
0	5	2	4	B5	120/60	Q0707	VRE/MD[1]
0	5	2	4	B5	120/60	Q0708	STD[1]
0	5	2	4	B5	75/50	SX975	TCP Mobile
0 or 2	5	2	4	B5	75/50	SX961	STD
0 or 2	5	2	4	B5	75/50	SZ977[5]	STD
0 or 2	5	2	4	B5	90/60	SX957	STD
0 or 2	5	2	4	B5	90/60	SX958	VR
0 or 2	5	2	4	B5	90/60	SX959	MD
0 or 2	5	2	4	B5	90/60	SZ978[5]	STD
0 or 2	5	2	4	B5	100/66	SX962	VRE/MD
0	5	2	5	C2	75/50	Q0725	TCP Mobile
0 or 2	5	2	5	C2	75/50	Q0700	STD
0 or 2	5	2	5	C2	75/50	Q0749	MD
0 or 2	5	2	5	C2	90/60	Q0699	STD
0 or 2	5	2	5	C2	100/50 or 66	Q0698	VRE/MD
0 or 2	5	2	5	C2	100/50 or 66	Q0697	STD
0	5	2	5	C2	120/60	Q0711	VRE/MD
0	5	2	5	C2	120/60	Q0732	VRE/MD
0	5	2	5	C2	133/66	Q0733	MD
0	5	2	5	C2	133/66	Q0751	MD
0	5	2	5	C2	133/66	Q0775	VRE/MD

Basic 75/90/100/120/133/150/166/200/233 MHz Pentium® Processor and Pentium Processor with MMX™ Technology Identification Information (Cont'd)

CPUID				Manufacturing Stepping	Speed (MHz) Core / Bus	S-Spec	Comments
Type	Family	Model	Stepping				
0	5	2	5	C2	75/50	SK079	TCP Mobile
0 or 2	5	2	5	C2	75/50	SX969	STD
0 or 2	5	2	5	C2	75/50	SX998	MD
0 or 2	5	2	5	C2	75/50	SZ994[5]	STD
0 or 2	5	2	5	C2	75/50	SU070[6]	STD
0 or 2	5	2	5	C2	90/60	SX968	STD
0 or 2	5	2	5	C2	90/60	SZ995[5]	STD
0 or 2	5	2	5	C2	90/60	SU031[6]	STD
0 or 2	5	2	5	C2	100/50 or 66	SX970	VRE/MD
0 or 2	5	2	5	C2	100/50 or 66	SX963	STD
0 or 2	5	2	5	C2	100/50 or 66	SZ996[5]	STD
0 or 2	5	2	5	C2	100/50 or 66	SU032[6]	STD
0	5	2	5	C2	120/60	SK086	VRE/MD
0	5	2	5	C2	120/60	SX994	VRE/MD
0	5	2	5	C2	120/60	SU033[6]	VRE/MD
0	5	2	5	C2	133/66	SK098	MD
0	5	2	5	mA1[4]	75/50	Q0686	VRT[2], TCP
0	5	2	5	mA1[4]	75/50	Q0689	VRT[2], SPGA
0	5	2	5	mA1[4]	90/60	Q0694	VRT[2], TCP
0	5	2	5	mA1[4]	90/60	Q0695	VRT[2], SPGA
0	5	2	5	mA1[4]	75/50	SK089	VRT[2], TCP
0	5	2	5	mA1[4]	75/50	SK091	VRT[2], SPGA
0	5	2	5	mA1[4]	90/60	SK090	VRT[2], TCP
0	5	2	5	mA1[4]	90/60	SK092	VRT[2], SPGA
0 or 2	5	2	B	cB1[4]	120/60	Q0776	STD/no Kit[3]
0 or 2	5	2	B	cB1[4]	133/66	Q0772	STD/no Kit[3]
0 or 2	5	2	B	cB1[4]	133/66	Q0773	STD
0 or 2	5	2	B	cB1[4]	133/66	Q0774	VRE/MD, no Kit[3]
0 or 2	5	2	B	cB1[4]	120/60	SK110	STD/no Kit[3]
0 or 2	5	2	B	cB1[4]	133/66	SK106	STD/no Kit[3]

Basic 75/90/100/120/133/150/166/200/233 MHz Pentium® Processor and Pentium Processor with MMX™ Technology Identification Information (Cont'd)

CPUID				Manufacturing Stepping	Speed (MHz) Core / Bus	S-Spec	Comments
Type	Family	Model	Stepping				
0 or 2	5	2	B	cB1[4]	133/66	S106J[7]	STD/no Kit[3]
0 or 2	5	2	B	cB1[4]	133/66	SK107	STD
0 or 2	5	2	B	cB1[4]	133/66	SU038[6]	STD/no Kit[3]
0	5	2	B	mcB1[4]	100/66	Q0884	VRT[2], TCP
0	5	2	B	mcB1[4]	120/60	Q0779	VRT[2], TCP
0	5	2	B	mcB1[4]	120/60	Q0808	3.3V, SPGA
0	5	2	B	mcB1[4]	100/66	SY029	VRT[2], TCP
0	5	2	B	mcB1[4]	120/60	SK113	VRT[2], TCP
0	5	2	B	mcB1[4]	120/60	SK118[7]	VRT[2], TCP
0	5	2	B	mcB1[4]	120/60	SX999	3.3V, SPGA
0 or 2	5	2	C	cC0	133/66	Q0843	STD/No Kit[3]
0 or 2	5	2	C	cC0	133/66	Q0844	STD
0 or 2	5	2	C	cC0	150/60	Q0835	STD
0 or 2	5	2	C	cC0	150/60	Q0878	STD, PPGA[9]
0 or 2	5	2	C	cC0	150/60	SU122[6]	STD
0 or 2	5	2	C	cC0	166/66	Q0836	VRE/No Kit[3]
0 or 2	5	2	C	cC0	166/66	Q0841	VRE
0 or 2	5	2	C	cC0	166/66	Q0886	VRE, PPGA[9]
0 or 2	5	2	C	cC0	166/66	Q0890	VRE, PPGA[9]
0	5	2	C	cC0	166/66	Q0949[8]	VRE, PPGA[9]
0 or 2	5	2	C	cC0	200/66	Q0951F[10]	VRE, PPGA[9]
0	5	2	C	cC0	200/66	Q0951[8]	VRE, PPGA[9]
0	5	2	C	cC0	200/66	SL25H[6, 8, 14]	VRE, PPGA[9]
0 or 2	5	2	C	cC0	120/60	SL22M[6]	STD
0 or 2	5	2	C	cC0	120/60	SL25J[5]	STD
0 or 2	5	2	C	cC0	120/60	SY062	STD
0 or 2	5	2	C	cC0	133/66	SL22Q[6]	STD
0 or 2	5	2	C	cC0	133/66	SL25L[5]	STD
0 or 2	5	2	C	cC0	133/66	SY022	STD
0 or 2	5	2	C	cC0	133/66	SY023	STD/ No Kit[3]
0 or 2	5	2	C	cC0	133/66	SU073[6]	STD/ No Kit[3]

Basic 75/90/100/120/133/150/166/200/233 MHz Pentium® Processor and Pentium Processor with MMX™ Technology Identification Information (Cont'd)

CPUID				Manufacturing Stepping	Speed (MHz) Core / Bus	S-Spec	Comments
Type	Family	Model	Stepping				
0 or 2	5	2	C	cC0	150/60	SY015	STD
0 or 2	5	2	C	cC0	150/60	SU071[6]	STD
0 or 2	5	2	C	cC0	166/66	SL24R	VRE, No Kit[3,13]
0 or 2	5	2	C	cC0	166/66	SY016	VRE, No Kit[3]
0 or 2	5	2	C	cC0	166/66	SY017	VRE
0 or 2	5	2	C	cC0	166/66	SU072[6]	VRE, No Kit[3]
0	5	2	C	cC0	166/66	SY037[8]	VRE, PPGA[9]
0 or 2	5	2	C	cC0	200/66	SY044	VRE, PPGA[9]
0	5	2	C	cC0	200/66	SY045[8,15]	VRE, PPGA[9]
0	5	2	C	cC0	200/66	SU114[5,8,14]	VRE, PPGA[9]
0	5	2	C	cC0	200/66	SL24Q[8]	VRE, PPGA[9], No Kit[3, 13]
0	5	7	0	mA4[4]	75/50	Q0848	VRT[2], TCP
0	5	7	0	mA4[4]	75/50	Q0851	VRT[2], SPGA
0	5	7	0	mA4[4]	90/60	Q0849	VRT[2], TCP
0	5	7	0	mA4[4]	90/60	Q0852	VRT[2], SPGA
0	5	7	0	mA4[4]	100/66	Q0850	VRT[2], TCP
0	5	7	0	mA4[4]	100/66	Q0853	VRT[2], SPGA
0	5	7	0	mA4[4]	75/50	SK119	VRT[2], TCP
0	5	7	0	mA4[4]	75/50	SK122	VRT[2], SPGA
0	5	7	0	mA4[4]	90/60	SK120	VRT[2], TCP
0	5	7	0	mA4[4]	90/60	SK123	VRT[2], SPGA
0	5	7	0	mA4[4]	100/66	SK121	VRT[2], TCP
0	5	7	0	mA4[4]	100/66	SK124	VRT[2], SPGA
0	5	2	C	mcC0[4]	100/66	Q0887	TCP/VRT[2]
0	5	2	C	mcC0[4]	120/60	Q0879	TCP/VRT[2]
0	5	2	C	mcC0[4]	120/60	Q0880	SPGA 3.1V
0	5	2	C	mcC0[4]	133/66	Q0881	TCP/VRT[2]

Basic 75/90/100/120/133/150/166/200/233 MHz Pentium® Processor and Pentium Processor with MMX™ Technology Identification Information (Cont'd)

CPUID				Manufacturing Stepping	Speed (MHz) Core / Bus	S-Spec	Comments
Type	Family	Model	Stepping				
0	5	2	C	mcC0[4]	133/66	Q0882	SPGA 3.1V
0	5	2	C	mcC0[4]	150/60	Q024	TCP/VRT[2]
0	5	2	C	mcC0[4]	150/60	Q0906	TCP 3.1V
0	5	2	C	mcC0[4]	150/60	Q040	SPGA/VRT[2]
0	5	2	C	mcC0[4]	75/50	SY056	TCP/VRT[2]
0	5	2	C	mcC0[4]	100/66	SY020	TCP/VRT[2]
0	5	2	C	mcC0[4]	100/66	SY046	SPGA 3.1V
0	5	2	C	mcC0[4]	120/60	SY021	TCP/VRT[2]
0	5	2	C	mcC0[4]	120/60	SY027	SPGA 3.1V
0	5	2	C	mcC0[4]	120/60	SY030	SPGA 3.3V
0	5	2	C	mcC0[4]	133/66	SY019	TCP/VRT[2]
0	5	2	C	mcC0[4]	133/66	SY028	SPGA 3.1V
0	5	2	C	mcC0[4]	150/60	SY061	TCP/VRT[2]
0	5	2	C	mcC0[4]	150/60	SY043	TCP 3.1V
0	5	2	C	mcC0[4]	150/60	SY058	SPGA/VRT[2]
0	5	2	6	E0	75/50	Q0846	TCP Mobile
0 or 2	5	2	6	E0	75/50	Q0837	STD
0 or 2	5	2	6	E0	90/60	Q0783	STD
0 or 2	5	2	6	E0	100/50 or 66	Q0784	STD
0 or 2	5	2	6	E0	120/60	Q0785	VRE
0	5	2	6	E0	75/50	SY009	TCP Mobile
0 or 2	5	2	6	E0	75/50	SY005	STD
0 or 2	5	2	6	E0	75/50	SU097[5]	STD
0 or 2	5	2	6	E0	75/50	SU098[6]	STD
0 or 2	5	2	6	E0	90/60	SY006	STD
0 or 2	5	2	6	E0	100/50 or 66	SY007	STD
0 or 2	5	2	6	E0	100/50 or 66	SU110[5]	STD
0 or 2	5	2	6	E0	100/50 or 66	SU099[6]	STD
0 or 2	5	2	6	E0	120/60	SY033	STD
0 or 2	5	2	6	E0	120/60	SU100[6]	STD

Basic 75/90/100/120/133/150/166/200/233 MHz Pentium® Processor and Pentium Processor with MMX™ Technology Identification Information (Cont'd)

CPUID				Manufacturing Stepping	Speed (MHz) Core / Bus	S-Spec	Comments
Type	Family	Model	Stepping				
0 or 2	5	4	4	xA3	150/60	Q020	ES, PPGA[12]
0 or 2	5	4	4	xA3	166/66	Q019	ES, PPGA[12]
0 or 2	5	4	4	xA3	200/66	Q018	ES, PPGA[12]
0 or 2	5	4	4	xA3	166/66	SL23T[6, 18]	SPGA[12]
0 or 2	5	4	4	xA3	166/66	SL23R[5]	PPGA[9,12]
0 or 2	5	4	4	xA3	166/66	SL25M[6]	PPGA[9,12]
0 or 2	5	4	4	xA3	166/66	SY059	PPGA[12]
0 or 2	5	4	4	xA3	166/66	SL2HU [5]	SPGA[12]
0 or 2	5	4	4	xA3	166/66	SL239	SPGA[12]
0 or 2	5	4	4	xA3	166/66	SL26V	SPGA[12,13]
0 or 2	5	4	4	xA3	166/66	SL26H	PPGA[12,13]
0 or 2	5	4	4	xA3	200/66	SL26J[15]	PPGA[12,13]
0 or 2	5	4	4	xA3	200/66	SY060	PPGA[12]
0 or 2	5	4	4	xA3	200/66	SL26Q[5]	PPGA[9,12,13]
0 or 2	5	4	4	xA3	200/66	SL274[6]	PPGA[9,12,13]
0 or 2	5	4	4	xA3	200/66	SL23S[5]	PPGA[9,12]
0 or 2	5	4	4	xA3	200/66	SL25N[6]	PPGA[9,12]
0	5	4	4	mxA3	150/60	Q016	ES, TCP[11]
0	5	4	4	mxA3	150/60	Q061	ES, PPGA[11]
0	5	4	4	mxA3	166/66	Q017	ES, TCP[11]
0	5	4	4	mxA3	166/66	Q062	ES, PPGA[11]
0	5	4	4	mxA3	150/60	SL22G	TCP[11]
0	5	4	4	mxA3	150/60	SL246	PPGA[11]
0	5	4	4	mxA3	166/66	SL22F	TCP[11]
0	5	4	4	mxA3	166/66	SL23Z	PPGA[11]
0 or 2	5	4	3	xB1	166/66	Q125	ES, PPGA[12]
0 or 2	5	4	3	xB1	166/66	Q126	ES, SPGA[12]
0 or 2	5	4	3	xB1	200/66	Q124	ES, PPGA[12]
0 or 2	5	4	3	xB1	233/66	Q140	ES, PPGA[12]
0 or 2	5	4	3	xB1	166/66	SL27H	PPGA[12]
0 or 2	5	4	3	xB1	166/66	SL27K	SPGA[12]

Basic 75/90/100/120/133/150/166/200/233 MHz Pentium® Processor and Pentium Processor with MMX™ Technology Identification Information (Cont'd)

CPUID				Manufacturing Stepping	Speed (MHz) Core / Bus	S-Spec	Comments
Type	Family	Model	Stepping				
0 or 2	5	4	3	xB1	166/66	SL2HX[5]	SPGA[12]
0 or 2	5	4	3	xB1	166/66	SL23X[6]	SPGA[12]
0 or 2	5	4	3	xB1	166/66	SL2FP[5]	PPGA[9, 12]
0 or 2	5	4	3	xB1	166/66	SL23V[6]	PPGA[9, 12]
0 or 2	5	4	3	xB1	200/66	SL27J	PPGA[12]
0 or 2	5	4	3	xB1	200/66	SL2FQ[5]	PPGA[9, 12]
0 or 2	5	4	3	xB1	200/66	SL23W[6]	PPGA[9, 12]
0 or 2	5	4	3	xB1	200/66	SL2RY	SPGA[12]
0 or 2	5	4	3	xB1	200/66	SL2S9[6]	SPGA[12]
0 or 2	5	4	3	xB1	233/66	SL27S	PPGA[12]
0 or 2	5	4	3	xB1	233/66	SL2BM[5]	PPGA[9, 12]
0 or 2	5	4	3	xB1	233/66	SL293[6]	PPGA[9, 12]
0	5	4	3	mxB1	120/60	Q230	ES, TCP [17]
0	5	4	3	mxB1	133/66	Q130	ES, TCP[11]
0	5	4	3	mxB1	133/66	Q129	ES, PPGA[11]
0	5	4	3	mxB1	150/60	Q116	ES, TCP[11]
0	5	4	3	mxB1	150/60	Q128	ES, PPGA[11]
0	5	4	3	mxB1	166/66	Q115	ES, TCP[11]
0	5	4	3	mxB1	166/66	Q127	ES, PPGA[11]
0	5	4	3	mxB1	133/66	SL27D	TCP[11]
0	5	4	3	mxB1	133/66	SL27C	PPGA[11]
0	5	4	3	mxB1	150/60	SL26U	TCP[11]
0	5	4	3	mxB1	150/60	SL27B	PPGA[11]
0	5	4	3	mxB1	166/66	SL26T	TCP[11]
0	5	4	3	mxB1	166/66	SL27A	PPGA[11]
0	5	8	1	myA0	166/66	Q255	TCP[16]
0	5	8	1	myA0	200/66	Q146	TCP[16]
0	5	8	1	myA0	233/66	Q147	TCP[16]
0	5	8	1	myA0	200/66	SL28P	TCP[16]
0	5	8	1	myA0	233/66	SL28Q	TCP[16]
0	5	8	1	myA0	266/66	Q250	TCP[19]

NOTES:

- For a definition of STD, VR, VRE, MD, VRE/MD, refer to Specification Change 18 and S-Spec 10 in this document. ES refers to Engineering Samples. DP indicates that this part can only be used as a dual processor. CPU Type of"2" or "0 or 2" indicates this part supports dual processing.
- The Type corresponds to bits [13:12] of the EDX register after RESET, bits [13:12] of the EAX register after the CPUID instruction is executed. This is shown as 2 different values based on the operation of the device as the primary processor or the dual processor upgrade.
- The Family corresponds to bits [11:8] of the EDX register after RESET, bits [11:8] of the EAX register after the CPUID instruction is executed.
- The Model corresponds to bits [7:4] of the EDX register after RESET, bits [7:4] of the EAX register after the CPUID instruction is executed.
- The Stepping corresponds to bits [3:0] of the EDX register after RESET, bits [3:0] of the EAX register after the CPUID instruction is executed.
- The absence of a package type in the comments column means the processor is SPGA by default.

1. T_{CASE} = 60°C.
2. VRT Intel's Voltage Reduction Technology: The V_{CC} for I/O is 3.3V, but the core V_{CC}, accounting for about 90% of power usage, is reduced to 2.9V, to reduce power consumption and heating.
3. No Kit means that part meets the specifications but is not tested to support 82498/82493 and 82497/82492 cache timings.
4. STEPPING The cB1 stepping is logically equivalent to the C2-step, but on a different manufacturing process. The mcB1 step is logically equivalent to the cB1 step (except it does not support DP, APIC or FRC). The mcB1, mA1, mA4 and mcC0-steps also use Intel's VRT (Voltage Reduction Technology, see note 2 above) and are available in the TCP and/or SPGA package, primarily to support mobile applications. The mxA3 is logically equivalent to the xA3 stepping (except it does not support DP or APIC). All mobile steppings are distinguished by an additional "m" prefix, for "mobile". All steppings of the Pentium® processor with MMX™ technology are distinguished by an additional "x" prefix.
5. This is a boxed Pentium processor without an attached fan heatsink.
6. This is a boxed Pentium processor with an attached fan heatsink.
7. These parts do not support boundary scan. S106J was previously marked (and is the same as) SK106J.
8. DP, FRC and APIC features are not supported on these parts.
9. These parts are packaged in the Plastic Pin Grid Array (PPGA) package. For additional specifications of this package, see specification clarifications 27 and 28.
10. Some Q0951F units are marked on the bottom side with spec number Q0951 and with an additional line immediately underneath spelling out "Full Feature" to properly identify the unit.
11. This is a mobile Pentium processor with MMX technology with a core operating voltage of 2.285V– 2.665V.
12. This is a desktop Pentium processor with MMX technology with a core operating voltage of 2.7V– 2.9V.
13. Max Freq means the part may run only at the maximum specified frequency. Specifically, a 200-MHz may be run at 200 MHz +0/–5 MHz (195 – 200 MHz) and a 166-MHz may be run at 166 MHz +0/–5 MHz (161 – 166 MHz).
14. SU114 and SL25H units are marked on the bottom side with a VMU code of "VSS". This is incorrect. The proper VMU code should read "VSU", since the units do not support DP, FRC or APIC features. This spec number has been discontinued and is replaced by spec number SY045.
15. This part also ships as a boxed processor with an unattached fan heatsink.
16. This is a mobile Pentium processor with MMX technology with a core operating voltage of 1.665V– 1.935V and an I/O operating voltage of 2.375V – 2.625V.
17. This is a mobile Pentium processor with MMX technology with a core operating voltage of 2.10V– 2.34V.
18. Some SL23T parts are incorrectly marked with "SSS" on the final line of the bottom side marking. The marking should read "2.8V" in this location. The incorrect marking does not affect the specification nor the operation of those units.
19. This is a mobile Pentium Processor with MMX technology with a core operating voltage of 1.850V– 2.150V and an I/O operating voltage of 2.375V – 2.625V.

Summary Table of Changes

The following table indicates the Specification Changes, S-Specs, Errata, Specification Clarifications or Documentation Changes, which apply to the listed 75/90/100/120/133/150/166/200/233 MHz Pentium processor and Pentium processor with MMX technology steppings. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLE

X:	Erratum, Specification Change or Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
DP:	Dual processing related errata.
AP:	APIC related errata.
TCP:	Applies to the listed stepping of a mobile Pentium processor in a TCP package only.
Shaded:	This item is either new or modified from the previous version of the document.

No.	B1	B3	B5	C2	mA1	cB1	mcB1	cC0	mA4	mcC0	E0	xA3	mxA3	xB1	mxB1	myA0	Plans	SPECIFICATION CHANGES
1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Doc	IDT limit violation causes GP fault, not interrupt 8
2										X							Doc	150 MHz active power dissipation (typical) change
3	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Doc	Redundant timing spec: t_{42d} for all bus frequencies
4															X		Doc	Stop clock power
5														X	X		Doc	Max valid delay A3 – A31
6															X		Doc	Max valid delay data bus D0 – D63
7															X		Doc	Maximum Stop-Grant/AutoHALT Power
8															X		Doc	TCK V_{IL}
9														X	X		Doc	2/7 bus fraction
10														X			Doc	233-MHz I_{CC} speciifications
11														X			Doc	Active power
12															X		Doc	133-MHz current and power specifications
13															X		Doc	1/2 bus fraction
14															X		Doc	Maximum thermal design power

No.	B1	B3	B5	C2	mA1	cB1	mcB1	cC0	mA4	mcC0	E0	xA3	mxA3	xB1	mxB1	myA0	Plans	SPECIFICATION CHANGES (Cont'd)
15												X		X			Doc	PCHK# Low state output current in DP mode
16												X	X	X	X		Doc	Absolute maximum rating for V_{CC3}
17															X		Doc	120/60 MHz V_{CC}, I_{CC} , power, DC and AC specifications
18																X	Doc	166- and 266-MHz V_{CC2}, I_{CC} and power specifications
No.	**B1**	**B3**	**B5**	**C2**	**mA1**	**cB1**	**mcB1**	**cC0**	**mA4**	**mcC0**	**E0**	**xA3**	**mxA3**	**xB1**	**mxB1**	**myA0**	**Plans**	**S-SPECS**
1					X				X								Fixed	t_{6a}, t_{6b}, max valid delay A31 – A3, BE7# – BE0#, ADS#, LOCK#
2					X				X								Fixed	Minimum required voltage separation between Vcc_3 and Vcc_2
3						X	X										Fixed	V_{IH} for TRST#
4							X										Fixed	V_{IL} for BF and BF1 is reduced
5										X							Fixed	Boundary scan timing changes
6										X							Fixed	SPGA Vcc_2 supply voltage change
7					X				X								Fixed	AC specifications for the Pentium Processor with Voltage Reduction Technology
8							X			X							Fixed	Reduced V_{IL} for TCK
9	X	X	X	X		X											Fixed	Mixing steppings in dual processing mode
10	X	X	X	X		X		X									Fixed	MD/VR/VRE specifications
11				X													Fixed	120-MHz and 133-MHz parts (Q0707, Q0708, Q0711, Q0732, Q0733, Q0751, Q0775, SK086, SX994, SK098, SU033) do not support dual processing
12				X													Fixed	120-MHz and 133-MHz parts (Q0707, Q0708, Q0711, Q0733, Q0751, Q0775, SK086, SK098) do not support FRC
13				X													Fixed	120-MHz and 133-MHz parts (Q0707, Q0708, Q0711, Q0733, Q0751, Q0775, SK086, SK098) V_{CC} to CLK startup specification
14				X													Fixed	120-MHz and 133-MHz parts (Q0707, Q0708, Q0711, Q0733, Q0751, Q0775, SK086, SK098) current leakage on PICD1 pin

No.	B1	B3	B5	C2	mA1	cB1	mcB1	cC0	mA4	mcC0	E0	xA3	mxA3	xB1	mxB1	myA0	Plans	S-SPECS (Cont'd)
15													X				Fixed	Mobile stop clock power
16												X	X				Fixed	I_{IH}, input leakage current
17												X	X				NoFix	Max valid delay A3 – A31 (Replaced by a Spec Change)
18													X				Fixed	Max valid delay ADS#
19													X				Fixed	Max valid delay HITM#
20													X				NoFix	Max valid delay data bus D0 – D63 (Replaced by a Spec Change)
21												X					Fixed	Desktop stop clock power
22															X		Fix	Min valid delay data bus D0 – D63

No.	B1	B3	B5	C2	mA1	cB1	mcB1	cC0	mA4	mcC0	E0	xA3	mxA3	xB1	mxB1	myA0	Plans	ERRATA
1	X	X	X														Fixed	Branch trace messages during lock cycles
2	X	X	X														Fixed	Breakpoint or single-step may be missed for one instruction following STI
3	X	X	X														Fixed	I/O restart does not function during single stepping or data breakpoint exceptions
4	X	X	X														Fixed	NMI or INIT in SMM with I/O restart during single-stepping
5	X	X	X														Fixed	SMI# and FLUSH# during shutdown
6	X	X	X														Fixed	No shutdown after IERR#
7	X	X	X														Fixed	FLUSH# with a breakpoint pending causes false DR6 values
8	X																Fixed	Processor core may not serialize on bus idle
9	X	X	X	X	X	X											Fixed	SMIACT# premature assertion during replacement writeback cycle
10	Superceded by a Specification Change																	STPCLK# deassertion not recognized for 5 CLKs after BRDY# returned
11	X	X	X														Fixed	Future Pentium® OverDrive® processor FERR# contention in two-socket systems
12	X																Fixed	Code cache lines are not invalidated if snooped during AutoHALT or Stop-Grant states

No.	B1	B3	B5	C2	mA1	cB1	mcB1	cC0	mA4	mcC0	E0	xA3	mxA3	xB1	mxB1	myA0	Plans	ERRATA (Cont'd)
13	X																Fixed	STPCLK# assertion during execution of the HALT instruction hangs system
14	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	NoFix	NMI or INIT during HALT within SMM may cause large amount of bus activity
15	X	X	X	X	X	X	X	X	X	X	X						Fixed	RUNBIST restrictions when run through boundary scan circuitry
16	X	X	X	X		X		X			X						Fixed	FRC mode miscompare due to uninitialized internal register
17	Superceded by a Specification Change																	STPCLK# restrictions during EWBE#
18	X	X	X														Fixed	Multiple allocations into branch target buffer
19	X	X	X														Fixed	100-MHz REP MOVS speed path
20	X	X	X														Fixed	Overflow undetected on some numbers on FIST
21	X	X	X														Fixed	Six operands result in unexpected FIST operation
22	X																Fixed	Snoop with table-walk violation may not invalidate snooped line
23	X	X															Fixed	Slight precision loss for floating-point divides on specific operand pairs
24	X	X	X														Fixed	FLUSH#, INIT or machine check dropped due to floating-point exception
25	X	X	X	X	X	X	X		X								Fixed	Floating-point operations may clear alignment check bit
26	X	X	X	X	X	X	X		X								Fixed	CMPXCHG8B across page boundary may cause invalid opcode exception
27	X	X	X									X	X	X	X	X	NoFix	Single-step debug exception breaks out of HALT
28	X	X	X	X	X	X	X	X	X	X	X						Fixed	Branch trace message corruption
29	X	X	X	X		X											Fixed	FRC lock-step failure during APIC write
30	X	X	X	X	X	X	X		X								Fixed	BE4# – BE0# sampled incorrectly at min V_{IH}
31	X	X	X	X		X											Fixed	Incorrect PCHK# output during boundary scan if in DP mode

No.	B1	B3	B5	C2	mA1	cB1	mcB1	cC0	mA4	mcC0	E0	xA3	mxA3	xB1	mxB1	myA0	Plans	ERRATA (Cont'd)
32	X	X	X	X	X	X	X		X								Fixed	EIP altered after specific FP operations followed by MOV Sreg, Reg
33	X	X	X	X	X	X	X	X	X	X	X						Fixed	WRMSR into illegal MSR does not generate GP Fault
34	X	X	X														Fixed	Inconsistent data cache state from concurrent snoop and memory write
35	X	X	X														Fixed	BE3# – BE0# not driven during boundary scan if RESET high
36	X	X	X	X	X	X	X	X	X	X	X						Fixed	Incorrect FIP after RESET
37	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	NoFix	Second assertion of FLUSH# not ignored
38	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	NoFix	Segment limit violation by FPU operand may corrupt FPU state
39	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	NoFix	FP exception inside SMM with pending NMI hangs system
40	X	X	X	X	X	X	X										Fixed	Current in Stop Clock state exceeds specification
41	X	X	X	X	X	X	X		X		X						Fixed	STPCLK# buffer samples incorrectly during boundary scan testing
42	X	X	X	X	X	X	X										Fixed	Incorrect decode of certain 0F instructions
43	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	NoFix	Data breakpoint deviations
44	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	NoFix	Event monitor counting discrepancies
45	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	NoFix	VERR type instructions causing page fault task switch with T bit set may corrupt CS:EIP
46	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	NoFix	BUSCHK# interrupt has wrong priority
47	X	X	X	X	X				X		X						Fixed	BF and CPUTYP buffers sample incorrectly during boundary scan testing
48	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	NoFix	Matched but disabled data breakpoint can be lost by STPCLK# assertion
49	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	NoFix	STPCLK# ignored in SMM when INIT or NMI pending
50	X	X	X	X	X	X	X	X	X	X	X			X	X		Fixed	STPCLK# pullup not engaged at RESET

No.	B1	B3	B5	C2	mA1	cB1	mcB1	cC0	mA4	mcC0	E0	xA3	mxA3	xB1	mxB1	myA0	Plans	ERRATA (Cont'd)
51	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	NoFix	A fault causing a page fault can cause an instruction to execute twice
52	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	NoFix	Machine check exception pending, then HLT, can cause skipped or incorrect instruction, or CPU hang
53	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	NoFix	FBSTP stores BCD operand incorrectly If address wrap and FPU error both occur
54	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	NoFix	V86 interrupt routine at illegal privilege level can cause spurious pushes to stack
55	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	NoFix	Corrupted HLT flag can cause skipped or incorrect instruction, or CPU hang
56	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	NoFix	Benign exceptions can erroneously cause double fault
57	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	NoFix	Double fault counter may not increment correctly
58					X		X		X	X							Fixed	Some input pins may float high when core V_{CC} powers up after I/O V_{CC} (mobile CPU)
59	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	NoFix	Short form of mov EAX / AX / AL may not pair
60	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	NoFix	Turning off paging may result in prefetch to random location
61	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	NoFix	STPCLK# ,FLUSH# or SMI# after STI
62	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	NoFix	REP string instruction not interruptable by STPCLK#
63	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	NoFix	Single step may not be reported on first instruction after FLUSH#
64	X	X	X	X		X		X			X	X	X	X	X	X	NoFix	Double fault may generate illegal bus cycle
65	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	NoFix	TRST# not asynchronous
66	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	NoFix	STPCLK# on RSM to HLT causes non-standard behavior
67	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	NoFix	Code cache dump may cause wrong IERR#
68	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	NoFix	Asserting TRST# pin or issuing JTAG instructions does not exit TAP Hi-Z state

No.	B1	B3	B5	C2	mA1	cB1	mcB1	cC0	mA4	mcC0	E0	xA3	mxA3	xB1	mxB1	myA0	Plans	ERRATA (Cont'd)
69	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	NoFix	ADS# may be delayed after HLDA deassertion
70	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	NoFix	Stack underflow in IRET gives #GP, not #SS
71	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	NoFix	Performance monitoring pins PM[1:0] may count the events incorrectly
72												X	X				Fixed	BIST is disabled
73												X	X	X	X	X	NoFix	Branch trace messages may cause system hang
74												X	X				Fixed	Enabling RDPMC in CR4 and also using SMM may cause shutdown
75												X	X			X	Fixed	Event monitor counting discrepancies (fix)
76												X	X	X	X	X	NoFix	Event monitor counting discrepancies (Nofix)
77												X	X				Fixed	INVD may leave valid entries in the cache due to snoop interaction
78												X	X	X	X	X	NoFix	TLB update is blocked after a specific sequence of events with a misaligned descriptor
79	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	NoFix	Erroneous debug exception on POPF/IRET instructions with a GP fault
80												X	X	X	X	X	NoFix	CR2 and CR4 Content upon Return from SMM
81	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Fix	Invalid operand with locked CMPXCHG8B instruction
82	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Fix	Event monitor counting discrepancy
1DP	X	X	X														Fixed	Problem with external snooping while two cycles are pending on the bus
2DP	X	X	X														Fixed	STPCLK# assertion and the Stop-Grant bus cycle
3DP	X	X	X														Fixed	External snooping with AHOLD asserted may cause processor to hang
4DP	X	X	X														Fixed	Address parity check not supported in dual processing mode
5DP	X	X															Fixed	Inconsistent cache state may result from interprocessor pipelined READ into a WRITE

No.	B1	B3	B5	C2	mA1	cB1	mcB1	cC0	mA4	mcC0	E0	xA3	mxA3	xB1	mxB1	myA0	Plans	ERRATA (Cont'd)
6DP	X	X	X														Fixed	Processors hang during Zero WS, pipelined bus cycles
7DP	X	X	X														Fixed	Bus lock-up problem in a specific dual processing mode sequence
8DP	X	X	X	X		X											Fixed	Incorrect assertion of PHITM# without PHIT#
9DP	X	X	X	X		X											Fixed	Double issuance of read cycles
10DP	X	X	X	X		X											Fixed	Line invalidation may occur on read or prefetch cycles
11DP	X	X	X	X		X		X			X						Fixed	EADS# or floating ADS# may cause extra invalidates
12DP	X	X	X	X		X											Fixed	HOLD and BOFF# during APIC cycle may cause dual processor arbitration problem
13DP	X	X	X	X		X											Fixed	System hang after hold during local APIC second INTA cycle
14DP	X	X	X	X		X		X			X						Fixed	External snoop can be incorrectly invalidated
15DP	X	X	X	X		X		X			X	X		X			NoFix	STPCLK# re-assertion recognition constraint with DP
16DP	X	X	X	X		X		X			X	X		X			NoFix	Second assertion of FLUSH# during flush acknowledge cycle may cause hang
17DP														X			NoFix	Asserting FLUSH# may cause a processor deadlock in a DP system with a 2/7 bus fraction
1AP	X	X	X														Fixed	Remote read message shows valid status after a checksum error
2AP	X	X	X														Fixed	Chance of clearing an unread error in the error register
3AP	X	X	X														Fixed	Writes to error register clears register
4AP	X	X	X														Fixed	Three interrupts of the same priority causes lost local interrupt
5AP	X	X	X														Fixed	APIC bus synchronization lost due to checksum error on a remote read message
6AP	X	X	X														Fixed	HOLD during a READ from local APIC register may cause incorrect PCHK#
7AP	X	X	X														Fixed	HOLD during an outstanding interprocessor pipelined APIC cycle hangs processor

No.	B1	B3	B5	C2	mA1	cB1	mcB1	cC0	mA4	mcC0	E0	xA3	mxA3	xB1	mxB1	myA0	Plans	ERRATA (Cont'd)
8AP	X	X	X														Fixed	PICCLK reflection may cause an APIC checksum error
9AP	X	X	X	X		X		X			X						Fixed	Spurious interrupt in APIC through local mode
10AP	X	X	X														Fixed	Potential for lost interrupts while using APIC in through Local mode
11AP	X	X	X	X		X											Fixed	Back to back assertions of HOLD or BOFF# may cause lost APIC write cycle
12AP	X	X	X	X		X		X									Fixed	System hangs when BOFF# is asserted during second internal INTA cycle
13AP	X	X	X	X		X		X			X						Fixed	APIC pipeline cycle during cache linefill causes restarted cycle to lose its attribute
14AP	X	X	X	X		X		X			X	X		X		X	NoFix	INIT and SMI via the APIC three-wire bus may be lost
15AP								X			X						Fixed	IERR# in FRC lock-step mode during APIC write
16AP	X	X	X	X	X	X	X	X			X						Fixed	Inadvertent BRDY# during external INTA cycle with BOFF#
17AP	X	X	X	X		X		X			X						Fixed	APIC read cycle may not complete upon assertion of BOFF# and HOLD
18AP	X	X	X	X		X		X			X	X		X		X	NoFix	PICCLK must toggle for at least twenty cycles before RESET
19AP												X					Fixed	APIC ID can not be changed
1TCP	X																Fixed	CPU may not reset correctly due to floating FRCMC# pin
2TCP	X			X	X		X		X	X	X						Fixed	BRDY# does not have buffer selection capability

No.	B1	B3	B5	C2	mA1	cB1	mcB1	cC0	mA4	mcC0	E0	xA3	mxA3	xB1	mxB1	myA0	Plans	SPECIFICATION CLARIFICATIONS
1	X	X	X	X		X		X			X	X		X			Doc	Pentium processor's response to startup and init IPIs
2	X	X	X														Doc	APIC timer use clarification
3	X	X	X														Fixed	PICCLK reflection may cause APIC checksum errors and dropped IPIs
4	X	X	X														Fixed	Boundary scan RUNBIST register requires initialization prior to use
5	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Doc	Only one SMI# can be latched during SMM

No.	B1	B3	B5	C2	mA1	cB1	mcB1	cC0	mA4	mcC0	E0	xA3	mxA3	xB1	mxB1	myA0	Plans	SPECIFICATION CLARIFICATIONS (Cont'd)
6	X	X	X	X		X		X			X	X	X	X	X	X	Doc	APIC 8-bit access
7	X	X	X	X		X		X			X	X	X	X	X	X	Doc	LOCK prefix excludes APIC memory space
8	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Doc	SMI# activation may cause a nested NMI handling
9	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Doc	Code breakpoints set on meaningless prefixes not guaranteed to be recognized
10	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Doc	Resume flag should be set by software
11	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Doc	Data breakpoints on INS delayed one iteration
12	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Doc	When L1 cache disabled, inquire cycles are blocked
13	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Doc	Serializing operation required when one CPU modifies another CPU's code
14	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Doc	For correct translations, the TLB should be flushed after the PSE bit in CR4 is set
15	X	X	X	X		X		X			X	X		X			Doc	When APIC enabled, its 4K block should not be used in regular memory
16	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Doc	Extra code break can occur on I/O or HLT instruction if SMI coincides
17												X	X	X	X	X	Doc	LRU maybe updated for non-cacheable cycles
18	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Doc	FYL2XP1 does not generate exceptions for X out of range
19	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Doc	Enabling NMI inside SMM
20	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Doc	BF[1:0] must not change values while RESET is active
21	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Doc	Active A20M# during SMM
22	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Doc	POP[ESP] with 16-bit stack size

No.	B1	B3	B5	C2	mA1	cB1	mcB1	cC0	mA4	mcC0	E0	xA3	mxA3	xB1	mxB1	myA0	Plans	DOCUMENTATION CHANGES
1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Doc	JMP cannot do a nested task switch, Volume 3, page 13-12
2					X		X		X	X							Doc	Incorrect TCP pinout
3	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Doc	Interrupt sampling window, Volume 3, page 23-39
4	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Doc	FSETPM is like NOP, not like FNOP
5	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Doc	Errors in three tables of special descriptor types
6												X		X			Doc	iCOMP® index 2.0 rating correction
7												X		X			Doc	Default setting for BF1-0 on a Pentium processor with MMX™ technology
8	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Doc	FPU exceptions cause branch trace messages
9													X		X		Doc	1/3 bus fraction
10															X		Doc	Die size reduction
11												X	X	X	X		Doc	Absolute maximum rating for V_{CC3}
12	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Doc	Invalid arithmetic operations and masked responses to them relative to FIST/FISTP instruction

SPECIFICATION CHANGES

The Specification Changes listed in this section apply to the *Pentium® Processor Family Developer's Manual,* (Order Number 241428), the *Intel Architecture Software Developer's Manual,* Volume 1: Basic Architecture (Order Number 243190); Volume 2: Instruction Set Reference Manual (Order Number 243191), the *Pentium® Processor at iCOMP® index 610\75 MHz, 735\90 MHz, 815\100 MHz, 1000\120 MHz, 1110\133 MHz* datasheet, (Order Number 241997), or the *Pentium® Processor with MMX™ Technology* datasheet (Order Number 243185). Specification Changes may be incorporated into future versions of the appropriate document(s).

1. IDT Limit Violation Causes GP Fault, Not Interrupt 8

The last sentence in Section 9.3 of the *Pentium® Processor Family Developer's Manual*, Volume 3, says about exception handling in Real Mode: "If an interrupt occurs and its entry in the interrupt table is beyond the limit stored in the IDTR register, a double-fault exception is generated." In fact, in the Pentium® processor, there is no difference between Real and Protected Mode when an IDT limit violation occurs. It generates interrupt 13: General Protection Fault in both modes.

2. 150 MHz Active Power Dissipation (typical) Change

These new specifications for Pentium processors at 150 MHz active power dissipation (typical) apply ONLY to the mcC0 stepping (mobile specific) TCP parts. The previous, preliminary range giving typical power (3.8 to 5.0 W) for V_{CC} Core of 2.9V has been reduced to the range (3.4 to 4.5 W). Parts with a V_{CC} Core of 3.1V are specified to have a typical power range (3.8 to 5.0 W).

Parameter	Previous Value (Watts)	Current Value (Watts)
150 MHz Active Power	N/A	3.8 – 5.0 W @ 3.1V
(typical) Dissipation	3.8 – 5.0 W @ 2.9V	3.4 – 4.5 W @ 2.9V

3. Redundant Timing Specification: t_{42d} for All Bus Frequencies (50, 60 and 66 MHz)

t_{42d} is the minimum hold time required when BRDYC# is used as a configuration signal and when RESET is driven synchronously with CLK. This timing specification is redundant because it is a subset of t_{21}, hold time for BRDYC# with respect to CLK. Therefore, t_{42d} will be removed from all future documentation.

4. Stop Clock Power

This is the new specification condition for the maximum stop clock power dissipation for the mobile Pentium processor with MMX™ technology. This will replace both the original specification in the *Mobile Pentium® Processor with MMX™ Technology* datasheet as well as S-Spec 15, mobile stop clock power.

Parameter	Previous Power	New Power
Maximum Stop Clock Power Dissipation	50 mW	50 mW (1)

NOTES:

1. Maximum stop clock power dissipation is measured at 50°C. At maximum temperature of 95°C, parts will typically draw 90mW.

5. Max Valid Delay A3 – A31

These are the new specifications for the maximum valid delay for t_{6e} of the Pentium processor with MMX technology. This will replace both the original specifications of t_{6e} in the *Pentium® Processor with MMX™ Technology* datasheet as well as S Spec 17, mobile max valid delay A3 – A31.

Symbol	Parameter	Bus Frequency	Previous Max Valid Delay	New Max Valid Delay
t_{6e}	A3 – A31	60 MHz (mobile only)	6.3 ns	7.0 ns
t_{6e}	A3 – A31	66 MHz	6.3 ns	6.6 ns

6. Max Valid Delay Data Bus D0 – D63

These are the new specifications for the maximum valid delay for t_{12} of mobile Pentium processor with MMX technology. This will replace both the original specifications for t_{12} in the *Mobile Pentium® Processor with MMX™ Technology* datasheet as well as S Spec 20, mobile max valid delay D0 – D63.

Symbol	Parameter	Bus Frequency	Previous Max Valid Delay	New Max Valid Delay
t_{12}	D0 – D63	60 MHz	7.5 ns	8.3 ns
t_{12}	D0 – D63	66 MHz	7.5 ns	8.0 ns

7. Maximum Stop-Grant/AutoHALT Power

These are the new specifications for the maximum Stop-Grant Power/AutoHALT dissipation for mobile Pentium processor with MMX technology. These will replace the original specifications in the *Mobile Pentium® Processor with MMX™ Technology* datasheet.

When in Stop-Grant/AutoHALT Power Down mode, the B-step mobile Pentium processor with MMX technology has a new power-savings feature which allows it to Power Down additional internal circuitry compared to the A-step. This enables even lower power dissipation while in the Stop-Grant/AutoHALT Power Down mode when this feature is enabled. In order to enable this feature, TR12 bit 21 must be set to 1 (the default is 0 or disabled).

Parameter	Core/Bus Frequency	Previous Power (1)	New Power (2)
Maximum Stop-Grant/AutoHALT Power	133/66 MHz	N/A	0.86W
Maximum Stop-Grant/AutoHALT Power	150/60 MHz	1.60 W	0.93W
Maximum Stop-Grant/AutoHALT Power	166/66 MHz	1.75 W	1W

NOTES:

1. This corresponds to the default state which has bit TR12.21 cleared.
2. This corresponds to the state with bit TR12.21 set.

8. TCK V_{IL}

This is the new specification for the V_{IL} of TCK on the mobile Pentium processor with MMX technology. This will replace the original specification in the *Mobile Pentium® Processor with MMX™ Technology* datasheet.

Symbol	Parameter	Previous V_{IL}	New V_{IL}
V_{IL}	TCK	0.8V	0.6V

9. 2/7 Bus Fraction

Bus Frequency Selections

BF1	BF0	Bus/Core Ratio	Max Bus/Core Frequency (MHz)	Min Bus/Core Frequency (MHz)
0	1	1/3	66/200	33/100
0	0	2/5	66/166	33/83
1	0	1/2 (1)	66/133	33/66
1	1	2/7	66/233	33/116

NOTES:

1. This is the default bus to core ratio for the Pentium® processor with MMX™ technology. If the BF pins are left floating, the processor will be configured for the 1/2 bus to core frequency ratio.

10. 233-MHz I_{CC} Specifications

Specifications
(Measured at Vcc_2 =2.9V and Vcc_3 =3.6V)

Symbol	Parameter	Min	Max	Unit	Notes
I_{CC2}	Power Supply Current		6500	mA	233 MHz (1)
I_{CC3}	Power Supply Current		750	mA	233 MHz (1)

NOTES:

1. This value should be used for power supply design. It was determined using a worst case instruction mix and maximum V_{CC}. Power supply transient response and decoupling capacitors must be sufficient to handle the instantaneous current changes occurring during transitions from Stop Clock to full Active modes.

11. Active Power

Power Dissipation Requirements for Thermal Design
(Measured at Vcc_2 =2.8V and Vcc_3 =3.3V

Parameter	Typical (1)	Max (2)	Unit	Notes
Active Power	7.9 (3)	17.0 (4)	Watts	233 MHz

NOTES:

1. This is the typical power dissipation in a system. This value is expected to be the average value that will be measured in a system using a typical device at Vcc_2 = 2.8V running typical applications. This value is highly dependent upon the specific system configuration. Typical power specifications are not tested.

2. Systems must be designed to thermally dissipate the maximum active power dissipation. It is determined using worst case instruction mix with Vcc_2 = 2.8V and Vcc_3 = 3.3 and also takes into account the thermal time constants of the package.
3. Active Power (typ) is the average power measured in a system using a typical device running typical applications under normal operating conditions at nominal V_{CC} and room temperature.
4. Active Power (max) is the maximum power dissipation under normal operating conditions at nominal Vcc_2, worst-case temperature, while executing the worst case power instruction mix. Active power (max) is equivalent to Thermal Design Power (max).

12. 133-MHz Current and Power Specifications

These are the new power specifications for the unannounced 133 MHz-mobile Pentium processor with MMX technology. These specifications will be part of the *Mobile Pentium® Processor with MMX™ Technology* datasheet.

I_{CC} Specifications

Symbol	Parameter	Min	Max	Unit	Notes
I_{CC2}	Power Supply Current		3.3	A	1
I_{CC3}	Power Supply Current		0.4	A	1

NOTES:

1. This value should be used for power supply design. It was determined using a worst case instruction mix and maximum V_{CC}. Power supply transient response and decoupling capacitors must be sufficient to handle the instantaneous current changes occurring during transitions from Stop Clock to full Active modes.

Power Dissipation Requirements for Thermal Design

Parameter	Typical	Max	Unit	Notes
Thermal Design Power	N/A (6)	7.8	Watts	1
Active Power	4.4	N/A	Watts	2, 5
Stop-Grant/AutoHALT Power	N/A	0.86	Watts	3
Stop Clock Power	0.02	0.05	Watts	4

NOTES:

1. This is the typical power dissipation in a system. This value is expected to be the average value that will be measured in a system using a typical device at Vcc_2 = 2.45V and Vcc_3 = 3.3V running typical applications. This value is highly dependent upon the specific system configuration. Typical power specifications are not tested.
2. Systems must be designed to thermally dissipate the maximum active power dissipation. It is determined using a worst-case instruction mix with Vcc_2 = 2.45V and Vcc_3 = 3.3V. The use of nominal V_{CC} in this measurement takes into account the thermal time constant of the package.
3. Stop-Grant/AutoHALT Power Down Power Dissipation is determined by asserting the STPCLK# pin or executing the HALT instruction. To achieve these, bit TR12.21 must be set.
4. Stop Clock Power Dissipation is determined at 50°C by asserting the STPCLK# pin and then removing the external CLK input. At maximum temperature of 95°C, parts will typically draw 90 mW.
5. Active Power is the average power measured in a system using a typical device running typical applications under normal operating conditions at nominal V_{CC} and room temperature.
6. For TDP (typ) refer to the Mobile Design Considerations application note.

13. 1/2 Bus Fraction

The 1/2 Bus Fraction is supported for the 133/66 MHz mobile Pentium processor with MMX technology. This will be added to Table 6 in the *Mobile Pentium® Processor with MMX™ Technology* datasheet.

Mobile Bus Frequency Selections

BF1	BF0	Bus/Core Ratio	Max Bus/Core Frequency (MHz)	Min Bus/Core Frequency (MHz)
1	0	1/2 (1)	66/133	33/66

NOTES:

1. This is the default bus to core ratio for the Pentium® processor with MMX™ technology. If the BF pins are left floating, the processor will be configured for the 1/2 bus to core frequency ratio.

14. Maximum Thermal Design Power

This is the new power specification for the 166 MHz (B-Step) mobile Pentium processor with MMX technology.

Power Dissipation Requirements for Thermal Design

Parameter	Typical (1)	Max (2)	Unit	Notes
Thermal Design Power	N/A (3)	9.5	Watts	166 MHz A-Step
Thermal Design Power	N/A (3)	9.0	Watts	166 MHz B-Step

NOTES:

1. This is the typical power dissipation in a system. This value is expected to be the average value that will be measured in a system using a typical device at Vcc_2 = 2.45V and Vcc_3 = 3.3V running typical applications. This value is highly dependent upon the specific system configuration. Typical power specifications are not tested.
2. Systems must be designed to thermally dissipate the maximum active power dissipation. It is determined using a worst-case instruction mix with Vcc_2 = 2.45V and Vcc_3 = 3.3V. The use of nominal V_{CC} in this measurement takes into account the thermal time constant of the package.
3. For typical Thermal Design Power refer to the Mobile Design Considerations application note.

15. PCHK# Low State Output Current in DP Mode

In the *Pentium® Processor with MMX™ Technology* datasheet, Note 4 on page 31 should be modified. Specifically, the PCHK# in a DP system should be changed from 14 mA to 13 mA. The new note should read:

4. "In dual processing systems, up to a 9 mA load from the second processor may be observed on the PCHK# signal. Based on silicon characterization data, VOL3 of PCHK# will remain less than 400 mV even with a 9 mA load. PCHK# VOL3 will increase to approximately 500 mV with a 13 mA load (worst case for a DP system with a 4 mA system load)."

16. Absolute Maximum Rating for V_{CC3}

In the 1997 *Pentium® Processor Family Developer's Manual*, Section 7.2, Table 7-1, it states the maximum V_{CC3} is 4.6V. This applies to the Pentium processor 75/90/100/120/133/150/166/200 only. The maximum V_{CC3} for the Pentium processor with MMX technology is 4.0V.

17. 120/60 MHz V_{CC}, I_{CC}, Power, DC and AC Specifications

These are the new V_{cc}, I_{cc}, power dissipation, DC and AC specifications for the 120/60 MHz mobile Pentium processor with MMX technology. All other specifications are identical to the 150/60 MHz mobile Pentium processor with MMX technology.

V_{cc} Specifications

Symbol	Parameter	Nominal	Max	Unit
V_{CC2}	Core Supply Voltage	2.22	±0.120	Volts
V_{CC3}	I/O Supply Voltage	3.30	±0.165	Volts

I_{cc} Specifications

Symbol	Parameter	Min	Max	Unit
I_{CC2}	Power Supply Current		2600	mA
I_{CC3}	Power Supply Current		370	mA

Power Dissipation Requirements for Thermal Design

Parameter	Typical	Max	Unit
Thermal Design Power		5.70	Watts
Active Power	3.4 (1)		Watts
Stop-Grant/AutoHALT Power (2)		0.67	Watts

NOTES:

1. Active power (typ) is the average power measured in a system using a typical device running typical applications under normal operating conditions at nominal V_{CC} and room temperature.
2. To achieve this, TR12.21 must be set.

3.3V DC Specifications

Symbol	Parameter	Min	Max	Unit
V_{IL3}*	Input Low Voltage TCK Pin		0.5	Volts

*TTL Level

AC Specifications

Symbol	Parameter	Min	Max	Unit
t6a	D/C#, SCYC Valid Delay	0.8		ns
t6e	A3-A31 Valid Delay	0.6		ns
t10b	HITM# Valid Delay	0.7		ns

18. 166- and 266-MHz V_{CC2}, I_{CC2} and Power Specifications

These are the new V_{cc}, I_{cc} and power dissipation specifications for the 166- and 266-MHz mobile Pentium processor with MMX technology with 0.25 micron process. All other specifications are identical to the 200 MHz mobile Pentium processor with MMX technology with 0.25 micron process.

V_{cc} Specifications

Symbol	Parameter	Min	Max	Tolerance	Unit	Notes
V_{CC2}	Core Supply Voltage	1.85	2.15	±0.150	V	@ 266 MHz

I_{cc} Specifications

Symbol	Parameter	Min	Max	Unit	Notes
I_{CC2}	Power Supply Current (1)		2.35 4.00	A A	@ 166 MHz @ 266 MHz
I_{CC3}	Power Supply Current		0.38	A	@ 266 MHz

NOTES:

1. This value should be used for power supply design. It was determined using a worst case instruction mix and a maximum V_{cc} at T_{case} = 0°C. Power supply transient response and decoupling capacitors must be sufficient to handle the instantaneous current changes which occur during transition from Stop Clock to full Active modes.

Power Dissipation Requirements for Thermal Design

Parameter	Typical	Max	Unit	Notes
Thermal Design Power		4.10 7.60	Watts Watts	@ 166 MHz @ 266 MHz
Stop-Grant/AutoHALT Power Down power dissipation (1)		0.42 0.70	Watts Watts	@ 166 MHz @ 266 MHz
Stop Clock Power		0.06	Watts	@ 266 MHz

NOTES:

1. Stop-Grant/AutoHALT Power Down power dissipation is determined by asserting the STPCLK# pin or executing the HALT instruction. When in this mode, the processor has a new feature which allows it to power down additional circuitry to enable lower power dissipation. This is the power without snooping at V_{CC2} = 1.8 V and with TR12 bit 21 set. In order to enable this feature, TR12 bit 21 must be set to 1 (the default is 0 or disabled). Stop-Grant/AutoHALT Power Down power dissipation without TR12 bit 21 set may be higher. The maximum rating may be changed in a future specification update.

Bus/Core (Speed) Ratio Pins on Mobile Pentium® Processor with MMX™ Technology with 0.25 micron Process

BF2 (1)	BF1	BF0	Bus/Core Ratio	Bus/Core Frequency
0	0	0	2/5	66/166
0	0	1	1/3	66/200
0	1	0	1/2	66/133
0	1	1	2/7	66/233
1	0	0	1/4	66/266
1	0	1	Reserved	N/A
1	1	0	Reserved	N/A
1	1	1	Reserved	N/A

NOTES:

1. The mobile Pentium® processor with MMX™ technology with 0.25 micron process uses BF0, BF1 and BF2 pins to determine the bus-to-core frequency ratio. Each processor must be externally configured with the BF2-0 pins to operate in the specific bus fraction mode. Operation out of specification is not supported. For example, a 200 MHz processor only supports a 1/3 bus fraction and not 2/5, 1/2, 2/7 or 1/4 modes.

S-SPECS

1 – 21. Refer to Appendix A of the 1997 Pentium® Processor Family Developer's Manual (Order Number 241428)

22. Min Valid Delay Data Bus D0 – D63

These are the new S Specs for the minimum valid delay for t_{12} of mobile Pentium processor with MMX technology.

Symbol	Parameter	Bus Frequency	Standard Min Valid Delay	S-Spec Min Valid Delay
t_{12}	D0 – D63	60 MHz	1.3 ns	1.1 ns
t_{12}	D0 – D63	66 MHz	1.3 ns	1.1 ns

ERRATA

1 – 60. Refer to Appendix A of the 1997 Pentium® Processor Family Developer's Manual (Order Number 241428)

61. REVISED ERRATUM: STPCLK#, FLUSH# or SMI# After STI

PROBLEM: The STI specification says that external interrupts are enabled at the end of the next instruction after STI. However, external interrupts may be enabled before the next instruction is executed following STI if a STPCLK#, FLUSH# or SMI# is asserted and serviced before the instruction boundary of this next instruction.

IMPLICATION: External interrupts which are assumed blocked until after the instruction following STI may be recognized before this instruction executes.

WORKAROUND: None identified at this time.

STATUS: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

62 – 78. Refer to Appendix A of the 1997 Pentium® Processor Family Developer's Manual (Order Number 241428)

79. Erroneous Debug Exception on POPF/IRET Instructions with a GP Fault

PROBLEM: An erroneous debug exception can occur due to execution of a POPF or IRET instruction in virtual 8086 mode, if there is a data breakpoint set on the address pointed to by SS:ESP, and the POPF or IRET triggers a general protection fault. This occurs in virtual 8086 mode when the IOPL < 3, causing POPF and IRET to trap to the GP fault without accessing the stack. The data breakpoint set on the stack should not be triggered, but in fact it is incorrectly triggered as soon as the GP fault handler is entered.

IMPLICATION: This results in an invalid debug exception where the saved state (CS:EIP in the stack, or in the TSS in the case of a task-switch for interrupt 1) points to the first instruction of the GP Fault handler. This may confuse the debug monitor which expects to find a pointer to an instruction accessing the stack. Note this erratum only occurs during debugging and does not affect normal execution.

WORKAROUND: The debug monitor could be revised to detect this erratum, and to only perform an IRET when this erratum is detected as the cause of entry into the debugger.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

80. CR2 and CR4 Content upon Return from SMM

PROBLEM: Control registers CR2 and CR4 should maintain values across breakpoints or interrupts. CR2 contains the page fault linear address. CR4 is used in protected mode to control operations such as virtual-8086 support, enabling I/O breakpoints, page size extension and machine check exceptions. If CR2 or CR4 are modified in SMM, the original contents of CR2 and CR4 prior to entering SMM are not restored when exiting SMM.

IMPLICATION: If either CR2 or CR4 is modified during the execution of the SMM handler, the modified values will remain after a resume from the SMM handler. The new values in CR2 or CR4 may be unexpected.

WORKAROUND: If the SMM handler needs to modify CR2 or CR4, the handler should store the values of CR2 and CR4 upon entering the SMM handler and restore the values prior to the RSM instruction.

STATUS: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

81. Invalid Operand with Locked CMPXCHG8B Instruction

PROBLEM: The CMPXCHG8B instruction compares an 8 byte value in EDX and EAX with an 8 byte value in memory (the destination operand). The only valid destination operands for this instruction are memory operands. If the destination operand is a register the processor should generate an invalid opcode exception, execution of the CMPXCHG8B instruction should be halted and the processor should execute the invalid opcode exception handler. This erratum occurs if the LOCK prefix is used with the CMPXCHG8B instruction with an (invalid) register destination operand. In this case, the processor may not start execution of the invalid opcode exception handler because the bus is locked. This results in a system hang.

IMPLICATION: If an (invalid) register destination operand is used with the CMPXCHG8B instruction and the LOCK prefix, the system may hang. No memory data is corrupted and the user can perform a system reset to return to normal operation. Note that the specific invalid code sequence necessary for this erratum to occur is not normally generated in the course of programming nor is such a sequence known by Intel to be generated by commercially available software.

This erratum only applies to Pentium processors, Pentium processors with MMX technology, Pentium OverDrive® processors and Pentium OverDrive processors with MMX technology. Pentium Pro processors, Pentium II processors and i486™ and earlier processors are not affected.

WORKAROUND: There are two workarounds for this erratum for protected mode operating systems. Both workarounds generate a page fault when the invalid opcode exception occurs. In both cases, the page fault will be serviced before the invalid opcode exception and thus prevent the lock condition from occurring. The implementation details will differ depending on the operating system. Use one of the following:

1. The first part of this workaround sets the first 7 entries (0-6) of the Interrupt Descriptor Table (IDT) in a non-writeable page. When the invalid opcode exception (exception 6) occurs due to the locked CMPXCHG8B instruction with an invalid register destination (and only then), the processor will generate a page fault if it does not have write access to the page containing entry 6 of the IDT. The second part of this workaround modifies the page fault handler to recognize and correctly dispatch the invalid opcode exceptions that are now routed through the page fault handler.

   Part I, IDT Page Access:

   a. Mark the page containing the first seven entries (0-6) of the IDT as read only by setting bit 1 of the page table entry to zero. Also set CR0.WP (bit 16) to 1. Now when the invalid opcode exception occurs on the locked CMPXCHG8B instruction, the processor will check for write access due to the lock prefix and trigger a page fault since it does not have write access to the page containing entry 6 of the IDT. This page fault prevents the bus lock condition and gives the OS complete control to process the invalid operand exception as appropriate. Note that exception 6 is the invalid opcode exception, so with this scheme an OS has complete control of any program executing an invalid CMPXCHG8B instruction.

   b. Optional: If updates to entries 7-255 of the IDT occur during the course of normal operation, page faults should be avoided on writes to these IDT entries. These page faults can be avoided by aligning the IDT across a 4KB page boundary such that the first seven entries (0-6) of the IDT are on the first read only page and the remaining entries are on a read/writeable page.

II, Page Fault Handler Modifications:

a. Modify the page fault handler to calculate which exception caused the page fault using the fault address in CR2. If the error code on the stack indicates the exception occurred from ring 0 and if the address corresponds to the invalid opcode exception, then pop the error code off the stack and jump to the invalid opcode exception handler. Otherwise continue with the normal page fault handler.

OR

2. This workaround has two parts. First, the Interrupt Descriptor Table (IDT) is aligned such that any invalid opcode exception will cause a page fault (due to the page not being present). Second, the page fault handler is modified to recognize and correctly dispatch the invalid opcode exception and certain other exceptions that are now routed through the page fault handler.

   Part I, IDT Alignment:

   a. Align the Interrupt Descriptor Table (IDT) such that it spans a 4KB page boundary by placing the first entry starting 56 bytes from the end of the first 4KB page. This places the first seven entries (0-6) on the first 4KB page, and the remaining entries on the second page.

   b. The page containing the first seven entries of the IDT must not have a mapping in the OS page tables. This will cause any of exceptions 0-6 to generate a page not present fault. A page fault prevents the bus lock condition and gives the OS complete control to process these exceptions as appropriate. Note that exception 6 is the invalid opcode exception, so with this scheme an OS has complete control of any program executing an invalid CMPXCHG8B instruction.

   Part II, Page Fault Handler Modifications:

   a. Recognize accesses to the first page of the IDT by testing the fault address in CR2. Page not present faults on other addresses can be processed normally.

   b. For page not present faults on the first page of the IDT, the OS must recognize and dispatch the exception which caused the page not present fault. Before proceeding, test the fault address in CR2 to determine if it is in the address range corresponding to exceptions 0-6.

   c. Calculate which exception caused the page not present fault from the fault address in CR2.

   d. Depending on the operating system, certain privilege level checks and adjustments to the interrupt stack may be required before jumping to the normal exception handler in Step e below. If you are an operating system vendor, please contact your local Intel representative for more information.

   e. Jump to the normal handler for the appropriate exception.

Both workarounds should only be implemented on Intel processors that return Family=5 via the CPUID instruction.

82. Event Monitor Counting Discrepancy

PROBLEM: The Pentium processor contains two registers which can count the occurrence of specific events used to measure and monitor various parameters that contribute to the performance of the processor. There is one condition where the counter does not operate as specified:

The “Stall on write to E or M state line” (event 011011) event counts the number of clocks the processor is stalled on a memory write to an E or M state line, while the write buffers are not empty, or EWBE# is negated. In order for event 011011 to accurately count stalled clocks cycles, it must ignore all other stall cases, such as TLB-miss. However, if data resides in the top 4 Kbyte of the physical address space, some stalls due to TLB-miss were also counted.

IMPLICATION: The event monitor counters report an inaccurate count for certain events.

WORKAROUND: Avoid mapping to the top 4 Kbytes of the address space.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

1DP – 16DP. Refer to Appendix A of the Pentium® Processor Family Developer's Manual (Order Number 241428)

17DP. Asserting FLUSH# May Cause a Processor Deadlock in a DP System with a 2/7 Bus Fraction

PROBLEM: In a Dual Processing (DP) system, when FLUSH# is asserted by the system, the bus ownership is first transferred from the primary to the secondary processor. With ownership of the bus, the secondary processor starts to flush its L1 cache. Upon completion of the flush, the secondary processor then returns the bus ownership to the primary processor. Next, the secondary processor will go into a waiting loop until the primary processor finishes flushing its cache and generates the flush acknowledge special cycle. Finally, upon sampling the flush acknowledge special cycle from the primary processor, the secondary processor exits the waiting loop and both processors return to the normal DP mode.

However, FLUSH# may not function correctly due to an internal cycle alignment issue in DP mode when operating with a 2/7 bus fraction. Due to this erratum, the secondary processor fails to wait for the primary processor to release the bus, and initiates a new bus request before the primary processor finishes flushing its L1 cache. In this case, the primary processor does not have access to the bus and therefore cannot finish flushing its cache and cannot generate the flush acknowledgment special cycle; at the same time, the secondary processor has the bus but cannot resume operation until the primary processor issues the flush acknowledgement special cycle.

IMPLICATION: In a DP system which operates at 2/7 bus fraction, the usage of FLUSH# may cause primary and secondary processors to end up in a dead-lock situation.

WORKAROUND: While using the processors in 2/7 bus fractions and DP mode, do not use FLUSH#.

1AP – 19AP. Refer to Appendix A of the Pentium® Processor Family Developer's Manual (Order Number 241428)

1TCP – 2TCP. Refer to Appendix A of the Pentium® Processor Family Developer's Manual (Order Number 241428)

SPECIFICATION CLARIFICATIONS

1. Pentium® Processor's Response to Startup and Init IPIs

The Pentium processor when used as a dual processor upgrade component, will require a STARTUP IPI to wake up this part after the following two situations:

1. After any assertion of RESET.

   Or

2. After any assertion of INIT.

(The assertion of INIT could come from toggling the INIT pin or though an APIC IPI.)

In either case, the dual processor upgrade component will not jump to the RESET Vector, it will instead go into a halt state. If an INIT IPI is then sent to the halted upgrade component, it will be latched and kept pending until a STARTUP IPI is received. From the time the STARTUP IPI is received the CPU will respond to further INIT IPIs but will ignore any STARTUP IPIs. It will not respond to future STARTUP IPIs until a RESET assertion or an INIT assertion (INIT Pin or INIT IPI) happens again.

The Pentium processor when used as a primary processor, will never respond to a STARTUP IPI at any time. It will ignore the STARTUP IPI with no effects.

To shutdown the processors the operating system should only use the INIT IPI, STARTUP IPIs should never be used once the processors are running.

The following pseudo-code shows the generic algorithm for waking up Pentium processors, including 82489DX based systems, dual processor systems and multi-processor systems. The algorithm will work with future processors too.

```
BSP sends AP an INIT IPI
BSP DELAYs (10mSec)
If (APIC VERSION is not an 82489DX)
{
    BSP sends AP a STARTUP IPI
    BSP DELAYs (200uSec)
    BSP sends AP a STARTUP IPI
    BSP DELAYs (200uSec)
}
BSP verifies synchronization with executing AP
```

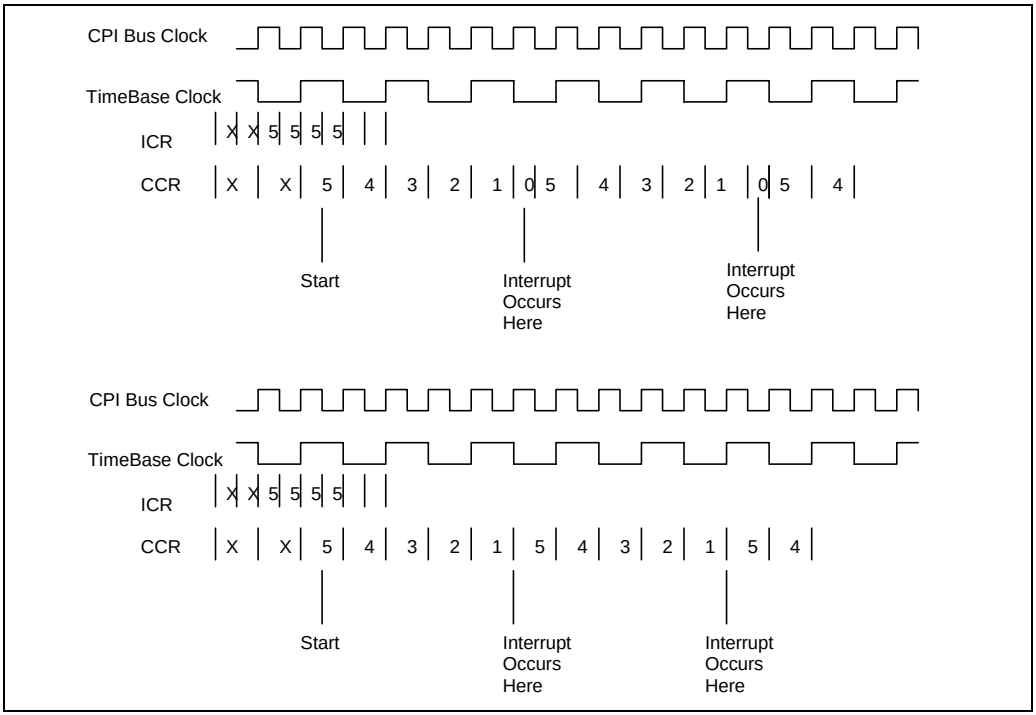
For additional information please refer to the *Intel Multiprocessor Specification*, Version 1.4 (Order Number 242016).

2. APIC Timer Use Clarification

The APIC Timer functions correctly, but there is one timer "tick" that is a different pulse width than the other timer "ticks". The countdown performs correctly regardless of the divisor that is programmed, each of these ticks is of the same pulse width, but the last tick is held for just one single timer clock regardless of the divisor programmed. This results in a slightly inaccurate timer. This last tick pulse width is shown in the top diagram. The lower diagram shows how the accuracy of the timer will be corrected in a future stepping. This phenomenon occurs when the timer is used as a single shot generator as well.

NOTE:

The CPU Bus clock in which the CCR is loaded from the ICR occurs one clock after the ICR is loaded.



3. PICCLK Reflection May Cause APIC Checksum Errors and Dropped IPIs

Many of the APIC errors that are listed in the erratum concern checksum errors on the APIC bus. This specification clarification is to address the elimination of checksum errors on the APIC bus. Doing so would reduce the error rate and would eliminate the possibility of dropping of Interprocessor Interrupts (IPI) due to multiple data errors on the same APIC message. Getting a single checksum error does not typically pose a problem, because the error will cause the APIC message will be resent, but if there is a high error rate then there is a possibility that the retries of the APIC messages may take up the bandwidth of the APIC bus some may be rescheduled or accidentally dropped. A system that performs in this manner has a fundamental design problem that needs to be corrected.

Most of the checksum errors observed are a result of the PICCLK not crossing the threshold cleanly, this can be tracked down to two possible issues: (1) PICCLK marginally meeting rise/fall time specification, and (2) reflections causing PICCLK to re-cross the threshold. Both of the problems are fairly easily solved, and a robust system design will typically show zero checksum errors in a 24 hour period during stress testing.

The current specification for the rise/fall time of the PICCLK signal is shown in the timing tables as t_{60e} and t_{60f} for all frequencies. This rise/fall time must be met to guarantee correct operation of the device. This rise/fall time should be verified at all receivers of the PICCLK signal. If a daisy chain type route is used with a large series termination resistor the rise/fall time at the devices near the driver end of the net are the most critical and should be checked. The high and low time specifications also need to be verified to meet the specification.

There is also a good chance that in a system using daisy chain route topologies that there will be reflections seen by receivers located close to the driver. It would be recommended to use a balanced star type route on clock signals like PICCLK to ensure there are no reflections that may re-cross any trip thresholds on the inputs to the CPU. The correct balanced route is based on both the length of the traces and the relative input capacitance loading presented by each device. It is also important to verify the selection of the correct series terminating resistors to dampen out any reflections on this line.

The values of the series resistances should be chosen using the following guidelines:

Single Receiver:

1. Driver and receiver on opposite ends of the trace.
2. R_driver + R_terminator = Zo.

Multiple Receivers:

1. Trace has 1 branch per receiver, branches are of equal equivalent capacitive loads.
2. Branch as close as possible to the Driver.
3. For single termination resistor (n branches):
   a. Place terminator as close to driver as possible.
   b. R_driver + R_terminator = Zo / n

4. For multiple termination resistors (n branches):
   a. Place terminators on each branch, as close to the branch point as possible.
   b. R_driver + R_terminator / n = Zo / n

Even though PICCLK is a lower frequency clock this clock is still critical and should be routed with care and reflections at each node should be eliminated. More detailed clock routing techniques are available in the AP-479 *Pentium™ Processor Clock Design* application note (Order Number 241574).

4. Boundary Scan RUNBIST Register Requires Initialization Prior to Use

It has been found that the Reset cell of the Boundary Scan register is not correctly initialized prior to use. There is a failing result reported from running the RUNBIST Command through the Boundary Scan circuitry.

The IEEE 1149.1-1990 specification states, “Where a test data register (other than the Boundary Scan register) must be initialized prior to execution of the self-test this must occur at the start of the self-test without any requirement to shift data into the component.”

To execute the TAP RUNBIST instruction:

1. Select “Sample/Preload” TAP instruction (XXXXXXXXX0001) and load the RESET BSCAN cell (cell #52) with ‘0’.
2. Shift in the “Runbist” TAP instruction move to and wait in the “run-test-idle” state for 2^{19} clocks.
3. Examine the pass/fail status by advancing to the “shift-dr” state to read the runbist register.

5. Only One SMI# Can Be Latched During SMM

Section 20.1.4.2 of Volume 3 of the *Pentium® Processor Family Developer's Manual* correctly states that only one SMI# can be latched by the CPU while it is in SMM (end of second paragraph). However, Section 5.1.50 of Volume 1 of the manual in the SMI# pin definition incorrectly implies by the use of the plural that more than one SMI# request may be held pending during SMM. Thus the following changes will be implemented in the next revision of the Manual:

Section 20.1.4.2 of Volume 3, next to last sentence in the second paragraph, will have the underlined phrase added: "The first SMI# interrupt request that occurs while the processor is in SMM **(i.e. after SMIACT# has been asserted)** is latched, and serviced when the processor exits SMM with the RSM instruction."

Section 5.1.50 of Volume 1: The second paragraph of the Signal Description, that refers to SMI# requests held pending during SMM, will be replaced with the entire second paragraph of Section 20.1.4.2 of Volume 3.

6. APIC 8-Bit Access

The following should be added to the *Pentium® Processor Family Developer's Manual*, Volume 3, Section 19.3.1.4. The APIC supports 32 bit sized, 32 bit aligned, read and write cycles to its registers. Therefore, all APIC registers should be accessed using 32-bit loads and stores. If a 32-bit APIC register is accessed with an 8 or 16 bit write cycle the result may be unpredictable. This implies that to modify a field, the entire 32-bit register should be read, the field modified, and the entire 32 bits written back.

7. LOCK Prefix Excludes APIC Memory Space

In the *Pentium® Processor Family Developer's Manual*, Volume 3, page 25-216, the LOCK prefix is described. A line should be added at the end of the description as follows: The LOCK prefix has no effect on instructions that address the APIC memory space. Therefore, LOCK# is not asserted.

8. SMI# Activation May Cause a Nested NMI Handling

In the *Pentium® Processor Family Developer's Manual*, Volume 3, Section 20.1.4.4, the following note should be added just before the last paragraph.

During NMI interrupt handling NMI interrupts are disabled. NMI interrupts are serviced and completed with IRET one at a time. When the processor enters SMM from the NMI interrupt handler, the processor saves the SMRAM State Save Map (e.g. contents of status registers) but does not save the attribute to keep NMI interrupts disabled. Potentially a NMI could be latched (while in SMM or upon exit) and serviced upon exit of SMM even though the previous NMI handler has still not completed. One or more NMI's could be nested in the first NMI handler. The interrupt handler should take this into consideration.

9. Code Breakpoints Set on Meaningless Prefixes Not Guaranteed to be Recognized

The following should be added to the *Pentium® Processor Family Developer's Manual*, Volume 3, Section 17.3.1.1 (Instruction-Breakpoint Fault).

Code breakpoints set on meaningless instruction prefixes (a prefix which has no logical meaning for that instruction, e.g. a segment override prefix on an instruction that does not access memory) are not guaranteed to be recognized.

Code breakpoints should be set on the instruction opcode, not on a meaningless prefix.

In the *Pentium® Processor Family Developer's Manual*, Volume 3, Sections 3-4 (Instruction Format) and 25.2 (Instruction Format), after "For each instruction one prefix may be used from each group. The effect of redundant prefixes (more than on prefix from a group) is undefined and may vary from processor to processor." The following should be added:

Some prefixes when attached to specific instructions have no logical meaning (e.g. a segment override prefix on an instruction that does not access memory). The effect of attaching meaningless prefixes to instructions is undefined and may vary from processor to processor.

10. Resume Flag Should Be Set by Software

The lead-in sentences and first bullet of Section 14.3.3 in the *Pentium® Processor Family Developer's Manual*, Volume 3 should be replaced with the following:

The RF (Resume Flag) in the EFLAGS register should be used during debugging to avoid servicing an instruction breakpoint fault multiple times. RF works as follows:

- The debug handler (interrupt #1) should set the RF bit in the EFLAGS image on the stack whenever it is servicing an instruction breakpoint fault (rather than a data breakpoint trap), and the breakpoint is being left in place. If this is not done, the CPU will return to execute the instruction, fault on the breakpoint again to interrupt #1, and so on.

The following should be added as fifth and sixth bullets:

- If a fault type breakpoint coincides with another fault (the instruction accesses a not present page, violates a general protection rule, etc.) one spurious repetition of the breakpoint will occur after the second fault is handled, even though the debug handler sets RF. As an optional debugging convenience, to avoid this occasional confusion, all interrupt handlers that could interact during debugging in this way can be modified by having them also set the RF bit in the EFLAGS image on their stack.
- The CPU, in branching to fault handlers under some circumstances, will set the RF bit in the EFLAGS image on the stack by hardware action. Exactly when the CPU does this is implementation specific and should not be relied upon by software. No problem is caused by setting this bit again if it is already set.

11. Data Breakpoints on INS Delayed One Iteration

The *Pentium® Processor Family Developer's Manual,* Volume 3, last paragraph and sentence of Section 17.3.1.2 states, "Repeated INS and OUTS instructions generate a memory breakpoint debug exception trap after the iteration in which the memory address breakpoint location is accessed."

The sentence should read, "Repeated OUTS instructions generate a memory breakpoint debug exception trap after the iteration in which the memory address breakpoint location is accessed. Repeated INS instructions generate the memory breakpoint debug exception trap one iteration later".

12. When L1 Cache Disabled, Inquire Cycles are Blocked

The last line in Table 18-2 in the *Pentium® Processor Family Developer's Manual,* Volume 3 presently reads "Invalidation is inhibited". This is part of the description of L1 cache behavior when it is "disabled" by setting CR0 bits CD = NW = 1. This line will be clarified to read "Inquire cycles (triggered by EADS# active) and resulting invalidation and any APCHK# assertions are inhibited."

13. Serializing Operation Required When One CPU Modifies Another CPU's Code

A new subsection, 19.2.1, will be added to the *Pentium® Processor Family Developer's Manual,* Volume 3, titled *Processor Modifying Another Processor's Code***,** and it will be referenced in the current subsection 18.2.3 on self modifying code.

A particular problem in memory access ordering occurs in a multiprocessing system if one processor (CPU1) modifies the code of another (CPU2). This obviously requires a semaphore check by CPU2 before executing in the area being modified, to assure that CPU1 is finished with the changes before CPU2 begins executing the changed code. In addition, it is necessary for CPU2 to execute a serializing operation after the semaphore allows access but before the modified code is executed. This is needed because the external snoops into CPU2 caused by the code modification by CPU1 will invalidate any matching lines in CPU2's code cache, but not in its prefetch buffers or execution pipeline. Note that this is different from the situation described in Section 18.2.3 on self-modifying code. When the CPU modifies its own code, the prefetch buffers and pipeline as well as the code cache are checked and invalidated if necessary.

14. For Correct Translations, the TLB Should be Flushed After the PSE Bit in CR4 Is Set

Memory mapping tables may be changed by setting the page size extension bit in CR4 (bit 4). However if the TLB is not flushed after the CR4.PSE bit is set, it may provide an erroneous 4 Kbyte page translation rather than a new 4 Mbyte page translation, or the other way around. Therefore for correct translations, the TLB should be flushed by writing to CR3 after the CR4.PSE bit is set.

This will be added to the *Pentium® Processor Family Developer's Manual,* Volume 3, Sections 10.1.3 and 11.3.5.

15. When APIC Enabled, its 4K Block Should Not be Used in Regular Memory

When the local APIC is enabled, it uses a 4 Kbyte memory mapped address block starting at 0FEE00000H for its control and status registers. Obviously one can't use the 4K block at 0FEE00000H in regular memory for data, because reads and writes would always go to the APIC registers instead. Not obviously, code placed in this location in memory usually is fetched correctly, because the bus unit normally distinguishes code fetches from APIC reads and puts the code fetches on the external bus. Nonetheless, this 4K block should not be used for code either, because in a case when the code fetch is backed off, the bus unit directs the recovered code fetch cycle to the APIC, resulting in interrupt 6, or unpredictable execution.

The following NOTE will be added as the last text in Section 19.3.1.4 in the *Pentium® Processor Family Developer's Manual,* Volume 3: "When the APIC is enabled, the 4K page in regular memory that overlays the 4K block assigned to the APIC should not be used, for either code or data."

16. Extra Code Break Can Occur on I/O or HLT Instruction if SMI Coincides

If a code breakpoint is set on an I/O instruction, as usual the breakpoint will be taken before the I/O instruction is executed. If the I/O instruction is also used as part of an I/O restart protocol, I/O restart is enabled, and executing the instruction triggers SMI, RSM from the SMI handler will return to the start of the I/O instruction, and the code breakpoint will be taken again before the I/O instruction is executed a second time.

Similarly, if a code breakpoint is set on an HLT instruction, the breakpoint will be taken before the processor enters the HLT state. If SMI occurs during this state, and the SMI handler chooses to RSM to the HLT instruction (the usual choice, for SMI to be transparent), the code breakpoint will be taken again before the HLT state is re-entered. In this case, other problems can occur, because an internal HLT flag remains set incorrectly. These problems are documented in Erratum # 55, case 2.

This information will be added to the end of Section 17.3.1.1, on "Instruction-Breakpoint Faults," in the *Pentium® Processor Family Developer's Manual,* Volume 3.

17. LRU May Be Updated for Non-cacheable Cycles

The following will be added to the *Pentium® Processor Family Developer's Manual*, Volume 3, page 18-7:

Memory reads may update the LRU bits in the Pentium processor with MMX technology even if the cycle is non-cacheable. The LRU replacement mechanism is implementation specific and may vary between processors.

18. FYL2XP1 Does Not Generate Exceptions for X Out of Range

The FYL2XP1 instruction is intended to be used only for taking the log of numbers very close to one, to provide improved accuracy. For X values outside of the FYL2XP1 instruction's valid range, the FYL2X instruction should be used instead. The present documentation of what happens when X is outside of the FYL2XP1 instruction's valid range is inconsistent. For FYL2XP1, out of range behavior will be replaced by "If the ST operand is outside of its acceptable range, the result is undefined, and software should not rely on an exception being generated. Under some circumstances exceptions may be generated when ST is out of range, but this behavior is implementation specific and not guaranteed." The information on pages 7-15 and 25-161 of the *Pentium® Processor Family Developer's Manual,* Volume *3* will be clarified.

19. Enabling NMI Inside SMM

Page 20-11 of the *Pentium® Processor Family Developer's Manual* Volume 3 states "Although NMI requests are blocked when the CPU enters SMM, they may be enabled through software by invoking a dummy interrupt and vectoring to an Interrupt Service Routine." This will be changed to: "Although NMI requests are blocked when the CPU enters SMM, they may be enabled by first enabling interrupts through INTR by setting the IF flag, and then by triggering INTR. Also, for the Pentium processor, exceptions that invoke a trap or fault handler will enable NMI inside of SMM. This behavior of exceptions enabling NMI within SMM is not part of the Intel Architecture, and is implementation specific".

20. BF[1:0] Must Not Change Values While RESET is Active

Table 4-3 and page 2-49 of the *Pentium® Processor Family Developer's Manual* states that BF[1:0] must not change values while RESET is active. Page 5-18 of the *Pentium® Processor Family Developer's Manual* also states that BF[1:0] must meet a 1 mS setup time to the falling edge of RESET. Since RESET has to be active for at least 1ms, the setup time spec of 1mS is a subset of the specification in Table 4-3 and will be removed. t43a (BF[1:0] 1 mS setup time to the falling edge of RESET) will also be removed from Tables 7-8, 7-10, 7-12 and page 2-49.

The following will also be added to the "When Sampled/Driven" section on page 5-18:

Additionally, BF[1:0] must not change values while RESET is active.

The following will be added to the end of the first paragraph on page 5-17 and to note 22 on page 7-27:

In order to override the internal defaults and guarantee that the BF[1:0] inputs remain stable while RESET is active, these pins should be strapped directly to or through a pullup/pulldown resistor to Vcc_3 or ground. Driving these pins with active logic is not recommended unless stability during RESET can be guaranteed.

On pages 3-1 and 5-80, the sentence starting with "During power up, RESET must be asserted while V_{CC}..." will be modified as follows:

During power up, RESET should be asserted prior to or ramped simultaneously with the core voltage supply to the processor.

21. Active A20M# During SMM

Section 14.3.3. of the 1997 *Pentium® Processor Family Developer's Manual* describes two considerations when using the A20M# input and SMM when SMRAM is relocated above 1 Megabyte. The system designer must ensure that A20M# is de-asserted on entry into SMM. A20M# must be driven inactive before the first cycle of the SMM state save, and must be returned to its original level after the last cycle of the SMM state restore. This can be done by blocking the assertion of A20M# whenever SMIACT# is active.

The following will be added to the end of Section 14.3.3:

In addition to blocking the assertion of A20M# whenever SMIACT# is active, the system must also guarantee that A20M# is de-asserted at least one I/O clock prior to the assertion of SMIACT#. The processor may start the SMM state save as soon as SMIACT# is asserted. Processors faster than 200 MHz may not have enough time to recognize the de-assertion of A20M# before starting the SMM state save. As a result, this may cause the processor to start the first few cycles of the SMM state save with A20M# asserted. To avoid this, the system designer can use either of the following:

1. When relocating the SMRAM above 1 Megabyte, ensure that the SMRAM does not coincide with any odd megabyte addresses. (Note that systems which use A20M# and SMM but do not relocate SMRAM above 1 Megabyte are not affected.)
2. Use external logic to prevent the assertion of SMI to the processor until A20M# is de-asserted (and guarantee that A20M# remains de-asserted while in SMM).

Note that the A20M# input must also meet setup and hold times in order to be recognized in a specific clock.

22. POP[ESP] with 16-bit Stack Size

In the *Pentium® Pro Family Developer's Manual, Volume 2: Programmer's Reference Manual* and the *Intel Architecture Software Developer's Manual, Volume 2: Instruction Set Reference*, the section regarding "POP–Pop a Value from the Stack", the following note is incomplete:

"If the ESP register is used as a base register for addressing a destination operand in memory, the POP instruction computes the effective address of the operand after it increments the ESP register."

It should read as follows:

"If the ESP register is used as a base register for addressing a destination operand in memory, the POP instruction computes the effective address of the operand after it increments the ESP register. In the case of a 16-bit stack where ESP wraps to 0h as a result of the POP instruction, the resulting location of the memory write is processor family specific."

In Section 15.12.1. of the *Pentium® Pro Family Developer's Manual, Volume 3: Operating System Writer's Guide* and Section 17.23.1. of the *Intel Architecture Software Developer's Manual, Volume 3: System Programming Guide*, add a new section:

A POP-to-memory instruction, which uses the stack pointer (ESP) as a base register.

For a POP-to-memory instruction that meets the following conditions:

1. The stack segment size is 16-bit,
2. Any 32-bit addressing form with the SIB byte specifying ESP as the base register, and
3. The initial stack pointer is FFFCh(32-bit operand) or FFFEh (16-bit operand) and will wrap around to 0h as a result of the POP operation,

The result of the memory write is processor family specific. For example, in Pentium II and Pentium Pro processors, the result of the memory write is to SS:0h plus any scaled index and displacement. In Pentium and Intel486 processors, the result of the memory write may be either a stack fault (real mode or protected mode with a stack segment size of 64 Kbytes), or write to SS:10000h plus any scaled index and displacement (protected mode and stack segment size exceeds 64 Kbytes).

DOCUMENTATION CHANGES

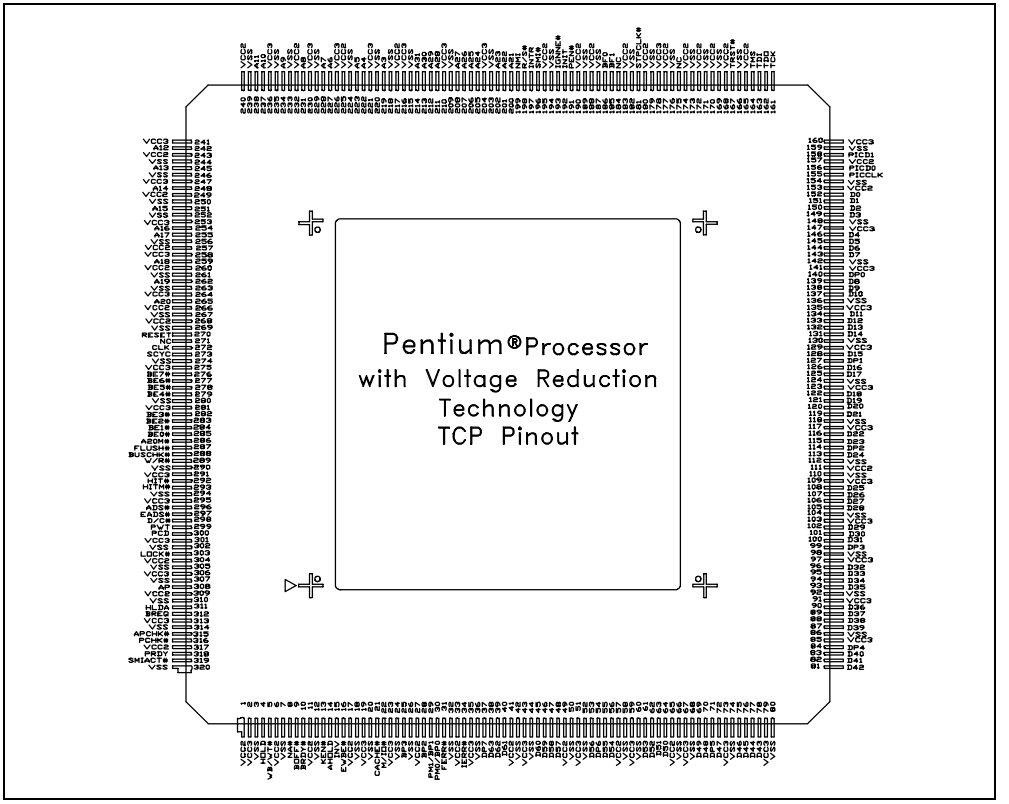
The Documentation Changes listed in this section apply to the *Pentium® Processor Family Developer's Manual*, Volumes 1 and 3. All Documentation Changes will be incorporated into a future version of the appropriate Pentium processor documentation.

1. JMP Cannot Do a Nested Task Switch, Volume 3, Page 13-12

In the *Pentium® Processor Family Developer's Manual*, Volume 3, Section 13.6, the sentence "When an interrupt, exception, jump, or call causes a task switch..." incorrectly includes the **jump** in the list of actions that can cause a **nested** task switch. The word "jump" will be removed from the sentence. The Table 13-2 correctly shows the effects of task switches via jumps vs. Task switches via CALL's or interrupts, on the NT flag and the Link field of the TSS.

2. Incorrect TCP Pinout Drawing

The TCP pinout drawing on page 8 of the *Pentium Processor with Voltage Reduction Technology* datasheet was inadvertently rotated. The correct orientation is shown below.



3. Interrupt Sampling Window, Volume 3, Page 23-39

In the *Pentium® Processor Family Developer's Manual*, Volume 3, Section 23.3.7 the first sentence of the second paragraph "The Pentium processor... asserts the FERR# pin." Should be replaced with the following:

The Pentium processor and the Intel486 processor implement the "No-Wait" Floating-Point instructions (See Section 6.3.7) in the DOS-Compatibility mode (CR0.NE = 0) in the following manner:

In the event of a pending unmasked numeric exception, the "No-Wait" class of instructions asserts the FERR# pin.

4. FSETPM Is Like NOP, Not Like FNOP

In the *Pentium® Processor Family Developer's Manual,* Volume 3, page 23-37 in the Section 23.3.4 on Instructions, the 80287 instruction FSETPM is described as being equivalent to an FNOP when executed in the Intel387 math coprocessor and the Intel486 and Pentium processors. In fact, FSETPM is treated as a NOP in these processors, as is correctly explained (along with the difference between FNOP and NOP) on the next page in Section 23.3.6. "FNOP" will be changed to "NOP" in the FSETPM description.

5. Errors in Three Tables of Special Descriptor Types

In the *Pentium® Processor Family Developer's Manual,* Volume 3 on page 25-199 and on page 25-222, in the descriptions of the **LAR** and **LSL** instructions respectively, tables are given of the special segment and gate descriptor types and names, with indication of which ones are valid with the given instruction. The same two pairs of descriptor types are interchanged in these two tables. Descriptor type 6 is the 16-bit interrupt gate, not trap gate, and type 7 is the 16-bit trap gate, not interrupt gate. Similarly, descriptor type 0Eh is the 32-bit interrupt gate, and 0Fh is the 32-bit trap gate. Table 12-1 gives a completely correct listing of the special descriptor types, but in the same chapter, Table 12-3 (page 12-22) incorrectly indicates that the 16-bit gates are not valid for the **LSL** instruction (this table *does* have the correct types for the interrupt and trap gates that it shows).

6. iCOMP® Index 2.0 Rating Correction

The 200 MHz Pentium processor with MMX technology has an iCOMP® index 2.0 Rating of 182. The table at the top of page i of the *Pentium® Processor Family Developer's Manual* lists the iCOMP Index 2.0 Rating of the 200 MHz Pentium processor with MMX technology incorrect as 183.

7. Default Setting for BF1-0 on a Pentium® Processor with MMX™ Technology

In the *Pentium® Processor Family Developer's Manual*, Section 5.1.10 page 5-18, the sentence" If BF[1:0] are left unconnected on the Pentium processor with MMX technology, the bus-to-core ratio defaults to 2/5." should be " If BF[1:0] are left unconnected on the Pentium processor with MMX technology, the bus-to-core ratio defaults to 1/2".

8. FPU Exceptions Cause Branch Trace Messages

In the *Pentium® Processor Family Developer's Manual*, Section 13.1.0 page 13-2, the sentence "Masked floating point exceptions and all other exceptions that invoke a trap or fault handler" should be changed to "certain Floating point exceptions (both masked and un-masked) and all other exceptions that invoke a trap or fault handler".

9. 1/3 Bus Fraction

In Section 3.6 of the *Mobile Pentium® Processor with MMX™ Technology* datasheet, Table 6, "Bus Frequency Selections," incorrectly states the 1/3 Bus Fraction. Table 6 is amended as follows:

Mobile Bus Frequency Selections

BF1	BF0	Bus/Core Ratio	Max Bus/Core Frequency (MHz)	Min Bus/Core Frequency (MHz)
0	1	1/3 (1)	N/A (1)	N/A (1)

NOTES:

1 This bus ratio is currently not supported in mobile Pentium® processor products.

10. Die Size Reduction

The B-Step Die size has been reduced to the following dimensions:

Die Length = **12.238** mm, Die Width = **10.579** mm

11. PICD0-1 External Capacitance Requirement

In the 1997 *Pentium® Processor Family Developer's Manual*, Section 7.4.3, Table 7-13, Note 28 states, "This assumes an external pullup resistor to V_{CC} and a lumped capacitive load. The pullup resistor must be between 300 ohms and 1k ohms, the capacitance must be between 20 pF and 240 pF, and the RC product must be between 6 ns and 36 ns. V_{OL} for PICD0-1 is 0.55 V."

This should be replaced with the following:

28. "This assumes an external pullup resistor to V_{CC} and a lumped capacitive load. The pullup resistor must be between 300 ohms and 1k ohms, the capacitance must be between 20 pF and 120 pF, and the RC product must be between 6 ns and 36 ns. V_{OL} for PICD0-1 is 0.55 V."

12. Invalid Arithmetic Operations and Masked Responses to Them Relative to FIST/FISTP Instruction

The *Pentium® Pro Family Developer's Manual, Volume 2: Programmer's Reference Manual*, Table 7-20 and the *Intel Architecture Software Developer's Manual, Volume 1*, Table 7-20 show "Invalid Arithmetic Operations and the Masked Responses to Them." The table entry corresponding to the FIST/FISTP condition is missing, and is shown below:

Condition	Masked Response
FIST/FISTP instruction when input operand <> MAXINT for destination operand size.	Return MAXNEG to destination operand.

Part II:

Specification Update for Pentium® OverDrive® Processors

GENERAL INFORMATION

This section covers the various Pentium OverDrive processors.

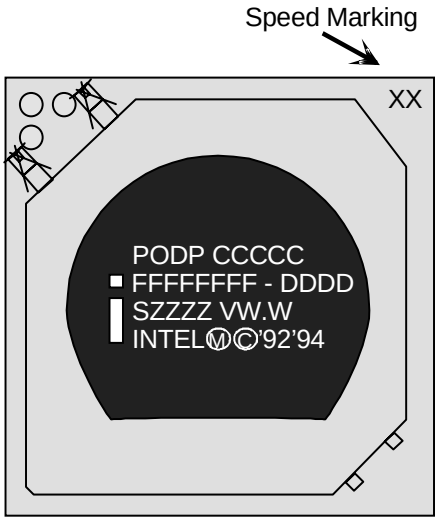
The 63- and 83-MHz Pentium OverDrive processors are Pentium processor technology upgrades for Intel486 processor-based systems. For more information on the 63- and 83-MHz Pentium OverDrive processors, please refer to the *Intel Pentium® OverDrive® Processor* datasheet (Order Number 290544).

The 120/133-MHz Pentium OverDrive processor is a Pentium processor technology upgrade for 60/66-MHz Pentium processor-based systems. The 125-, 150- and 166-MHz Pentium OverDrive processors are Pentium processor technology upgrades for 75-, 90- and 100-MHz Pentium processor-based systems. For more information on the Pentium OverDrive processors for Pentium processor based systems, please refer to the *Pentium® OverDrive® Processors for Pentium Processor-Based Systems* datasheet, (Order Number 290579).

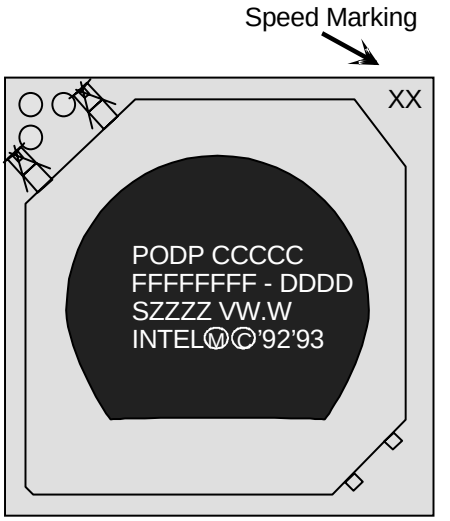
The 125/150/166/180- and 200-MHz Pentium OverDrive processors with MMX technology are upgrades for 75-, 90- and 100-MHz Pentium processor-based systems. In addition to normal increased performance from running faster than the original Pentium processor in the system, these OverDrive processors enable end-users to experience the benefits of MMX technology.

Top Markings

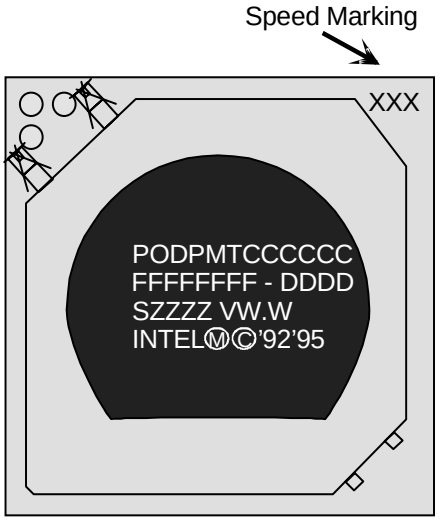
The Pentium OverDrive processor can be identified by the number on the base of the heat sink, under the integrated fan. To remove the fan, squeeze the retaining clips in the upper left corner of the chip and lift up. The figure below shows the laser mark found on the heatsink base of the processor. A marking is also used to indicate the speed of the part and is located in the upper right of the package.



63- and 83-MHz Pentium® OverDrive® Processors
for Intel486™ Processor-based Systems



120/133-, 125-, 150- and 166-MHz
Pentium® OverDrive® Processors



125/150/166/180- and 200-MHz Pentium®
OverDrive® Processors with MMX™ Technology

NOTES:

- XX or XXX = Core Speed (MHz).
- CCCCC or CCCCCC= Product Code.
- FFFFFFFF = FPO # (Test Lot Traceability #).
- DDDD = Serialization Code.
- SZZZZ = Spec number.
- VW.W = Version number.
- The FPO – Serial Number is unique for every Pentium® OverDrive® processors.
- The Version Number is used to easily identify major processor steppings: it applies to OverDrive processors only.

Basic Pentium® OverDrive® Processor Identification Information

CPUID					Mfg. Stepping[1]	Speed (MHz) Core / Bus	S-Spec	Version	Notes
Product Code	Type	Family	Model	Stepping					
PODP5V63	1	5	3	1	B1	63/25	SZ953	1.0	
PODP5V63	1	5	3	1	B2	63/25	SZ990	1.1	
PODP5V63	1	5	3	1	C0	63/25	SU013	1.0	
PODP5V83	1	5	3	2	C0	83/33	SU014	2.1	
PODP5V133	0	5	1	A	tA0	120/60,133/66	SU082	1.0	1, 2
PODP3V125	0	5	2	C	aC0	125/50	SU081	1.0	1, 3
PODP3V150	0	5	2	C	aC0	150/60	SU083	1.0	1, 3
PODP3V166	0	5	2	C	aC0	166/66	SU084	1.0	1, 3
PODPMT60X150	1	5	4	4	oxA3	125/50,150/60	SL24V	1.0	3, 4
PODPMT66X166	1	5	4	4	oxA3	166/66	SL24W	1.0	3, 4
PODPMT60X180	1	5	4	3	oxB1	180/60	SL2FE	2.0	3.4
PODPMT66X200	1	5	4	3	oxB1	200/66	SL2FF	2.0	3.4

NOTES:

- The Type corresponds to bits [13:12] of the EDX register after RESET, bits [13:12] of the EAX register after the CPUID instruction is executed.
- The Family corresponds to bits [11:8] of the EDX register after RESET, bits [11:8] of the EAX register after the CPUID instruction is executed.
- The Model corresponds to bits [7:4] of the EDX register after RESET, bits [7:4] of the EAX register after the CPUID instruction is executed.
- The Stepping corresponds to bits [3:0] of the EDX register after RESET, bits [3:0] of the EAX register after the CPUID instruction is execute.

1. Manufacturing steppings prefixed with a lower-case "t" refer to the 120/133-MHz Pentium® OverDrive® processor for 60/66-MHz Pentium processor-based systems. Steppings prefixed with a lower-case "a" refer to the 125-, 150- and 166-MHz Pentium OverDrive processors for 75-, 90- and 100-MHz Pentium processor-based systems. Steppings without a prefix refer to the 63/83-MHz Pentium OverDrive processors for Intel486™ processor-based system.
2. The V_{CC} operating voltage for these parts is 4.75 – 5.40.
3. The V_{CC} operating voltage for these parts is 3.135 – 3.6V.
4. Manufacturing steppings prefixed with a lower-case "ox" refer to the 125/150/166/180- and 200-MHz Pentium OverDrive processors with MMX technology for 75-, 90- and 100-MHz Pentium processor-based systems.

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to the listed Pentium OverDrive processor steppings. Intel intends to correct some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or specification changes as noted. Any items that are shaded are new for this revision of the document. This table uses the following notations:

CODES USED IN SUMMARY TABLE

X:	Erratum, Specification Change or Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
PP##:	Please refer to Part I: Specification Update for 75/90/100/120/133/150/166/ 200/233 MHz Pentium® Processors and Pentium Processors with MMX™ Technology.
Shaded:	This item is either new or modified from the previous version of the document.

No.	B1	B2	C0	tA0	aC0	oxA3	oxB1	Refer to	Plans	SPECIFICATION CHANGES
1	X	X	X						Doc	Clock low time (t_3) change
2		X	X						Doc	Removal of V_{CC} pin A4
3		X	X						Doc	Minimum operating temperature
4	X	X	X			X	X	PP1	Doc	IDT limit violation causes GP fault, not interrupt 8
5	X	X	X						Doc	Maximum I_{CC} values
6						X	X		Doc	Min case temperature under bias with fan attached
7	X	X	X	X	X	X	X	PP3	Doc	Redundant timing spec: t_{42d} for all bus frequencies
No.	**B1**	**B2**	**C0**	**tA0**	**aC0**	**oxA3**	**oxB1**	**Refer to**	**Plans**	**ERRATA**
1	X	X	X					PP1	Fixed	Branch trace messages during lock cycles
2	X	X	X					PP2	Fixed	Breakpoint or single-step may be missed for one instruction following STI
3	X	X	X					PP3	Fixed	I/O restart does not function during single-stepping or data breakpoint exceptions
4	X	X	X					PP4	Fixed	NMI or INIT in SMM with I/O restart during single-stepping
5	X	X	X					PP5	Fixed	SMI# and FLUSH# during shutdown
6	X	X				X	X		Fix	BIST disabled

No.	B1	B2	C0	tA0	aC0	oxA3	oxB1	Refer to	Plans	ERRATA (Cont'd)
7										Maximum I_{CC} usage (Refer to Spec Change 5)
8	X	X	X					PP6	Fixed	No shutdown after internal error
9	X	X	X					PP7	Fixed	FLUSH# with a breakpoint pending causes false DR6 values
10	Superseded by a Specification Change									STPCLK# deassertion not recognized for 5 CLKs after BRDY# returned
11	X	X	X	X	X	X	X	PP14	NoFix	NMI or INIT during HALT within SMM may cause large amount of bus activity
12	Superseded by a Specification Change									STPCLK# restrictions during EWBE#
13	X	X							Fixed	CLK required for UP# to be driven
14	X	X						PP18	Fixed	Multiple allocations into branch target buffer
15	X	X	X					PP24	Fixed	FLUSH#, INIT or Machine Check dropped due to floating-point exception
16	X	X	X					PP25	Fixed	Floating-point operations may clear Alignment Check bit
17	X	X	X					PP26	Fixed	CMPXCHG8B across page boundary may cause invalid opcode exception
18	X	X	X			X	X	PP27	NoFix	Single-step debug exception breaks out of HALT
19	X	X	X					PP28	Fixed	Branch trace message corruption
20	X	X	X					PP32	Fixed	EIP altered after specific FP operations followed by MOV Sreg. Reg
21	X	X	X	X	X			PP33	Fixed	WRMSR into illegal MSR does not generate GP fault
22	X	X	X					PP34	Fixed	Inconsistent data cache state from concurrent snoop and memory write
23	X	X	X	X	X			PP36	Fixed	Incorrect FIP after RESET
24	X								Fixed	Errors in least significant bit of an FMUL instruction result with specific operands
25	X	X	X	X	X	X	X	PP37	NoFix	Second assertion of FLUSH# not ignored
26	X	X	X					PP9	Fixed	SMIACT# premature assertion during replacement writeback cycle
27	X	X	X	X	X	X	X	PP38	NoFix	Segment limit violation by FPU operand may corrupt FPU state
28	X	X	X	X	X	X	X	PP39	NoFix	FP exception inside SMM with pending NMI hangs system
29	X	X	X					PP40	Fixed	Current in Stop Clock state exceeds specification
30	X	X	X	X	X	X	X	PP43	NoFix	Data breakpoint deviations

No.	B1	B2	C0	tA0	aC0	oxA3	oxB1	Refer to	Plans	ERRATA (Cont'd)
31	X	X	X	X	X	X	X	PP44	NoFix	Event monitor counting discrepancies
32	X	X	X	X	X	X	X	PP45	NoFix	VERR type instructions causing page fault task switch with T bit set may corrupt CS:EIP
33	X	X	X		X	X	X	PP48	NoFix	Matched but disabled data breakpoint can be lost by STPCLK# assertion
34	X	X	X		X	X	X	PP49	NoFix	STPCLK# ignored in SMM when INIT or NMI pending
35	X	X	X	X	X	X	X	PP51	NoFix	A fault causing a page fault can cause an instruction to execute twice
36	X	X	X	X	X	X	X	PP53	NoFix	FBSTP stores BCD operand incorrectly if address wrap & FPU error both occur
37	X	X	X	X	X	X	X	PP54	NoFix	V86 interrupt routine at illegal privilege level can cause spurious pushes to stack
38	X	X	X	X	X	X	X	PP55	NoFix	Corrupted HLT flag can cause skipped or incorrect instruction, or CPU hang
39	X	X	X	X	X	X	X	PP56	NoFix	Benign exceptions can erroneously cause double fault
40	X	X	X	X	X	X	X	PP57	NoFix	Double fault counter may not increment correctly
41	X	X	X	X	X	X	X	PP59	NoFix	Short form of mov EAX/ AX/ AL may not pair
42	X	X	X	X	X	X	X	PP60	NoFix	Turning off paging may result in prefetch to random location
43	X	X	X	X	X	X	X	PP61	NoFix	STPCLK#, FLUSH# or SMI# after STI
44	X	X	X		X	X	X	PP62	NoFix	REP string instruction not interruptable by STPCLK#
45	X	X	X	X	X	X	X	PP63	NoFix	Single step may not be reported on first instruction after FLUSH#
46	X	X	X	X	X	X	X	PP66	NoFix	STPCLK# on RSM to HLT causes non-standard behavior
47				X	X			PP15	Fixed	RUNBIST restrictions when run through boundary scan circuitry
48				X	X	X	X	PP46	NoFix	BUSCHK# interrupt has wrong priority
49					X			PP50	Fixed	STPCLK# pullup not engaged at RESET
50				X	X	X	X	PP52	NoFix	Machine check exception pending, then HLT, can cause skipped or incorrect instruction, or CPU hang
51				X		X	X	PP64	NoFix	Double fault may generate illegal bus cycle
52				X	X	X	X	PP65	NoFix	TRST# not asynchronous
53				X					NoFix	I/O Buffer Leakage

No.	B1	B2	C0	tA0	aC0	oxA3	oxB1	Refer to	Plans	ERRATA (Cont'd)
54				X					NoFix	Break in Boundary Scan Chain
55				X	X				NoFix	Incorrect type field in CPUID
56	X	X	X	X	X	X	X	PP67	NoFix	Code cache dump may cause wrong IERR#
57	X	X	X	X	X	X	X	PP68	NoFix	Asserting TRST# pin or issuing JTAG instructions does not exit TAP Hi-Z state
58				X					Fix	CLK input capacitance exceeds specification
59	X	X	X	X	X	X	X	PP69	NoFix	ADS# may be delayed after HLDA deassertion
60	X	X	X	X	X	X	X	PP70	NoFix	Stack underflow in IRET gives #GP, not #SS
61				X	X	X	X	PP71	NoFix	Performance monitoring pins PM[1:0] may count the events incorrectly
62	X	X	X	X	X	X	X	PP79	NoFix	Erroneous Debug Exception on POPF/IRET instructions with a GP Fault
63						X	X	PP73	NoFix	Branch trace message execution may cause system hang
64						X	X	PP74	Fix	Enabling RDPMC at in CR4 and also using SMM may cause shut down
65						X	X	PP75	Fix	Event monitor counting discrepancies (Fix)
66						X	X	PP76	NoFix	Event monitor counting discrepancies (NoFix)
67						X	X	PP77	Fix	INVD may leave valid entries in the cache due to snoop interaction
68						X	X	PP78	NoFix	TLB update is blocked after a specific sequence of events with a misaligned descriptor
69						X	X	PP80	NoFix	CR2 and CR4 content upon return from SMM
70	X	X	X	X	X	X	X	PP81	Fixed	Invalid operand with locked CMPXCHG8B instruction
71	X	X	X	X	X	X	X	PP82	NoFix	Event monitor counting discrepancy

No.	B1	B2	C0	tA0	aC0	oxA3	oxB1	Refer to	Plans	SPECIFICATION CLARIFICATIONS
1	X	X	X						Doc	CACHE#, KEN# and BLAST# Behavior
2	X	X	X						Doc	Behavior of writeback support pins in writethrough mode
3	X	X	X						Doc	HITM# deassertion behavior
4	X	X	X	X	X	X	X	PP5	Doc	Only one SMI# can be latched during SMM
5	X	X	X	X	X	X	X	PP8	Doc	SMI# activation may cause a nested NMI handling
6	X	X	X	X	X	X	X	PP9	Doc	Code breakpoints set on meaningless prefixes not guaranteed to be recognized

No.	B1	B2	C0	tA0	aC0	oxA3	oxB1	Refer to	Plans	SPECIFICATION CLARIFICATIONS (Cont'd)
7	X	X	X	X	X	X	X	PP10	Doc	Resume flag should be set by software
8	X	X	X	X	X	X	X	PP11	Doc	Data breakpoints on INS delayed one iteration
9	X	X	X	X	X	X	X	PP12	Doc	When L1 cache disabled, inquire cycles are blocked
10	X	X	X	X	X	X	X	PP14	Doc	For correct translations, the TLB should be flushed after the PSE bit in CR4 is set
11	X	X	X	X	X	X	X	PP16	Doc	Extra code break can occur on I/O or HLT instruction if SMI coincides
12	X	X	X	X	X	X	X	PP18	Doc	FYL2XP1 does not generate exceptions for X out of range
13	X	X	X	X	X	X	X	PP19	Doc	Enabling NMI inside SMM
14						X			Doc	CLK Undershoot
15						X	X	PP17	Doc	LRU may be updated for non-cacheable cycles
16	X	X	X	X	X	X	X	PP21	Doc	Active A20M# during SMM
17	X	X	X	X	X	X	X	PP22	Doc	POP[ESP] with 16-bit stack size

No.	B1	B2	C0	tA0	aC0	oxA3	oxB1	Refer to	Plans	DOCUMENTATION CHANGES
1	X	X	X	X	X	X	X	PP1	Doc	JMP cannot do a nested task switch, Volume 3, page 13-12
2	X	X	X	X	X	X	X	PP3	Doc	Interrupt sampling window, Volume 3, page 23-39
3	X	X	X	X	X	X	X	PP4	Doc	FSETPM is like NOP, not like FNOP
4	X	X	X	X	X	X	X	PP5	Doc	Errors in 3 tables of special descriptor types
5	X	X	X	X	X	X	X	PP8	Doc	FPU exceptions cause branch trace messages
6	X	X	X	X	X	X	X	PP12	Doc	Invalid arithmetic operations and masked responses to them relative to FIST/FISTP instruction

SPECIFICATION CHANGES

The Specification Changes listed in this section apply to the Pentium OverDrive processor datasheets. All Specification Changes will be incorporated into future versions of the appropriate document(s).

1. Clock Low Time (t_3) Change

The AC timings for the Pentium OverDrive processor CLK low time have been changed to better meet the needs of the installed base of Intel486 processor-based systems. The change to the Pentium OverDrive processor CLK low time specification applies to the Pentium OverDrive processor only, and does not affect any other clock specifications, such as CLK High time or rise/fall specifications.

NEW SPECIFICATIONS

Pentium® OverDrive® Processor 25 MHz AC Characteristics
(V_{CC} = 5V ±5%; T_A(IN) = 10°C T_O +55°C; C_L = 50PF unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
t_3	CLK Low Time	11		ns

Pentium® OverDrive® Processor 33 MHz AC Characteristics
(V_{CC} = 5V ±5%; T_A(IN) = 10°C T_O +55°C; C_L = 50PF unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
t_3	CLK Low Time	8		ns

2. Removal of V_{CC} Pin A4

To resolve compatibility concerns with a limited number of incorrectly designed motherboards, pin A4 (V_{CC}) will be removed from the Pentium OverDrive processors and will no longer be present on the package. The removal of this V_{CC} pin will not adversely affect the operation of the processor due to the large number of V_{SS} and V_{CC} pins remaining in the outer row.

3. Minimum Operating Temperature

The specification for the minimum operating temperature of the Pentium OverDrive processors has been changed. All other temperature specifications, such as the absolute maximum ratings, remained unchanged. The new temperature specification is detailed in the table below:

$T_{A(IN)}$ Old Specification (°C)	$T_{A(IN)}$ New Specification (°C)
0 to +55	10 to +55

4. Refer to Summary Table of Changes

5. Maximum I_{CC} Values

The maximum current requirements originally estimated for the Pentium OverDrive processors were found to be slightly lower than the actual values. The new values are listed in the table below.

Old max	New max	Notes
1.9 A	2.2 A	63/25 MHz
2.6 A	2.8 A	83/33 MHz

6. Min Case Temperature Under Bias with Fan Attached

The specification for the minimum case temperature under bias with the fan attached for the Pentium OverDrive processors with MMX technology has been changed from 0°C to 10°C.

Pentium® OverDrive® Processors with MMX™ Technology with Fan Attached

Parameter	Min	Max	Unit
Case Temperature Under Bias	10		°C

7. Refer to Summary Table of Changes

ERRATA

1 – 5. Refer to Summary Table of Changes

6. BIST Disabled

PROBLEM: The current production stepping of the Pentium OverDrive processor has disabled the Built-In Self Test (BIST) functionality.

IMPLICATION: If BIST is performed (AHOLD high at the falling edge of RESET), the processor will not actually perform the BIST, but will return a value of 'zero' in the EAX register to indicate that all tests have passed.

WORKAROUND: None required.

STATUS: This erratum has been fixed in the C-0 stepping.

7. Maximum I_{CC} Usage (Refer to Spec. Change 5.)

8 – 12. Refer to Summary Table of Changes

13. CLK Required for UP# to be Driven

PROBLEM: The Upgrade Present (UP#) output pin is intended to be driven low after power-up to indicate that an upgrade processor is present in the system. The UP# pin on the Pentium OverDrive processor requires that the CLK input toggle while the system is starting to insure that RESET reaches the UP# circuitry. If CLK does not toggle, UP# may or may not be driven low, depending on the initial state of the UP# circuitry.

IMPLICATION: If an Intel486 processor system is dependent on having UP# driven low before driving the CLK input on the Pentium OverDrive processor, it may never boot since CLK may never be driven to the processor if UP# remains high. This is generally only a potential issue in systems with two processor sites, such as those with a surface-mount Intel486 processor and a PGA upgrade processor site.

WORKAROUND: Most two site systems have the ability to disable the processor in the surface-mount location so that a different Intel486 (non-upgrade) processor may be used in the PGA socket location. If the system has a jumper or switch that is documented to specifically disable the surface mount processor (or the original processor in a two socket system), use it to disable the second processor and thereby route the CLK signal to the upgrade PGA socket location.

STATUS: This erratum has been fixed in the C-0 stepping.

14. Multiple Allocations Into Branch Target Buffer

PROBLEM: Please refer to Part II of this document. This errata entry for the Pentium OverDrive processor has been added for clarification of the issue as it applies to this processor specifically.

IMPLICATION: Please refer to Erratum 18 of Part II of this document.

WORKAROUND: Please refer to Erratum 18 of Part II of this document.

STATUS: This erratum has been fixed in the C-0 stepping. Although this erratum has been recreated in proprietary Intel test systems, it has not been observed on a Pentium OverDrive processor in an actual personal computer system.

15 – 23. Refer to Summary Table of Changes

24. Errors in Least Significant Bit of an FMUL Instruction Result with Specific Operands

PROBLEM: The result of multiplying two operands, one of which is typically close to infinity or close to the smallest representable normal number, may be incorrect in the Least Significant Bit (LSB) and may result in flags that are incorrectly set. This problem is limited to a small percentage of the first production units of the 63MHz Pentium OverDrive processor (specification number SZ953, Ver#: 1.0).

All precisions: single, double and extended are affected. All rounding modes: nearest, up, down and chop are affected. Only specific operand pairs result in errors.

IMPLICATION: Only a fraction of the Pentium OverDrive processors may produce errors in the least significant bit of the result when using the FMUL instruction with one of these specific input operands. Any of the exception flag bits in the FPU status word may also be incorrect.

WORKAROUND: None identified. Intel includes software with the Pentium OverDrive processor that can detect this erratum. Please see the following Status paragraph.

STATUS: The Pentium OverDrive processors currently in production are free from this defect. Only a fraction of the first production units at 63-MHz marked SZ953 may exhibit the defect. Owners of Pentium OverDrive processors should run the diagnostics on the disk supplied with the Pentium OverDrive processor. The diagnostic program tests the processor and will notify the user of pass/fail information. Should the processor fail, the diagnostic program will report that “The Floating Point Conformance Test has Failed” and will wait for a keystroke before continuing. Owners of the Pentium OverDrive processor should contact the Intel support line if there are any questions.

25. Second Assertion of FLUSH# Not Ignored

PROBLEM: Please refer to Part II of this document. This errata entry for the Pentium OverDrive processors has been added for clarification of the issue as it applies to these OverDrive processors specifically.

IMPLICATION: This erratum applies to the Pentium OverDrive processor in Enhanced (WB) bus mode only. Standard bus mode (WT) is not affected. Please refer to Part II of this document for more information.

WORKAROUND: Please refer to Part II of this document.

STATUS: For the steppings affected, please see the Summary of Changes table at the beginning of this section.

26 – 28. Refer to Summary Table of Changes

29. Current in Stop Clock State Exceeds Specification

PROBLEM: Please refer to Part II of this document. This errata entry for the Pentium OverDrive processors has been added for clarification of the issue as it applies to these OverDrive processors specifically.

IMPLICATION: Please refer to Part II of this document for more information.

WORKAROUND: None Identified. The workaround as stated in Part II of this document is not valid for the Pentium OverDrive processor since the boundary scan pins are not available on production units.

STATUS: For the steppings affected, please see the Summary of Changes table at the beginning of this section.

30 – 38. Refer to Summary Table of Changes

39. Benign Exceptions Can Erroneously Cause Double Fault

PROBLEM: Please refer to Part II of this document. This errata entry for the Pentium OverDrive processors has been added for clarification of the issue as it applies to these OverDrive processors specifically.

IMPLICATION: This erratum applies to the Pentium OverDrive processor in Case 1 only. Case 2 “A machine check exception (INT 18) is generated” does not apply. Please refer to Part II of this document for more information.

WORKAROUND: Please refer to Part II of this document

STATUS: For the steppings affected, please see the Summary of Changes table at the beginning of this section.

40 – 42. Refer to Summary Table of Changes

43. STPCLK# or FLUSH# After STI

PROBLEM: Please refer to Part II of this document. This errata entry for the 63 and 83-MHz Pentium OverDrive processors has been added for clarification of the issue as it applies to these OverDrive processors specifically.

IMPLICATION: In the case of “FLUSH# After STI,” this erratum applies to the Pentium OverDrive processor in Enhanced (WB) bus mode only. Standard bus mode (WT) is not affected. Please refer to Part II of this document for more information.

WORKAROUND: Please refer to Part II of this document.

STATUS: For the steppings affected, please see the Summary of Changes table at the beginning of this section.

44. Refer to Summary Table of Changes

45. Single Step May Not be Reported on First Instruction After FLUSH#

PROBLEM: Please refer to Part II of this document. This errata entry for the 63 and 83-MHz Pentium OverDrive processors has been added for clarification of the issue as it applies to these OverDrive processors specifically.

IMPLICATION: This erratum applies to the Pentium OverDrive processor in Enhanced (WB) bus mode only. Standard bus mode (WT) is not affected. Please refer to Part II of this document for more information.

WORKAROUND: Please refer to Part II of this document.

STATUS: For the steppings affected, please see the Summary of Changes table at the beginning of this section.

46 – 52. Refer to Summary Table of Changes

53. I/O Buffer Leakage

PROBLEM: When an I/O pin is driven high by the Pentium OverDrive processor and then tri-stated, the output is still weakly driven high until the line is driven low by either the processor or another source.

IMPLICATION: If a weak pull-down (greater than 1kΩ) is used on a signal line and the value of the line is expected at a given time after being tri-stated by the processor, the incorrect value can be read.

WORKAROUND: None identified at this time.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

54. Break in Boundary Scan Chain

PROBLEM: The boundary scan problem can most easily be described as a broken link in the boundary scan chain. The effects of this broken link on the output testing are minimal, since the majority of the chain is before the break. This part of the chain can still be filled, and the data sent to the output pins. However, any pins after the break will not be able to send out the correct output data. The effects of this broken link on input testing are more drastic. Only the last four cells worth of data can be collected at the boundary scan output. With respect to operating with other devices, the boundary scan chain will not not be able to shift data through the processor to other devices.

IMPLICATION: This problem only affects operation of the component while in boundary scan mode.

WORKAROUND: The bypass mode for the processor does still work, so other devices in the boundary scan chain can be accessed using this method.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

55. Incorrect Type Field in CPUID

PROBLEM: Execution of the CPUID with a ‘1’ in the EAX register does not return a value of ‘01’ (OverDrive processor installed) in the type field (Bits 13.12). Instead it returns a ‘00’ (Primary Processor) in the type field.

IMPLICATION: BIOS or application software that relies on the type field to be '01' when an OverDrive processor is installed, may function improperly.

WORKAROUND: BIOS or application software should be written to function properly when '00' is returned in the type field and an OverDrive processor is present in the system.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

56. Refer to Summary Table of Changes

57. Asserting TRST# Pin or Issuing JTAG Instructions Does not Exit TAP Hi-Z State

PROBLEM: Please refer to Part II of this document. This errata entry for the Pentium OverDrive processor has been added for clarification of the issue as it applies to the 63- and 83-MHz Pentium OverDrive processors for Intel486 processor-based systems specifically.

IMPLICATION: This erratum applies to the 63- and 83-MHz Pentium OverDrive processors only when issuing JTAG instructions. The 63- and 83-MHz Pentium OverDrive processors do not have a TRST# pin. Please refer to Part II of this document for more information.

WORKAROUND: Please refer to Part II of this document.

STATUS: For the steppings affected, please see the Summary of Changes table at the beginning of this section.

58. CLK Input Capacitance Exceeds Specification

PROBLEM: The input capacitance on the CLK pin is higher than the specification due to the ceramic package design. The specification for the 120/133-MHz Pentium OverDrive processor's input capacitance iS 8pF whereas the measured value on the clock pin is 13pF. This added capacitance may cause excessive ringback on the CLK signal.

IMPLICATION: If the CLK signal going to the processor is also used as an input to another device, the ringback can cause the other device to detect an incorrect rising edge on CLK. This can cause the system to not boot or to hang. Only a small percentage of systems appear to be affected by the higher capacitance.

The only confirmed issue is related to some boards with an Intel 82430LX chipset. The 82434LX PCMC's HCLKA output is used to drive the clock to the processor. This clock signal may also be used as a feedback to the chipset to minimize the clock skew between the CPU and PCMC. The capacitance difference will create a reflection on the clock signal that, if sufficient in amplitude, will cause the PCMC to detect a false clock edge and the bus state machines to get out of synchronization causing the system to lock up. This condition is dependent upon not only the capacitance difference but also the physical board design and voltage threshold of the chipset.

WORKAROUND: If an end user experiences any problems, they should remove the Pentium OverDrive processor and install the original 60/66-MHz Pentium processor. The end user should then contact the Intel Customer Support Hotline listed on the OverDrive processor retail box for assistance.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

59 – 71. Refer to Summary Table of Changes

SPECIFICATION CLARIFICATIONS

1. CACHE#, KEN# and BLAST# Behavior

If CACHE# is driven LOW during a read cycle, this implies that the processor intends to perform a linefill; however, this does not imply that BLAST# will be driven HIGH. As with the IntelDX2 (processor, KEN# controls the cacheability of data and can be used to refuse the linefill. If the processor requires only one transfer to get the required data, BLAST# will be driven LOW if KEN# is sampled HIGH.

2. Behavior of Writeback Support Pins in Writethrough Mode

Three new output pins are used to support the internal writeback cache of the Pentium OverDrive processor. These pins are HIT#, HITM# and CACHE#. The writeback mode of the processor can be enabled by driving the WB/WT# pin to the appropriate state during the falling edge of RESET. The clarification is as follows:

The three internal writeback support pins will be driven at all times regardless of the processor cache mode (enhanced (writeback) or standard (writethrough)). This implies that the HIT# and HITM# pins will always be driven HIGH in writethrough mode since there can be no writeback cycles. It also implies that in writethrough mode, the CACHE# pin will be toggled normally for reads and will be driven HIGH for all write cycles.

3. HITM# Deassertion Behavior

The HITM# pin is driven LOW in response to an external snoop that hits a modified line in the cache. It remains low until an appropriate action occurs (usually a writeback cycle) to maintain consistency with main memory. The clarification deals with the deassertion of HITM#.

Previously available documentation stated that HITM# will be driven inactive “after the last RDY#/BRDY# of the writeback cycle” and is “guaranteed to be deasserted before the next ADS#.” This means that HITM# can be deasserted anytime between these two points, and hardware should not assume that HITM# is deasserted on any specific CLK. It also implies that the system design should not depend on the Pentium OverDrive processor to deassert HITM# in the same clock the writeback Enhanced IntelDX2 processor.

4 – 13. Refer to Summary Table of Changes

14. CLK Undershoot

The maximum undershoot, undershoot threshold duration, and maximum ringback specifications for CLK are described below:

MAXIMUM UNDERSHOOT SPECIFICATION: The maximum undershoot of the CLK signal must not drop below 0.9V.

UNDERSHOOT THRESHOLD DURATION SPECIFICATION: The undershoot threshold duration is defined as the sum of all time during which the CLK signal is below –0.5V within a single clock period. The undershoot threshold duration must not exceed 20% of the period.

MAXIMUM RINGBACK SPECIFICATION: The maximum ringback of CLK associated with its low state (undershoot) must not exceed 0.8V as shown in Figure 14-1.

Refer to Table 14-1 for a summary of the clock overshoot and undershoot specifications for the Pentium OverDrive processor with MMX technology.

Table 14-1. Undershoot Specification Summary

Specification Name	Value	Units	Notes
Threshold Level	–0.5	V	1
Minimum Undershoot Level	–0.9	V	1
Maximum Threshold Duration	20% of clock period below threshold voltage	ns	1
Maximum Ringback	0.8	V	1

NOTES:

1. See Figure 14-1 and Figure 14-2.

CLOCK SIGNAL MEASUREMENT METHODOLOGY: The waveform of the clock signals should be measured at the bottom side of the processor pins using an oscilloscope with a 3 dB bandwidth of at least 20 MHz (100 MS/s digital sampling rate). There should be a short isolation ground lead attached to a processor pin on the bottom side of the board. An 1 Mohm probe with loading of less than 1 pF (e.g., Tektronics 6243 or Tektronics 6245) is recommended. The measurement should be taken at the CLK (AK18) pin and its nearest VSS pins (AM18).

MAXIMUM UNDERSHOOT AND MAXIMUM RINGBACK SPECIFICATIONS: The display should show continuous sampling (e.g., infinite persistence) of the waveform at 500 mV/div and 5 ns/div (for CLK) for a recommended duration of approximately five seconds. Adjust the vertical position to measure the maximum undershoot and associated ringback. There is no allowance for crossing the maximum undershoot or maximum ringback specifications.

UNDERSHOOT THRESHOLD DURATION SPECIFICATION: A snapshot of the clock signal should be taken at 500 mV/div and 500 pS/div (for CLK). Adjust the vertical position and horizontal offset position to view the threshold duration. The undershoot threshold duration is defined as the sum of all time during which the clock signal is below –0.5V within a single clock period. The undershoot threshold duration must not exceed 20% of the period.

This undershoot specifications are illustrated graphically in Figure 14-1 and Figure 14-2.

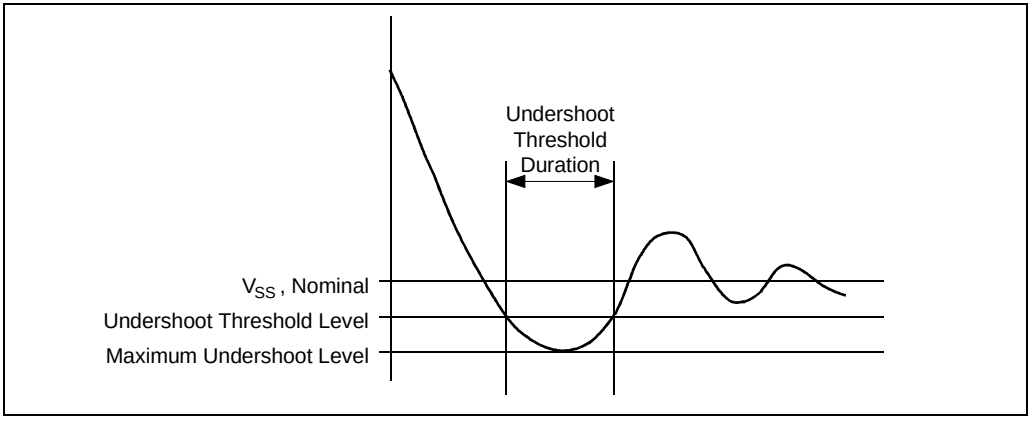


Figure14-1. Maximum Undershoot Level, Undershoot Threshold Level, and Undershoot Threshold Duration

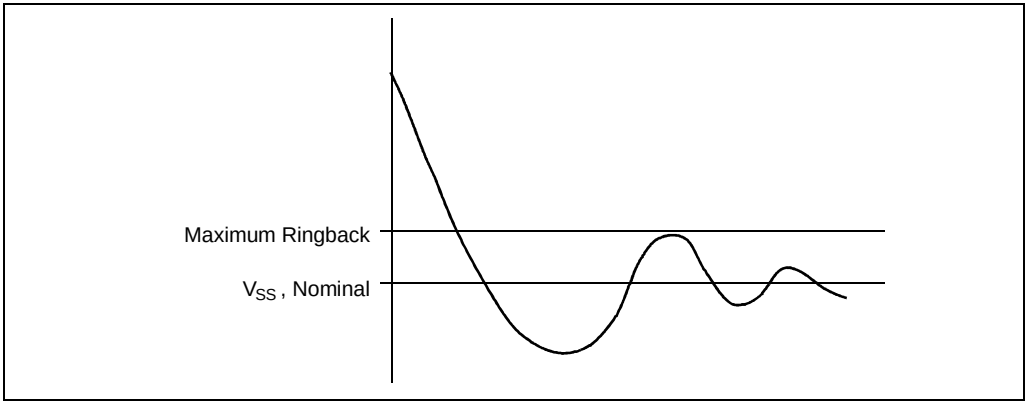


Figure 14-2. Maximum Ringback Associated with the Signal Low State

15 – 17. Refer to Summary Table of Changes

DOCUMENTATION CHANGES

The Documentation Changes listed in this section apply to the Pentium OverDrive processor datasheets. All Documentation Changes will be incorporated into the appropriate documentation.

1 – 6. Refer to Summary Table of Changes

Appendix A

Pentium® Processor Related Technical Collateral

PUBLIC DOCUMENTATION

Unless otherwise noted, the following documentation may be obtained by visiting Intel's website at http:\\www.intel.com or by contacting Intel's Literature Center at 1-800-879-4683 in the U.S. and Canada. In other geographies, please contact your local sales office.

Document Title	Order Number
Pentium® Processor Family Developer's Manual (1997)	241428
Intel Architecture Software Developer's Manual, Volume 1: Basic Architecture	243190
Intel Architecture Software Developer's Manual, Volume 2: Instruction Set Reference	243191
Pentium® Processor datasheet (75 MHz, 90 MHz, 100 MHz, 120 MHz, 133 MHz, 150 MHz, 166 MHz and 200 MHz)	241997
Pentium® Processor Specification Update	242480
MultiProcessor Specification	242016
Pentium® Processor Family Product Brief	241561
Pentium® Processor Performance Brief	241557
Pentium® Processor Technical Overview	241610
Intel MMX™ Technology Overview	243081
Intel Architecture MMX™ Technology Programmer's Reference Manual	243007
Intel Architecture MMX™ Technology Developer's Manual	243006
Intel MMX™ Technology at a Glance	243100
Pentium® Processor 60 and 66 MHz Specification Update	243326
AP-579: Pentium® Processor Flexible Motherboard Design Guidelines	243187
AP-479: Pentium® Processor Clock Design	241574
AP-480: Pentium® Processor Thermal Design Guidelines	241575
AP-485: Intel Processor Identification with the CPUID Instruction	241618
AP-500: Optimizations for Intel's 32-Bit Processors	241799
AP-577: An Introduction to PPGA Packaging	243103
AP-522: Implementation Guidelines for 3.3V Pentium® Processors with VRE Specifications	242687
AP-578: Software and Hardware Considerations in Handling FPU Exceptions	242415
Pentium® Processor 3.3V Clock Driver Specifications	Contact your local Intel/ Distributor Sales Office
Pentium® Processor 3.3V ASIC Interface Specification	Contact your local Intel/ Distributor Sales Office
Pentium® Processor 3.3V Pipeline BSRAM Specification	Contact your local Intel/ Distributor Sales Office

Document Title	Order Number
Pentium® Processor with MMX™ Technology datasheet	243185
Pentium® Processor with Voltage Reduction Technology datasheet	242557
Mobile Pentium® Processor with MMX™ Technology datasheet	243292
Pentium® Processor at iCOMP® index 815\100 MHz, Pentium Processor at iCOMP Index 735\90 MHz, Pentium Processor at iCOMP Index 610\75 MHz with Voltage Reduction Technology datasheet	242973
Mobile Pentium® Processor with MMX™ Technology on 0.25 Micron datasheet	243468