Overview of the Cyrix M2 Microprocessor

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Presentation Agenda

- Product Goals
- M2 Key Features
- Microarchitecture Overview
- L1 cache and TLB
- Performance
- Multimedia Enhancements
- Summary

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M2 Product Goals

- Highest performance desktop for Windows® 95 and Windows® NT in '97
- Acceleration of multimedia applications
- Provide flexible system cost/performance options
- Low cost - highly manufacturable
- Low power - mainstream mobile solution

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M2 Key Features

- High-performance superscalar native x86 core
  - Optimizations for 16-bit and 32-bit code
  - 2x faster than the 6x86 on 32-bit code
  - Enhanced cache, MMU, BTB
- 180 to 225 MHz operation
  - 75/187, 66/200, 75/225 initial offerings
  - 2:1, 2.5:1, 3:1, 3.5:1 core to bus clock ratio
- Pentium® Pro + MMX instruction set
- Standard 6x86 socket
  - 2.5 V core, 3.3 V bus interface
  - 6 M transistors
  - less than 200 sq. mm, .35u 5 layer metal CMOS

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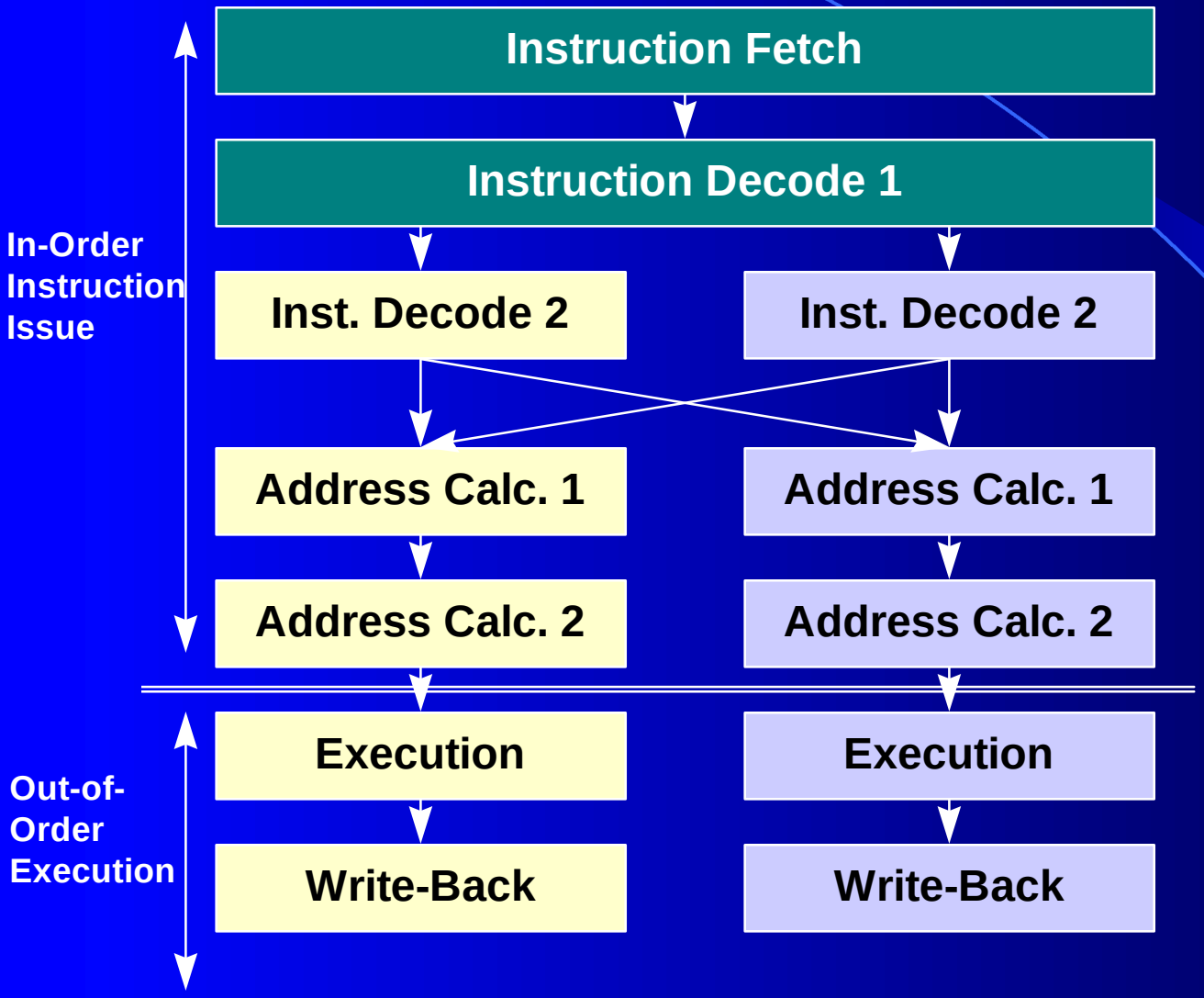
M2 Pipeline



- Fetches 16 bytes per clock.
- Branch Target Buffer and branch prediction.

- .Determines instruction length for up to 2 instructions per clock.

- Decodes 2 instructions per clock.
- Determines optimum pipe to be used for execution.

- Calculates 2 addresses per clock.
- Scoreboard checks and register renaming.

- TLB translation and cache access.
- Register file access.
- Segmentation and paging checks.

- Dual single cycle execution units.
- Multiplier/divider in X pipe only.
- FPU/MMX in X pipe only.

- Write to register/write buffers.
- Data immediately available to AC and EX stages.

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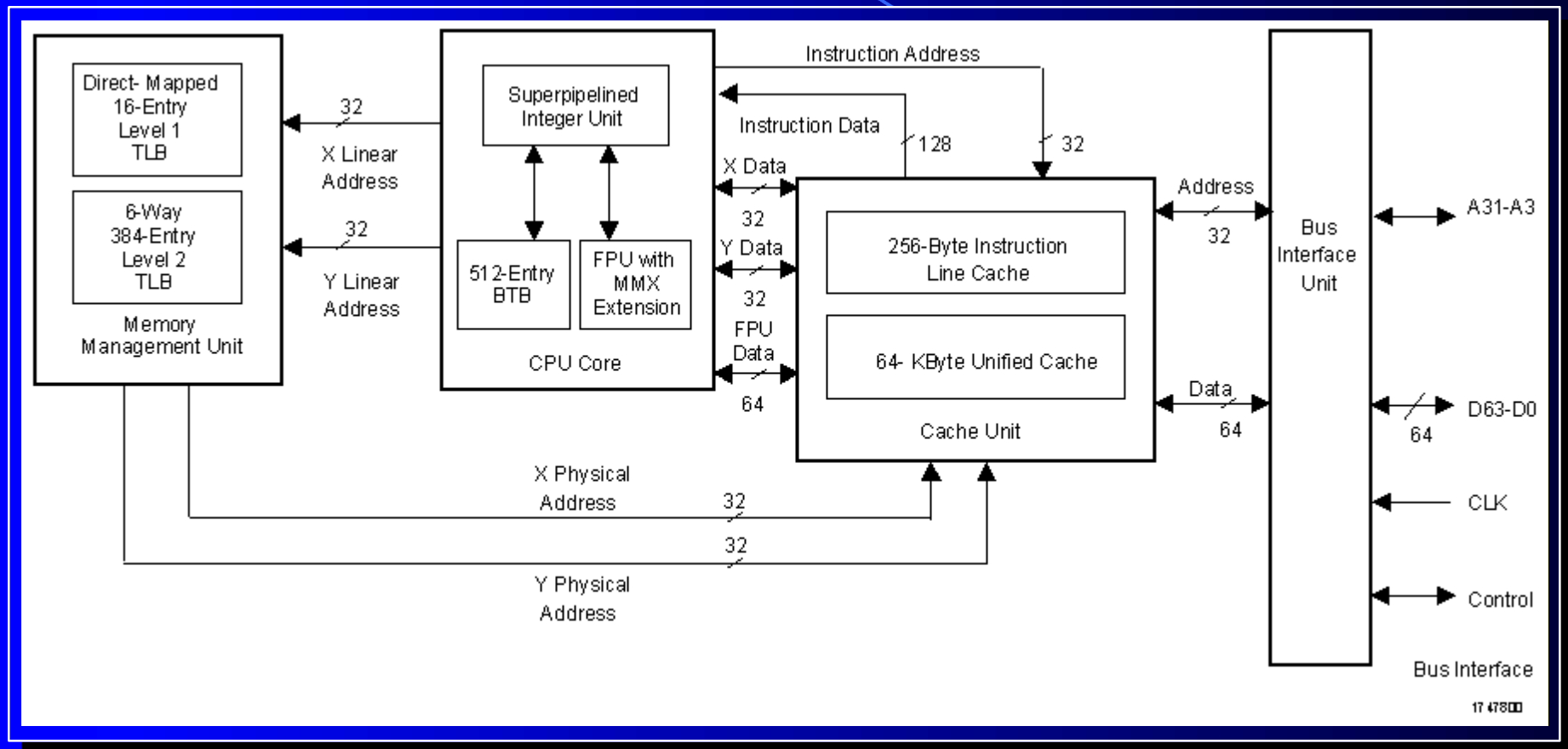
M2 Block Diagram



M2 Architectural Features

Feature	P6	M2
Full x86 instruction set optimization		√
MMX Instructions		√
Superscalar	√	√
Superpipelined	√	√
Register renaming	√	√
Data dependency removal	√	√
Multi-branch prediction	√	√
Speculative execution	√	√
Out-of-order completion	√	√
80-bit floating point unit	√	√

The M2 is a native mode sixth-generation x86 processor

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M2 Branch Unit

- Branch target cache
  - 512 entries
  - 4-way set associative
- Branch history table
  - 512 entries
  - 4-state branch prediction algorithm
- Return stack
  - 8 entries

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M2 Memory Management Unit

- Two level TLB architecture
- L1 TLB
  - 16 entry, direct mapped
  - Dual ported
- L2 TLB
  - 384 entry, 6-way set associative
  - Dual ported

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M2 Cache Architecture

- 64 Kbyte unified cache
  - Primary data cache, secondary instruction cache
  - 4-way set associative, 32 byte line size
  - 2 accesses per cycle
- 256 byte instruction line cache
  - Primary instruction cache
  - 8 entries, 32 byte line size
  - Fully associative

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M2 Performance

- Windows 95 and Windows NT
  - TLB, cache miss rate increase with 32-bit apps
  - Critical word latency limits performance

	Pentium Pro	M2
L1 Cache	8K instr. 8K data	64K unified
L2 Cache	On module 256K or 512K	Off chip 256K or 512K
TLB	32-entry instr. 64-entry data	16-entry L1 384-entry L2
BTB	512-entry	512-entry

- Growing mismatches between processor frequency and bus frequency exacerbate the cache miss penalty
  - 1 bus cycle = 2-3 processor cycles

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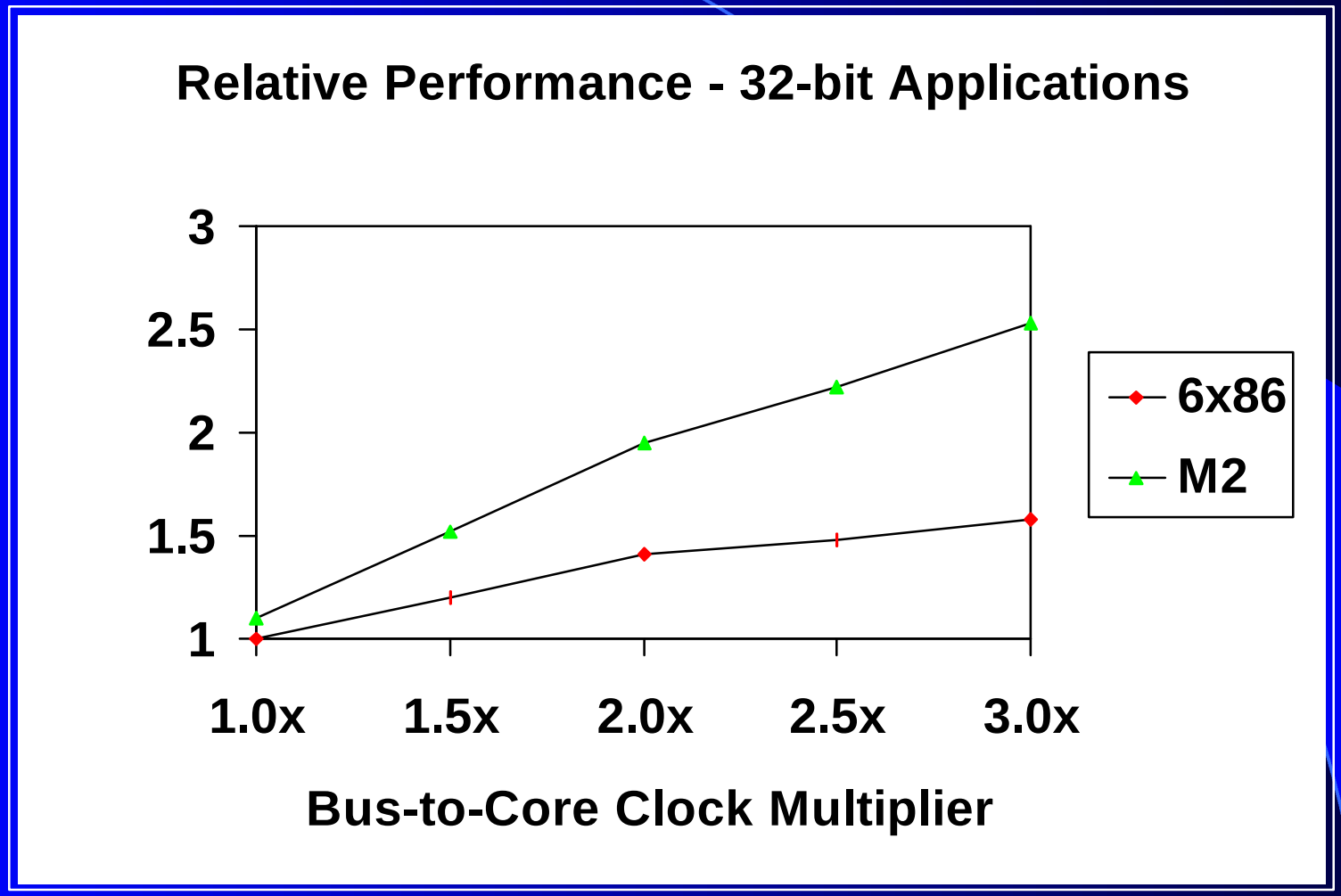
M2 Performance Analysis



M2 Multimedia Extensions: Overview

- New data types: packed Byte/Word/Doubleword, Quadword
- Eight media registers
  - Aliased with floating point (FP) register state
  - 64-bit general purpose registers
- Instruction set
  - Single Instruction Multiple Data (SIMD)
  - Saturation or modulo arithmetic
- Instructions
  - Arithmetic, Comparison, Conversion, Logical, Shift, & Data Transfer
  - Source operand can reside in memory or in media register
  - Destination operand can only reside in media register

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Integrated Multimedia & FPU

- Existing wide adders & multiplier in FP module can be efficiently subdivided to support SIMD processing
- FPU pipeline design can accommodate single-cycle multiply & fused multiply-add operations
- MMX compatibility prohibits simultaneous use of FPU hardware by both x86 FP & MMX operations
  - Why add dedicated functional unit/hardware?

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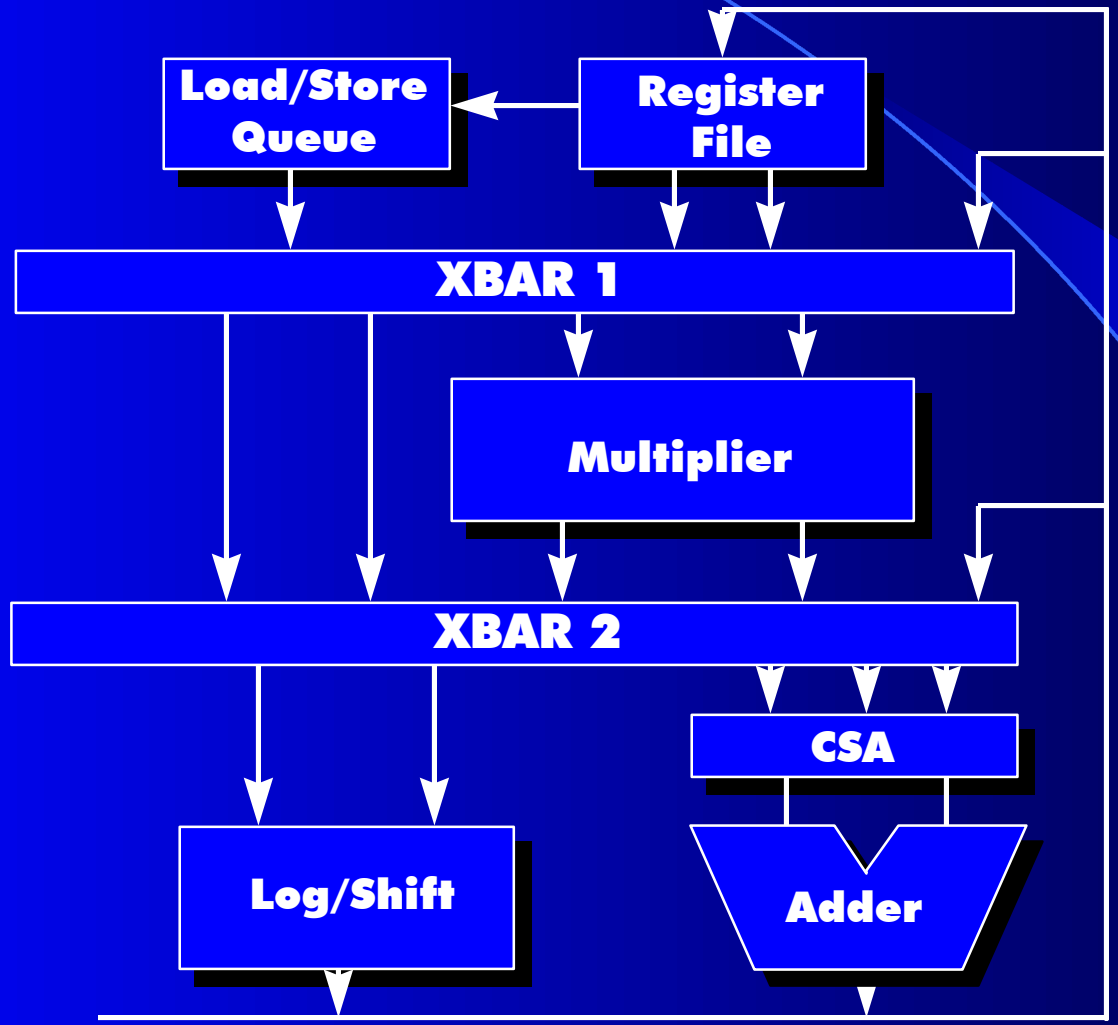
M2 Multimedia/FPU Block Diagram



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M2 Multimedia Architecture: Pipeline Diagram

Multimedia instructions execute in a variable length pipeline. Instructions sent to instruction shelf in IQ stage.

Arithmetic/Logical/Shift:

IF ==> Fetch
ID1 ==> Instruction Decode 1
ID2 ==> Instruction Decode 2
AC1 ==> Address Calculation
AC2 ==> Address Calculation/Cache Access
IQ ==> Transfer to MMX Instruction Shelf
RF ==> FP Register File Access
ALS ==> Arithmetic/Logical/Shift
M1 ==> Multiply Stage 1
M2 ==> Multiply Stage 2
WB ==> Write-Back

Multiply Pipeline:

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M2 Multimedia Performance

- Cache line locking ==> scratch pad memory
  - Locked memory lines guarantee locality of reference
  - Used by driver software code & data
  - Predictable access speed yields real-time capability
- Pipeline accesses to L1 cache
  - Memory operand access at same speed as register access
  - Combined with lockdown capability, permits giant "register files"
- Single-cycle execution
  - EMMS, Add, Subtract, Logical, & Shift operations execute in a single cycle
  - Multiply & MAC execute with single-cycle throughput & latency of 2 clocks

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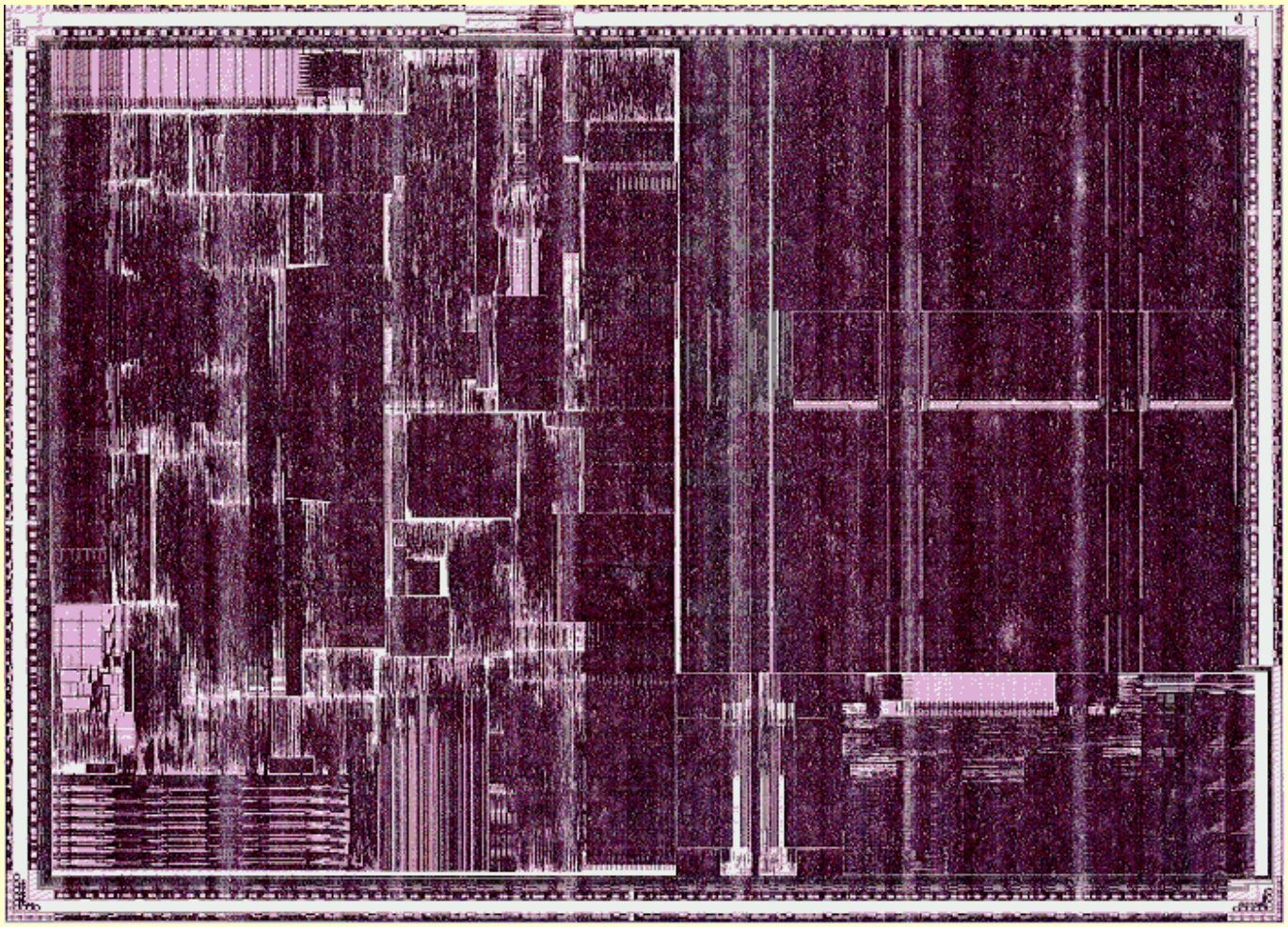
M2 Die



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Summary

- High-performance superscalar x86 microprocessor
- Optimizations for 16-bit and 32-bit code
- 200 MHz core frequency
- MMX software compatible
- Utilizes existing board and chipset infrastructure
- Production: 1H ‘97

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