# 4.0 ELECTRICAL SPECIFICATIONS

## 4.1 Electrical Connections

This section provides information on electrical connections, absolute maximum ratings, recommended operating conditions, DC characteristics, and AC characteristics. All voltage values in Electrical Specifications are measured with respect to $V_{SS}$ unless otherwise noted.

### 4.1.1 Power and Ground Connections and Decoupling

Testing and operating the 6x86 CPU requires the use of standard high frequency techniques to reduce parasitic effects. The high clock frequencies used in the 6x86 CPU and its output buffer circuits can cause transient power surges when several output buffers switch output levels simultaneously. These effects can be minimized by filtering the DC power leads with low-inductance decoupling capacitors, using low impedance wiring, and by utilizing all of the $V_{CC}$ and GND pins. The 6x86 CPU contains 296 pins with 53 pins connected to $V_{CC}$ and 53 connected to $V_{SS}$ (ground).

### 4.1.2 Pull-Up/Pull-Down Resistors

Table 4-1 lists the input pins that are internally connected to pull-up and pull-down resistors. The pull-up resistors are connected to $V_{CC}$ and the pull-down resistors are connected to $V_{SS}$. When unused, these inputs do not require connection to external pull-up or pull-down resistors. The SUSP# pin is unique in that it is connected to a pull-up resistor only when SUSP# is not asserted.

**Table 4-1. Pins Connected to Internal Pull-Up and Pull-Down Resistors**

| SIGNAL | PIN NO. | RESISTOR |
|---|---|---|
| BRDYC# | Y3 | 20-k**Ω** pull-up |
| CLKMUL | Y33 | 20-k**Ω** pull-down |
| QDUMP# | AL7 | 20-k**Ω** pull-up |
| SMI# | AB34 | |
| SUSP# | Y34 | 20-k**Ω** pull-up (see text) |
| TCK | M34 | 20-k**Ω** pull-up |
| TDI | N35 | |
| TMS | P34 | |
| TRST# | Q33 | |
| Reserved | J33 | |
| Reserved | W35 | |
| Reserved | Y35 | |
| Reserved | AN35 | 20-k**Ω** pull-down |

### 4.1.3 Unused Input Pins

All inputs not used by the system designer and not listed in Table 4-1 should be connected either to ground or to $V_{CC}$. Connect active--high inputs to ground through a 20 kΩ (± 10%) pull-down resistor and active-low inputs to $V_{CC}$ through a 20 kΩ (± 10%) pull-up resistor to prevent possible spurious operation.

### 4.1.4 NC and Reserved Pins

Pins designated NC have no internal connections. Pins designated RESV or RESERVED should be left disconnected. Connecting a reserved pin to a pull-up resistor, pull-down resistor, or an active signal could cause unexpected results and possible circuit malfunctions.

## 4.2 Absolute Maximum Ratings

The following table lists absolute maximum ratings for the 6x86 CPU microprocessors. Stresses beyond those listed under Table 4-2 limits may cause permanent damage to the device. These are stress ratings only and do not imply that operation under any conditions other than those listed under "Recommended Operating Conditions" Table 4-3 (Page 4-3) is possible. Exposure to conditions beyond Table 4-2 may (1) reduce device reliability and (2) result in premature failure even when there is no immediately apparent sign of failure. Prolonged exposure to conditions at or near the absolute maximum ratings may also result in reduced useful life and reliability.

**Table 4-2. Absolute Maximum Ratings**

| PARAMETER | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|
| Case Temperature | -65 | 110 | °C | Power Applied |
| Storage Temperature | -65 | 150 | °C | |
| Supply Voltage, $V_{CC}$ | -0.5 | 4.0 | V | |
| Voltage On Any Pin | -0.5 | $V_{CC}$ +0.5 | V | |
| Input Clamp Current, $I_{IK}$ | | 10 | mA | Power Applied |
| Output Clamp Current, $I_{OK}$ | | 25 | mA | Power Applied |

## 4.3 Recommended Operating Conditions

Table 4-3 presents the recommended operating conditions for the 6x86 CPU device.

**Table 4-3. Recommended Operating Conditions**

| PARAMETER | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|
| $T_C$ Operating Case Temperature | 0 | 70 | °C | Power Applied |
| $V_{CC}$ Supply Voltage | 3.15 | 3.6 | V | |
| $V_{IH}$ High-Level Input Voltage | 2.0 | 5.5 | V | |
| $V_{IL}$ Low-Level Input Voltage | -0.3 | 0.8 | V | |
| $I_{OH}$ High-Level Output Current<br>All outputs except A20-A3 and W/R#<br>A20-A3 and W/R# | | <br>-1.0<br>-2.0 | mA | $V_O=V_{OH(MIN)}$ |
| $I_{OL}$ Low-Level Output Current<br>All outputs except A20-A3 and W/R#<br>A20-A3 and W/R# | | <br>5.0<br>10.0 | mA | $V_O=V_{OL(MAX)}$ |

## 4.4 DC Characteristics

### Table 4-4. DC Characteristics (at Recommended Operating Conditions)

| PARAMETER | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| $V_{OL}$ Output Low Voltage<br>$I_{OL}$ = 5 mA | | | 0.4 | V | |
| $V_{OH}$ Output High Voltage<br>$I_{OH}$ = -1 mA | 2.4 | | | V | |
| $I_I$ Input Leakage Current<br>For all pins except those listed in Table 4-1. | | | ±15 | µA | $0 < V_{IN} < V_{CC}$ |
| $I_{IH}$ Input Leakage Current<br>For all pins with internal pull-downs. | | | 200 | µA | $V_{IH}$ = 2.4 V<br>See Table 4-1. |
| $I_{IL}$ Input Leakage Current<br>For all pins with internal pull-ups. | | | -400 | µA | $V_{IL}$ = 0.45 V<br>See Table 4-1. |
| $I_{CC}$ Active $I_{CC}$<br>80 MHz<br>100 MHz<br>110 MHz<br>120 MHz<br>133 MHz | | <br>3.9<br>4.5<br>4.8<br>5.1<br>5.5 | <br>4.7<br>5.4<br>5.8<br>6.1<br>6.6 | <br>A | Note 1, 5 |
| $I_{CCSM}$ Suspend Mode $I_{CC}$<br>80 MHz<br>100 MHz<br>110 MHz<br>120 MHz<br>133 MHz | | <br>43<br>48<br>50<br>51<br>54 | <br>75<br>80<br>83<br>86<br>95 | <br>mA | Note 1, 3, 5 |
| $I_{CCSS}$ Standby $I_{CC}$<br>0 MHz (Suspended/CLK Stopped) | | 35 | 55 | mA | Note 4,5 |
| $C_{IN}$ Input Capacitance | | | 15 | pF | f = 1 MHz, Note 2 |
| $C_{OUT}$ Output Capacitance | | | 20 | pF | f = 1 MHz, Note 2 |
| $C_{IO}$ I/O Capacitance | | | 25 | pF | f = 1 MHz, Note 2 |
| $C_{CLK}$ CLK Capacitance | | | 15 | pF | f = 1 MHz, Note 2 |

Notes:
1. Frequency (MHz) ratings refer to the internal clock frequency.
2. Not 100% tested.
3. All inputs at 0.4 or $V_{CC}$ - 0.4 (CMOS levels). All inputs held static except clock and all outputs unloaded (static $I_{OUT}$ = 0 mA).
4. All inputs at 0.4 or $V_{CC}$ - 0.4 (CMOS levels). All inputs held static and all outputs unloaded (static $I_{OUT}$ = 0 mA).
5. Typical, measured at $V_{CC}$ = 3.3 V.

## 4.5 AC Characteristics

Tables 4-6 through 4-11 (Pages 4-7 through 4-13) list the AC characteristics including output delays, input setup requirements, input hold requirements and output float delays. These measurements are based on the measurement points identified in Figure 4-1 (Page 4-6) and Figure 4-2 (Page 4-7). The rising clock edge reference level $V_{REF}$ and other reference levels are shown in Table 4-5. Input or output signals must cross these levels during testing.

Figure 4-1 shows output delay (A and B) and input setup and hold times (C and D). Input setup and hold times (C and D) are specified minimums, defining the smallest acceptable sampling window a synchronous input signal must be stable for correct operation.

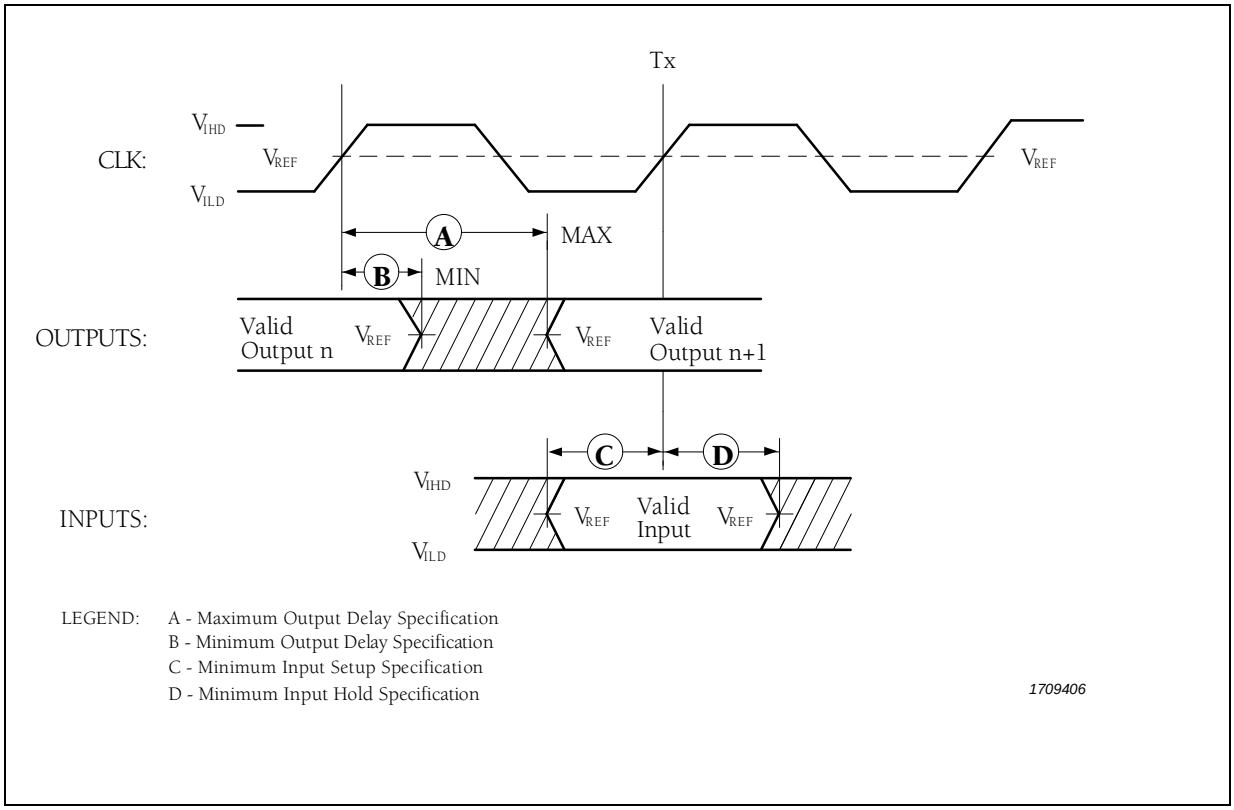


**Figure 4-1. Drive Level and Measurement Points for Switching Characteristics**

**Table 4-5. Drive Level and Measurement Points for Switching Characteristics**

| SYMBOL | VOLTAGE (Volts) |
|---|---|
| $V_{REF}$ | 1.5 |
| $V_{IHD}$ | 2.3 |
| $V_{ILD}$ | 0 |

Note: Refer to Figure 4-1.

**Table 4-6. Clock Specifications**

$T_{CASE}$ = 0°C to 70°C, See Figure 4-2

| SYMBOL | PARAMETER | 40-MHz BUS | | 50-MHz BUS | | 55-MHz BUS | | 60-MHz BUS | | 66-MHz BUS | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| | CLK Frequency | | 40 | | 50 | | 55 | | 60 | | 66.6 | MHz |
| T1 | CLK Period | 25 | | 20 | | 18 | | 16.67 | 33.33 | 15.0 | 30.0 | ns |
| T2 | CLK Period Stability | | ± 250 | | ± 250 | | ±250 | | ±250 | | ±250 | ps |
| T3 | CLK High Time | 9 | | 7 | | 4.0 | | 4.0 | | 4.0 | | ns |
| T4 | CLK Low Time | 9 | | 7 | | 4.0 | | 4.0 | | 4.0 | | ns |
| T5 | CLK Fall Time | 0.15 | 2 | 0.15 | 2 | 0.15 | 1.5 | 0.15 | 1.5 | 0.15 | 1.5 | ns |
| T6 | CLK Rise Time | 0.15 | 2 | 0.15 | 2 | 0.15 | 1.5 | 0.15 | 1.5 | 0.15 | 1.5 | ns |

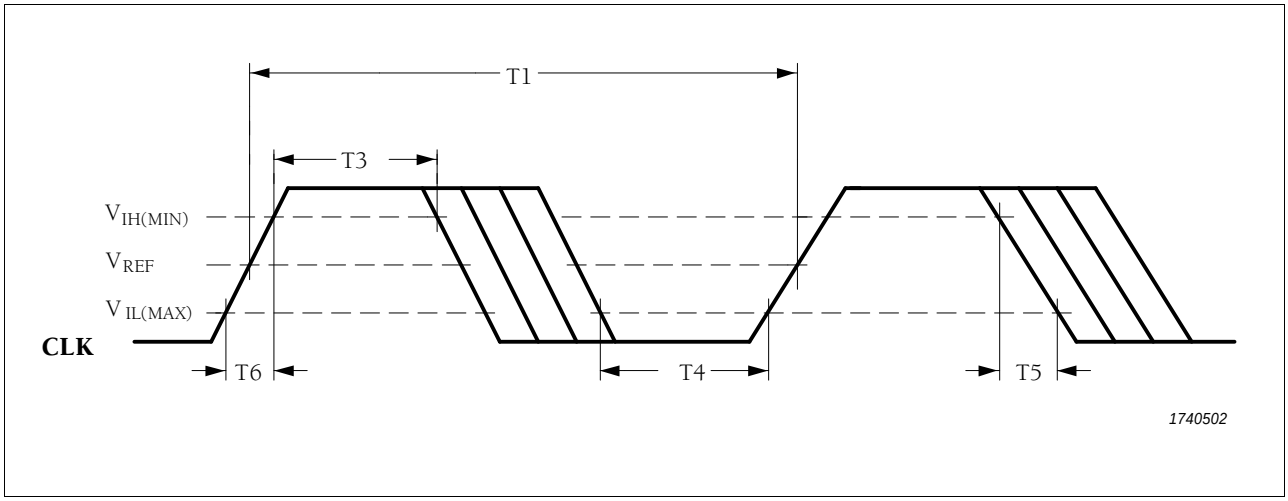


**Figure 4-2. CLK Timing and Measurement Points**

## Table 4-7. Output Valid Delays

$C_L$ = 50 pF, $T_{case}$ = 0°C to 70°C, See Figure 4-3

| | PARAMETER | 40-MHz BUS | | 50-MHz BUS | | 55-MHz BUS | | 60-MHz BUS | | 66-MHz BUS | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| T7a | A31-A3, BE7#-BE0#, CACHE#, D/C#, LBA#, LOCK#, PCD, PWT, SCYC, SMIACT#, W/R# | 3 | 14 | 1.0 | 12 | 1.0 | 7.0 | 1.0 | 7.0 | 1.0 | 7.0 | ns |
| T7b | ADS#, M/IO# | 3 | 14 | 1.0 | 12 | 1.0 | 7.0 | 1.0 | 7.0 | 1.0 | 6.0 | |
| T8 | ADSC# | 3 | 14 | 1.0 | 12 | 1.0 | 7.0 | 1.0 | 7.0 | 1.0 | 7.0 | ns |
| T9 | AP | 3 | 14 | 1.0 | 12 | 1.0 | 8.5 | 1.0 | 8.5 | 1.0 | 8.5 | ns |
| T10 | APCHK#, PCHK#, FERR# | 3 | 16 | 1.0 | 14 | 1.0 | 8.3 | 1.0 | 7.0 | 1.0 | 7.0 | ns |
| T11 | D63-D0, DP7-DP0 (Write) | 3 | 14 | 1.3 | 12 | 1.3 | 8.5 | 1.3 | 7.5 | 1.3 | 7.5 | ns |
| T12a | HIT# | 3 | 14 | 1.0 | 12 | 1.0 | 8.0 | 1.0 | 8.0 | 1.0 | 8.0 | ns |
| T12b | HITM# | 3 | 14 | 1.1 | 12 | 1.1 | 6.0 | 1.1 | 6.0 | 1.1 | 6.0 | |
| T13 | BREQ, HLDA | 3 | 14 | 1.0 | 12 | 1.0 | 8.0 | 1.0 | 8.0 | 1.0 | 8.0 | ns |
| T14 | SUSPA# | 3 | 16 | 1.0 | 14 | 1.0 | 8.0 | 1.0 | 8.0 | 1.0 | 8.0 | ns |

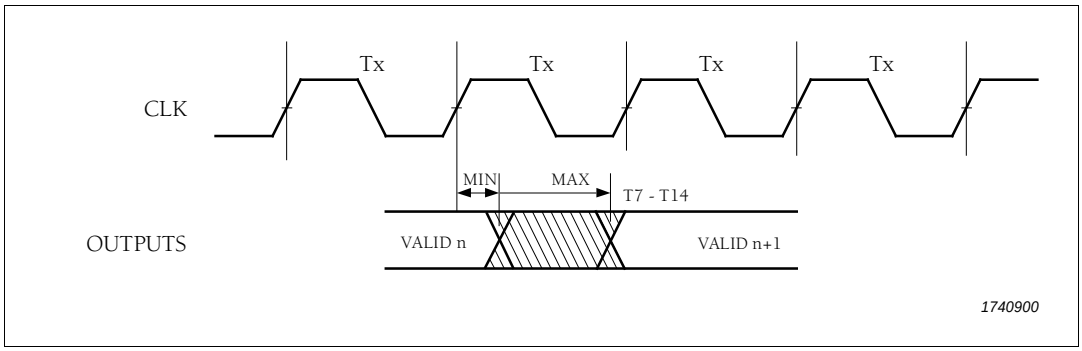


**Figure 4-3. Output Valid Delay Timing**

**Table 4-8. Output Float Delays**

$C_L$ = 50 pF, $T_{case}$ = 0°C to 70°C, See Figure 4-5

| | PARAMETER | 40-MHz BUS | | 50-MHz BUS | | 55-MHz BUS | | 60-MHz BUS | | 66-MHz BUS | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| T15 | A31-A3, ADS#, BE7#-BE0#, BREQ, CACHE#, D/C#, LBA#, LOCK#, M/IO#, PCD, PWT, SCYC, SMIACT#, W/R# | | 19 | | 16 | | 10.0 | | 10.0 | | 10.0 | ns |
| T16 | AP | | 19 | | 16 | | 10.0 | | 10.0 | | 10.0 | ns |
| T17 | D63-D0, DP7-DP0 (Write) | | 19 | | 16 | | 10.0 | | 10.0 | | 10.0 | ns |

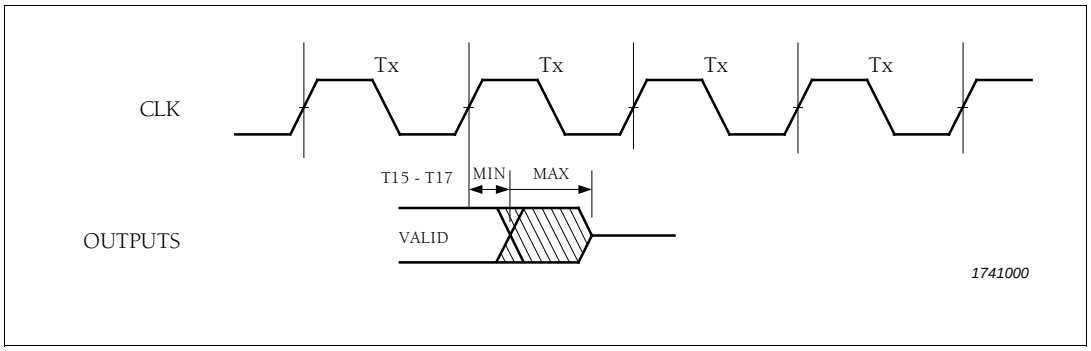


**Figure 4-4. Output Float Delay Timing**

## Table 4-9. Input Setup Times

$T_{case}$ = 0°C to 70°C, See Figure 4-5

| | PARAMETER | 40-MHz BUS | 50-MHz BUS | 55-MHz BUS | 60-MHz BUS | 66-MHz BUS | UNITS |
|---|---|---|---|---|---|---|---|
| | | MIN | MIN | MIN | MIN | MIN | |
| T18 | A20M#, FLUSH#, IGNNE#, SUSP# | 5.0 | 5.0 | 5.0 | 5.0 | 5.0 | ns |
| T19 | AHOLD, BHOLD, BOFF#, DHOLD, HOLD | 5.0 | 5.0 | 5.0 | 5.0 | 5.0 | ns |
| T20 | BRDY# | 5.0 | 5.0 | 5.0 | 5.0 | 5.0 | ns |
| T21 | BRDYC# | 5.0 | 5.0 | 5.0 | 5.0 | 5.0 | ns |
| T22 | A31-A3, AP, BE7#-BE0#, | 5.0 | 5.0 | 5.0 | 5.0 | 5.0 | |
| T22a | D63-D0 (Read), DP7-DP0 (Read) | 3.8 | 3.8 | 3.8 | 3.0 | 3.0 | ns |
| T23 | EADS#, INV | 5.0 | 5.0 | 5.0 | 5.0 | 5.0 | ns |
| T24 | INTR, NMI, RESET, SMI#, WM_RST | 5.0 | 5.0 | 5.0 | 5.0 | 5.0 | ns |
| T25 | EWBE#, KEN#, NA#, WB/WT# | 5.0 | 5.0 | 4.5 | 4.5 | 4.5 | ns |
| T26 | QDUMP# | 5.0 | 5.0 | 5.0 | 5.0 | 5.0 | ns |

## Table 4-10. Input Hold Times

$T_{case}$ = 0°C to 70°C, See Figure 4-5

| SYMBOL | PARAMETER | 40-MHz BUS | 50-MHz BUS | 55-MHz BUS | 60-MHz BUS | 66-MHz BUS | UNITS |
|---|---|---|---|---|---|---|---|
| | | MIN | MIN | MIN | MIN | MIN | |
| T27 | A20M#, FLUSH#, IGNNE#, SUSP# | 3.0 | 2.0 | 1.0 | 1.0 | 1.0 | ns |
| T28 | AHOLD, BHOLD, BOFF#, DHOLD, HOLD | 3.0 | 2.0 | 1.0 | 1.0 | 1.0 | ns |
| T29 | BRDY# | 3.0 | 2.0 | 1.0 | 1.0 | 1.0 | ns |
| T30 | BRDYC# | 3.0 | 2.0 | 1.0 | 1.0 | 1.0 | ns |
| T31a | A31-A3, AP, BE7#-BE0# | 3.0 | 2.0 | 1.0 | 1.0 | 1.0 | ns |
| T31b | D63-D0, DP7-DP0 (Read) | 3.0 | 2.0 | 2.0 | 2.0 | 2.0 | ns |
| T32 | EADS#, INV | 3.0 | 2.0 | 1.0 | 1.0 | 1.0 | ns |
| T33 | INTR, NMI, RESET, SMI#, WM_RST | 3.0 | 2.0 | 1.0 | 1.0 | 1.0 | ns |
| T34 | EWBE#, KEN#, NA#, WB/WT# | 3.0 | 2.0 | 1.0 | 1.0 | 1.0 | ns |
| T35 | QDUMP# | 3.0 | 2.0 | 1.0 | 1.0 | 1.0 | ns |

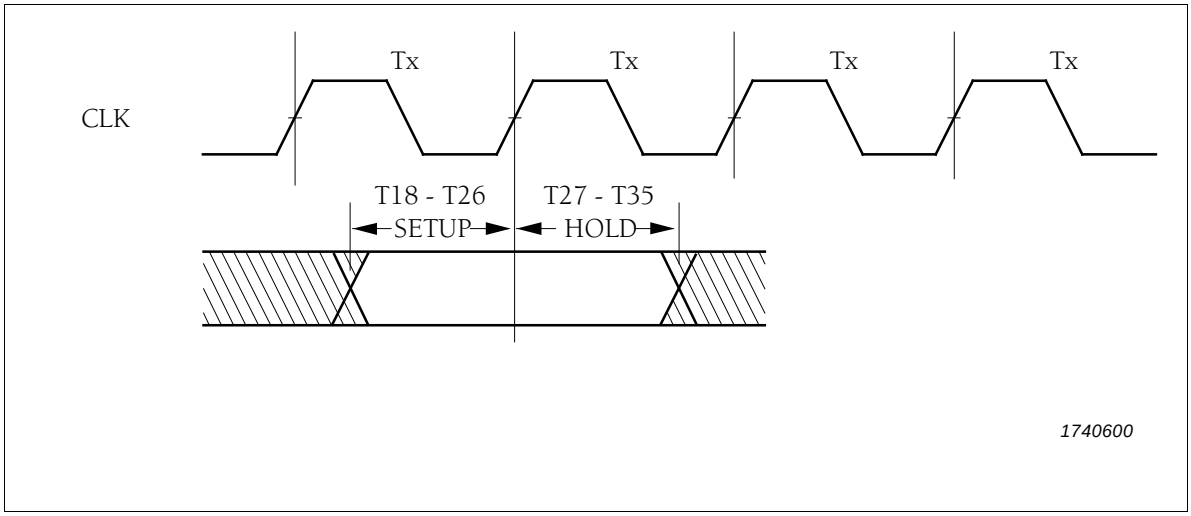


**Figure 4-5. Input Setup and Hold Timing**

## Table 4-11. JTAG AC Specifications

| SYMBOL | PARAMETER | ALL BUS FREQUENCIES | | UNITS | FIGURE |
|---|---|---|---|---|---|
| | | MIN | MAX | | |
| | TCK Frequency (MHz) | | 20 | ns | |
| T36 | TCK Period | 50 | | ns | 4-6 |
| T37 | TCK High Time | 25 | | ns | 4-6 |
| T38 | TCK Low Time | 25 | | ns | 4-6 |
| T39 | TCK Rise Time | | 5 | ns | 4-6 |
| T40 | TCK Fall Time | | 5 | ns | 4-6 |
| T41 | TDO Valid Delay | 3 | 20 | ns | 4-7 |
| T42 | Non-test Outputs Valid Delay | 3 | 20 | ns | 4-7 |
| T43 | TDO Float Delay | | 25 | ns | 4-7 |
| T44 | Non-test Outputs Float Delay | | 25 | ns | 4-7 |
| T45 | TRST# Pulse Width | 40 | | ns | 4-8 |
| T46 | TDI, TMS Setup Time | 20 | | ns | 4-7 |
| T47 | Non-test Inputs Setup Time | 20 | | ns | 4-7 |
| T48 | TDI, TMS Hold Time | 13 | | ns | 4-7 |
| T49 | Non-test Inputs Hold Time | 13 | | ns | 4-7 |

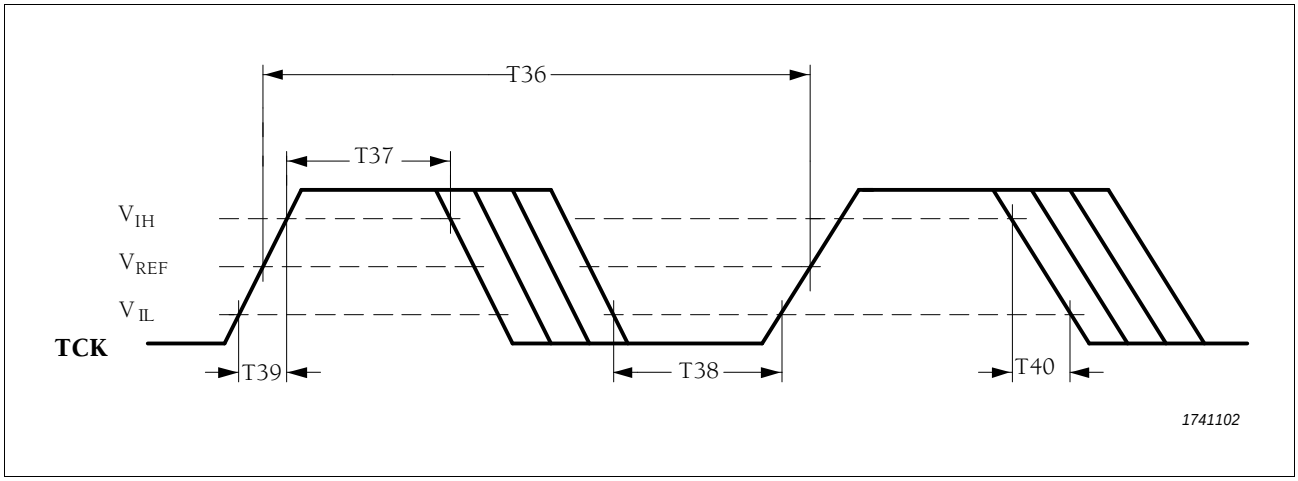


**Figure 4-6. TCK Timing and Measurement Points**

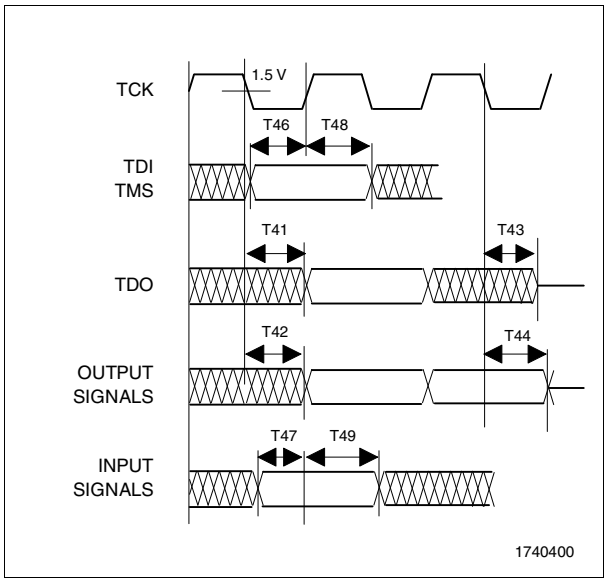


**Figure 4-7. JTAG Test Timings**

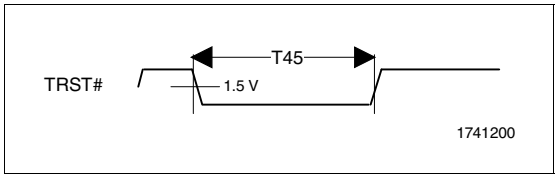


**Figure 4-8. Test Reset Timing**

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