

Am386™ SX

High-Performance, 32-Bit Microprocessor
with 16-Bit Data Bus


Advanced
Micro
Devices

DISTINCTIVE CHARACTERISTICS

- Compatible with 386SX systems and software
- 20-MHz operating speed
- Pin-for-pin replacement of the Intel i386SX
- Supports 387SX-compatible math coprocessors
- 100-lead PQFP package with optional protective ring for better lead coplanarity
- 24-bit address bus, 16-bit data bus
- Advanced 0.8 micron CMOS technology

GENERAL DESCRIPTION

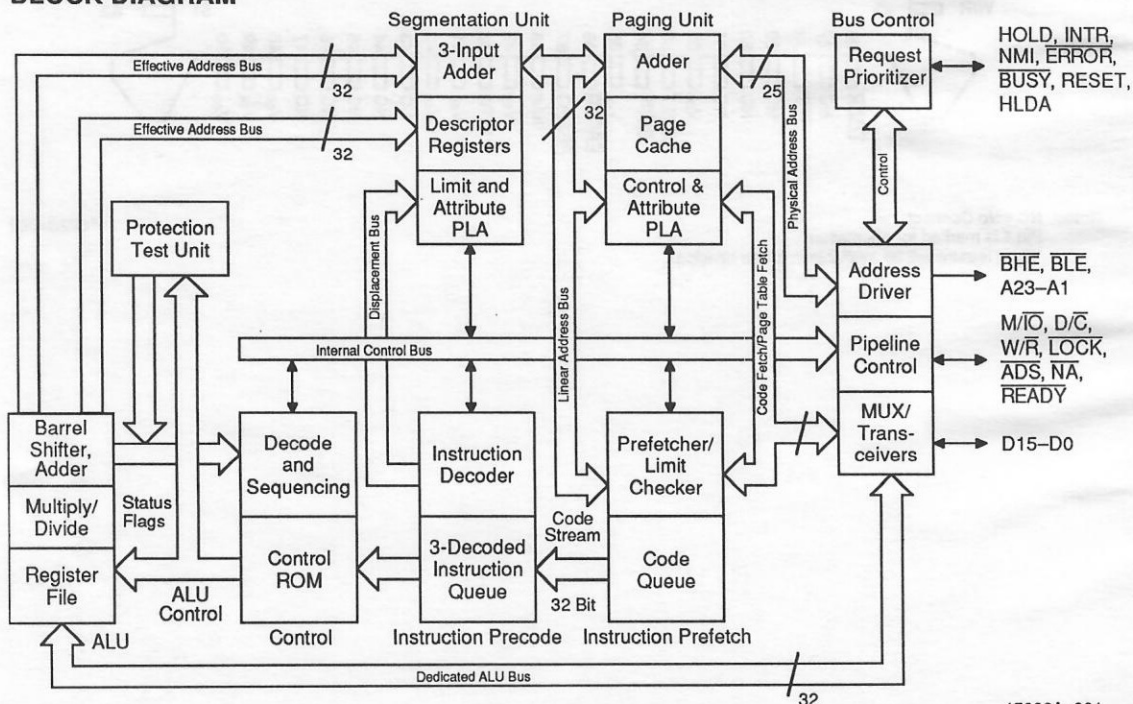
The Am386SX microprocessor is a compatible implementation of the Intel i386SX. It is engineered to meet strict requirements for compatibility. It is compatible with hardware designed for 386SX systems and is, in fact, a pin-for-pin replacement of the Intel i386SX. It is also compatible with operating systems written for the 386 and the wide variety of commercially available software applications.

The Am386SX microprocessor is a 32-bit CPU with a 16-bit external data bus, and a 24-bit external address

bus. It provides the performance and compatibility benefits of the 386 architecture with the cost savings associated with 16-bit hardware.

The device is manufactured using the AMD® advanced 0.8 micron CMOS process. It is packaged in a 100-pin plastic quad flat pack (PQFP). This package may be shipped in an optional protective ring for better lead protection during manufacturing.

BLOCK DIAGRAM

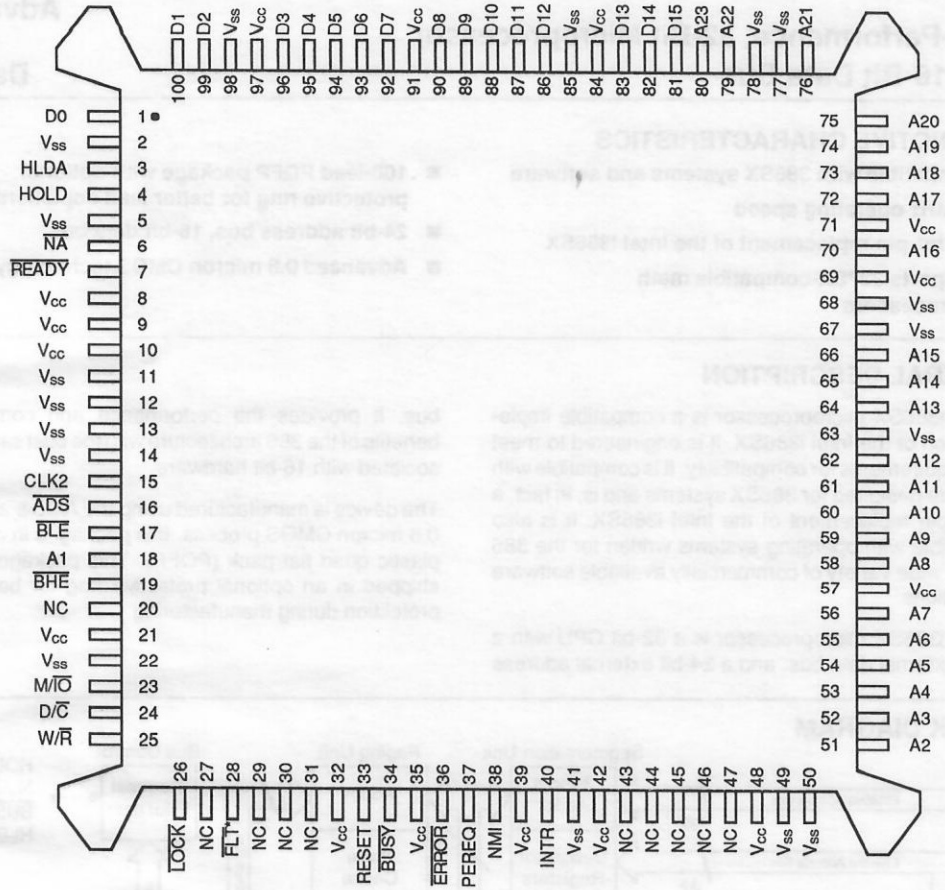


15022A-001



CONNECTION DIAGRAM

Top View



Notes: NC = No Connect
Pin 1 is marked for orientation.
*Float feature will be available in future revisions.

15022B-002

PIN DESIGNATIONS (Sorted by Pin Name)

Address		Data		Control		NC	V _{CC}	V _{SS}
Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin No.	Pin No.	Pin No.
A1	18	D0	1	ADS	16	20	8	2
A2	51	D1	100	BHE	19	27	9	5
A3	52	D2	99	BLE	17	29	10	11
A4	53	D3	96	BUSY	34	30	21	12
A5	54	D4	95	CLK2	15	31	32	13
A6	55	D5	94	D/C	24	43	39	14
A7	56	D6	93	ERROR	36	44	42	22
A8	58	D7	92	FLT*	28	45	48	35
A9	59	D8	90	HLDA	3	46	57	41
A10	60	D9	89	HOLD	4	47	69	49
A11	61	D10	88	INTR	40		71	50
A12	62	D11	87	LOCK	26		84	63
A13	64	D12	86	M/IO	23		91	67
A14	65	D13	83	NA	6		97	68
A15	66	D14	82	NMI	38			77
A16	70	D15	81	PEREQ	37			78
A17	72			READY	7			85
A18	73			RESET	33			98
A19	74			W/R	25			
A20	75							
A21	76							
A22	79							
A23	80							

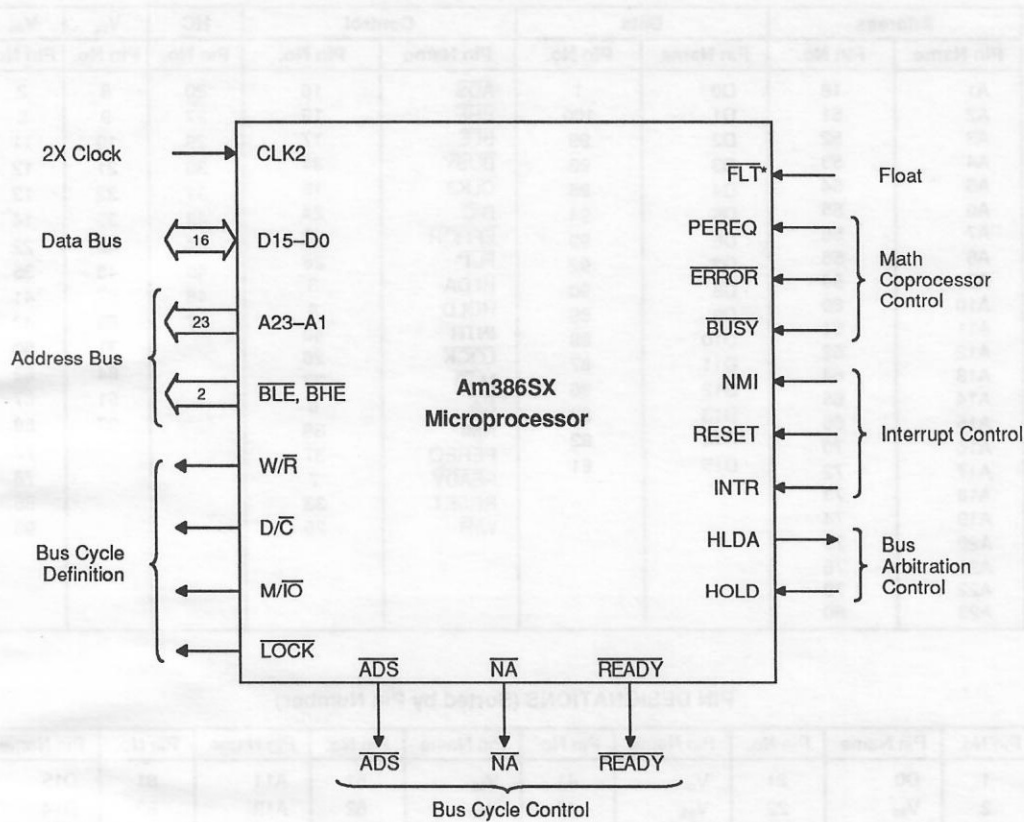
PIN DESIGNATIONS (Sorted by Pin Number)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	D0	21	V _{CC}	41	V _{SS}	61	A11	81	D15
2	V _{SS}	22	V _{SS}	42	V _{CC}	62	A12	82	D14
3	HLDA	23	M/IO	43	NC	63	V _{SS}	83	D13
4	HOLD	24	D/C	44	NC	64	A13	84	V _{CC}
5	V _{SS}	25	W/R	45	NC	65	A14	85	V _{SS}
6	NA	26	LOCK	46	NC	66	A15	86	D12
7	READY	27	NC	47	NC	67	V _{SS}	87	D11
8	V _{CC}	28	FLT*	48	V _{CC}	68	V _{SS}	88	D10
9	V _{CC}	29	NC	49	V _{SS}	69	V _{CC}	89	D9
10	V _{CC}	30	NC	50	V _{SS}	70	A16	90	D8
11	V _{SS}	31	NC	51	A2	71	V _{CC}	91	V _{CC}
12	V _{SS}	32	V _{CC}	52	A3	72	A17	92	D7
13	V _{SS}	33	RESET	53	A4	73	A18	93	D6
14	V _{SS}	34	BUSY	54	A5	74	A19	94	D5
15	CLK2	35	V _{SS}	55	A6	75	A20	95	D4
16	ADS	36	ERROR	56	A7	76	A21	96	D3
17	BLE	37	PEREQ	57	V _{CC}	77	V _{SS}	97	V _{CC}
18	A1	38	NMI	58	A8	78	V _{SS}	98	V _{SS}
19	BHE	39	V _{CC}	59	A9	79	A22	99	D2
20	NC	40	INTR	60	A10	80	A23	100	D1

*Float feature will be available in future revisions.



LOGIC SYMBOL



*Float feature will be available in future revisions.

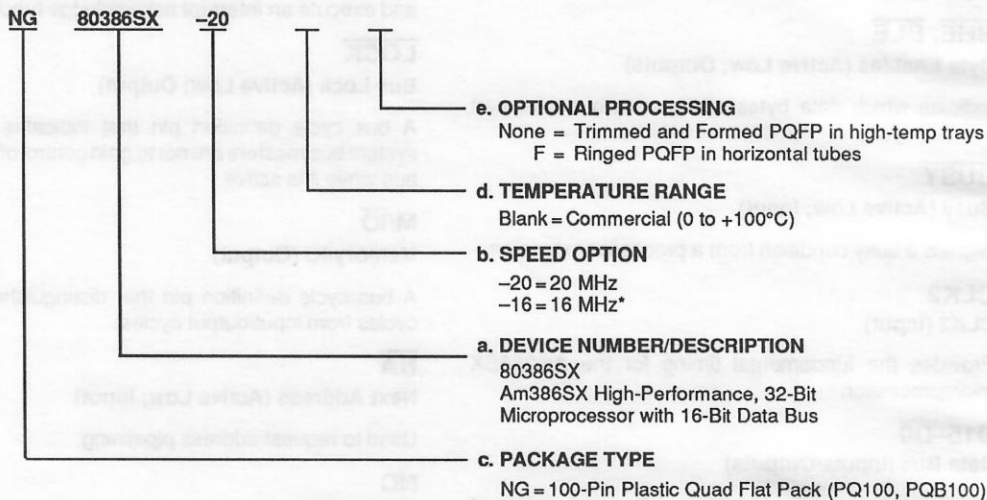
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ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number/Description
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations		
NG	80386SX	-20 -16* -20F -16F*

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

*Contact AMD for 16 MHz availability.



PIN DESCRIPTION

A23–A1

Address Bus (Outputs)

Outputs physical memory or port I/O addresses.

ADS

Address Status (Active Low; Output)

Indicates that a valid bus cycle definition and address (W/R, D/C, M/I/O, BHE, BLE, and A23–A1) are being driven at the Am386SX microprocessor pins.

BHE, BLE

Byte Enables (Active Low; Outputs)

Indicate which data bytes of the data bus take part in a bus cycle.

BUSY

Busy (Active Low; Input)

Signals a busy condition from a processor extension.

CLK2

CLK2 (Input)

Provides the fundamental timing for the Am386SX microprocessor.

D15–D0

Data Bus (Inputs/Outputs)

Inputs data during memory, I/O, and interrupt acknowledge read cycles; outputs data during memory and I/O write cycles.

D/C

Data/Control (Output)

A bus cycle definition pin that distinguishes data cycles, either memory or I/O, from control cycles which are: interrupt acknowledge, halt, and code fetch.

ERROR

Error (Active Low; Input)

Signals an error condition from a processor extension.

FLT*

Float (Active Low; Input)

An input which forces all bi-directional and output signals, including HLDA, to the three-state condition.

HLDA

Bus Hold Acknowledge (Active High; Output)

Output indicates that the Am386SX microprocessor has surrendered control of its logical bus to another bus master.

HOLD

Bus Hold Request (Active High; Input)

Input allows another bus master to request control of the local bus.

INTR

Interrupt Request (Active High; Input)

A maskable input that signals the Am386SX microprocessor to suspend execution of the current program and execute an interrupt acknowledge function.

LOCK

Bus Lock (Active Low; Output)

A bus cycle definition pin that indicates that other system bus masters are not to gain control of the system bus while it is active.

M/I/O

Memory/I/O (Output)

A bus cycle definition pin that distinguishes memory cycles from input/output cycles.

NA

Next Address (Active Low; Input)

Used to request address pipelining.

NC

No Connect

Should always be left unconnected. Connection of a NC pin may cause the processor to malfunction, or be incompatible with future steppings of the Am386SX microprocessor.

NMI

Non-Maskable Interrupt Request (Active High; Input)

A non-maskable input that signals the Am386SX microprocessor to suspend execution of the current program and execute an interrupt acknowledge function.

PEREQ

Processor Extension Request (Active High; Input)

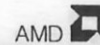
Indicates that the processor has data to be transferred by the Am386SX microprocessor.

READY

Bus Ready (Active Low; Input)

Terminates the bus cycle.

*Float feature will be available in future revisions.

**RESET****Reset (Active High; Input)**

Suspends any operation in progress and places the Am386SX microprocessor in a known reset state.

V_{cc}**System Power (Active High; Input)**

Provides the +5 V nominal DC supply input.

V_{ss}**System Ground (Input)**

Provides the 0 V connection from which all inputs and outputs are measured.

W/ \bar{R} **Write/Read (Output)**

A bus cycle definition pin that distinguishes write cycles from read cycles.

Pin	Symbol	Function	Direction
1	RESET	Reset (Active High)	Input
2	V _{CC}	System Power (+5 V)	Input
3	V _{SS}	System Ground (0 V)	Input
4	W/ \bar{R}	Write/Read (Active Low)	Output
5	AD ₁₅	Address Bus (Data In)	Input
6	AD ₁₄	Address Bus (Data In)	Input
7	AD ₁₃	Address Bus (Data In)	Input
8	AD ₁₂	Address Bus (Data In)	Input
9	AD ₁₁	Address Bus (Data In)	Input
10	AD ₁₀	Address Bus (Data In)	Input
11	AD ₉	Address Bus (Data In)	Input
12	AD ₈	Address Bus (Data In)	Input
13	AD ₇	Address Bus (Data In)	Input
14	AD ₆	Address Bus (Data In)	Input
15	AD ₅	Address Bus (Data In)	Input
16	AD ₄	Address Bus (Data In)	Input
17	AD ₃	Address Bus (Data In)	Input
18	AD ₂	Address Bus (Data In)	Input
19	AD ₁	Address Bus (Data In)	Input
20	AD ₀	Address Bus (Data In)	Input
21	DATA ₁₅	Data Bus (Data Out)	Output
22	DATA ₁₄	Data Bus (Data Out)	Output
23	DATA ₁₃	Data Bus (Data Out)	Output
24	DATA ₁₂	Data Bus (Data Out)	Output
25	DATA ₁₁	Data Bus (Data Out)	Output
26	DATA ₁₀	Data Bus (Data Out)	Output
27	DATA ₉	Data Bus (Data Out)	Output
28	DATA ₈	Data Bus (Data Out)	Output
29	DATA ₇	Data Bus (Data Out)	Output
30	DATA ₆	Data Bus (Data Out)	Output
31	DATA ₅	Data Bus (Data Out)	Output
32	DATA ₄	Data Bus (Data Out)	Output
33	DATA ₃	Data Bus (Data Out)	Output
34	DATA ₂	Data Bus (Data Out)	Output
35	DATA ₁	Data Bus (Data Out)	Output
36	DATA ₀	Data Bus (Data Out)	Output



ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under bias -65 to 110°C
 Storage Temperature -65 to 150°C

Stresses above those listed may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGES

Supply Voltage with respect to V_{SS} . . . -0.5 V to 6.5 V
 Voltage on other pins -0.5 V to $(V_{CC} + 0.5)V$

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges

$V_{CC} = 5 V \pm 10\%$; $T_{CASE} = 0^\circ C$ to $100^\circ C$

Symbol	Parameter Description	Notes	Min	Max	Unit
V_{IL}	Input Low Voltage		-0.3	+0.8	V
V_{IH}	Input High Voltage		2.0	$V_{CC} + 0.3$	V
V_{ILC}	CLK2 Input Low Voltage		-0.3	+0.8	V
V_{IHC}	CLK2 Input High Voltage		$V_{CC} - 0.8$	$V_{CC} + 0.3$	V
V_{OL}	Output Low Voltage $I_{OL} = 4$ mA: A23-A1, D15-D0 $I_{OL} = 5$ mA: BHE, BLE, W/R, D/C, M/I/O, LOCK, ADS, HLDA			0.45 0.45	V V
V_{OH}	Output High Voltage $I_{OH} = 1.0$ mA: A23-A1, D15-D0 $I_{OH} = 0.2$ mA: A23-A1, D15-D0 $I_{OH} = 0.9$ mA: BHE, BLE, W/R, D/C, M/I/O, LOCK, ADS, HLDA $I_{OH} = 0.18$ mA: BHE, BLE, W/R, D/C, M/I/O, LOCK, ADS, HLDA		2.4 $V_{CC} - 0.5$ 2.4 $V_{CC} - 0.5$		V V V
I_{LI}	Input Leakage Current (for all pins except PEREQ, BUSY, FLT*, and ERROR)	$0 V \leq V_{IN} \leq V_{CC}$		± 15	μA
I_{IH}	Input Leakage Current (PEREQ pin)	$V_{IH} = 2.4 V$ (1)		200	μA
I_{IL}	Input Leakage Current (BUSY, ERROR, and FLT* pins)	$V_{IL} = 0.45 V$ (2)		-400	μA
I_{LO}	Output Leakage Current	$0.45 V \leq V_{OUT} \leq V_{CC}$		± 15	μA
I_{CC}	Supply Current CLK2 = 32 MHz: with -16** CLK2 = 40 MHz: with -20	I_{CC} Typ = 175 mA (3) I_{CC} Typ = 200 mA (3)		275 305	mA mA
C_{IN}	Input Capacitance	$F_C = 1$ MHz (4)		10	pF
C_{OUT}	Output or I/O Capacitance	$F_C = 1$ MHz (4)		12	pF
C_{CLK}	CLK2 Capacitance	$F_C = 1$ MHz (4)		20	pF

Notes: Tested at the minimum operating frequency of the part.

*Float feature will be available in future revisions.

**Contact AMD for 16 MHz availability.

1. PEREQ input has an internal pull-down resistor.

2. BUSY, FLT*, and ERROR inputs each have an internal pull-up resistor.

3. I_{CC} Max measurement at worst case frequency, V_{CC} , and temperature, outputs unloaded.

4. Not 100% tested.

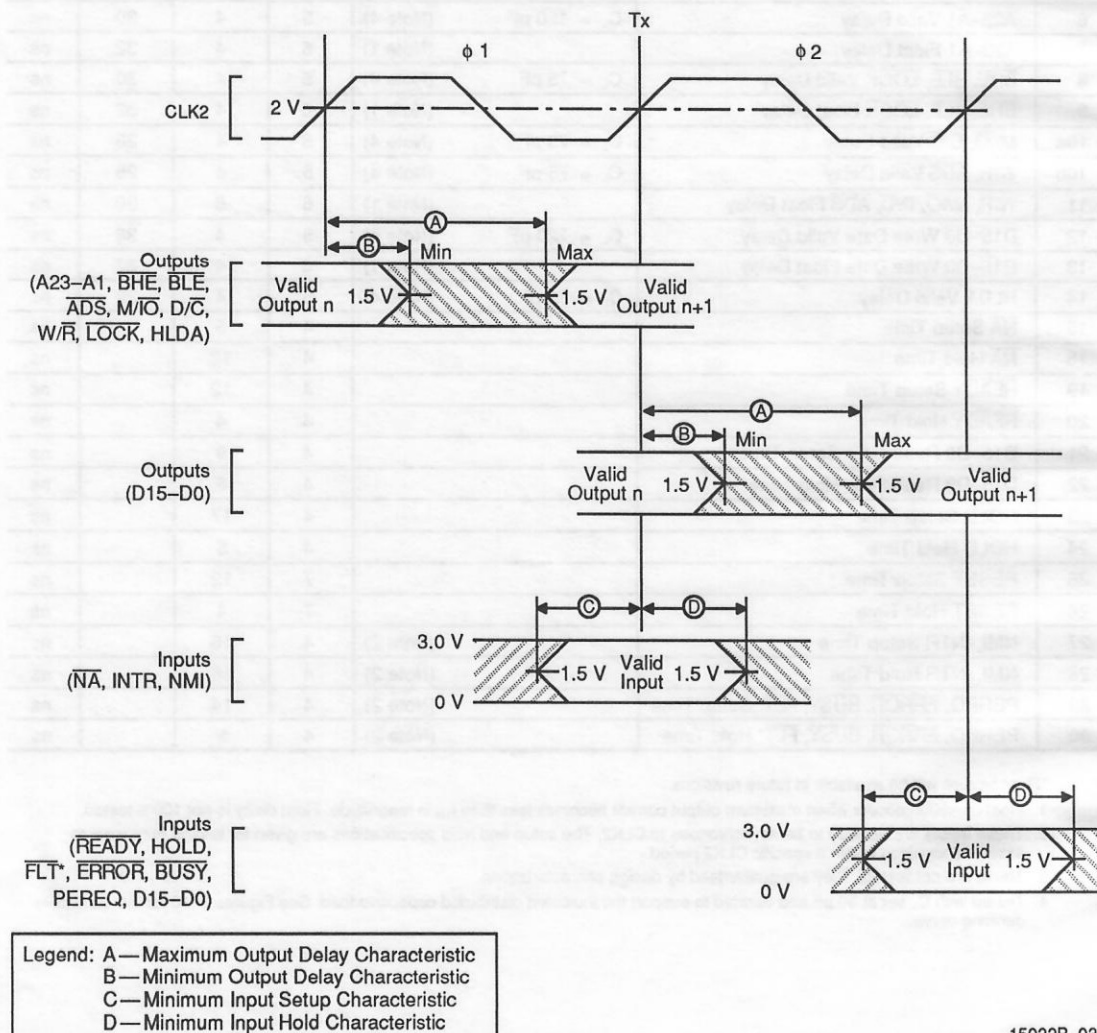
SWITCHING CHARACTERISTICS

The switching characteristics given consist of output delays, input setup requirements, and input hold requirements. All switching characteristics are relative to the CLK2 rising edge crossing the 2.0 V level.

Switching characteristic measurement is defined by Figure 1. Inputs must be driven to the voltage levels indicated by Figure 1 when switching characteristics are measured. Output delays are specified with minimum and maximum limits measured, as shown. The minimum delay times are hold times provided to external circuitry. Input setup and hold times are specified as

minimums, defining the smallest acceptable sampling window. Within the sampling window, a synchronous input signal must be stable for correct operation.

Outputs \overline{NA} , $\overline{W/R}$, $\overline{D/C}$, $\overline{M/I/O}$, \overline{LOCK} , \overline{BHE} , \overline{BLE} , A23–A1, and HLDA only change at the beginning of phase one. D15–D0 (write cycles) only change at the beginning of phase two. The \overline{READY} , \overline{HOLD} , \overline{BUSY} , \overline{ERROR} , \overline{PEREQ} , \overline{FLT}^* , and D15–D0 (read cycles) inputs are sampled at the beginning of phase one. The \overline{NA} , \overline{INTR} , and \overline{NMI} inputs are sampled at the beginning of phase two.



15022B-030

Figure 1. Drive Levels and Measurement Points for Switching Characteristics

*Float feature will be available in future revisions.



SWITCHING CHARACTERISTICS (continued)

Switching Characteristics at 20 MHz: $V_{CC} = 5 V \pm 10\%$; $T_{CASE} = 0^{\circ}C$ to $100^{\circ}C$

Symbol	Parameter Description	Notes	Ref. Figure	Min	Max	Unit
	Operating Frequency	Half CLK2 freq.		2	20	MHz
1	CLK2 Period		2	25	250	ns
2a	CLK2 High Time	at 2 V (Note 3)	2	8		ns
2b	CLK2 High Time	at ($V_{CC} - 0.8 V$) (Note 3)	2	5		ns
3a	CLK2 Low Time	at 2 V (Note 3)	2	8		ns
3b	CLK2 Low Time	at 0.8 V (Note 3)	2	6		ns
4	CLK2 Fall Time	($V_{CC} - 0.8 V$) to 0.8 V (Note 3)	2		8	ns
5	CLK2 Rise Time	0.8 V to ($V_{CC} - 0.8 V$) (Note 3)	2		8	ns
6	A23-A1 Valid Delay	$C_L = 120 pF$ (Note 4)	5	4	30	ns
7	A23-A1 Float Delay	(Note 1)	6	4	32	ns
8	\overline{BHE} , \overline{BLE} , \overline{LOCK} Valid Delay	$C_L = 75 pF$ (Note 4)	5	4	30	ns
9	\overline{BHE} , \overline{BLE} , \overline{LOCK} Float Delay	(Note 1)	6	4	32	ns
10a	\overline{MIO} , $\overline{D/C}$ Valid Delay	$C_L = 75 pF$ (Note 4)	5	4	28	ns
10b	$\overline{W/R}$, \overline{ADS} Valid Delay	$C_L = 75 pF$ (Note 4)	5	4	26	ns
11	$\overline{W/R}$, \overline{MIO} , $\overline{D/C}$, \overline{ADS} Float Delay	(Note 1)	6	6	30	ns
12	D15-D0 Write Data Valid Delay	$C_L = 120 pF$ (Note 4)	5	4	38	ns
13	D15-D0 Write Data Float Delay	(Note 1)	6	4	27	ns
14	HLDA Valid Delay	$C_L = 75 pF$ (Note 4)	5	4	28	ns
15	\overline{NA} Setup Time		4	5		ns
16	\overline{NA} Hold Time		4	12		ns
19	\overline{READY} Setup Time		4	12		ns
20	\overline{READY} Hold Time		4	4		ns
21	D15-D0 Read Data Setup Time		4	9		ns
22	D15-D0 Read Data Hold Time		4	6		ns
23	HOLD Setup Time		4	17		ns
24	HOLD Hold Time		4	5		ns
25	RESET Setup Time		7	12		ns
26	RESET Hold Time		7	4		ns
27	NMI, INTR Setup Time	(Note 2)	4	16		ns
28	NMI, INTR Hold Time	(Note 2)	4	16		ns
29	\overline{PEREQ} , \overline{ERROR} , \overline{BUSY} , \overline{FLT}^* Setup Time	(Note 2)	4	14		ns
30	\overline{PEREQ} , \overline{ERROR} , \overline{BUSY} , \overline{FLT}^* Hold Time	(Note 2)	4	5		ns

Notes: *Float feature will be available in future revisions.

1. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not 100% tested.
2. These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.
3. These are not tested. They are guaranteed by design characterization.
4. Tested with C_L set at 50 pF and derated to support the indicated distributed capacitive load. See Figures 8-10 for the capacitive derating curve.

SWITCHING CHARACTERISTICS

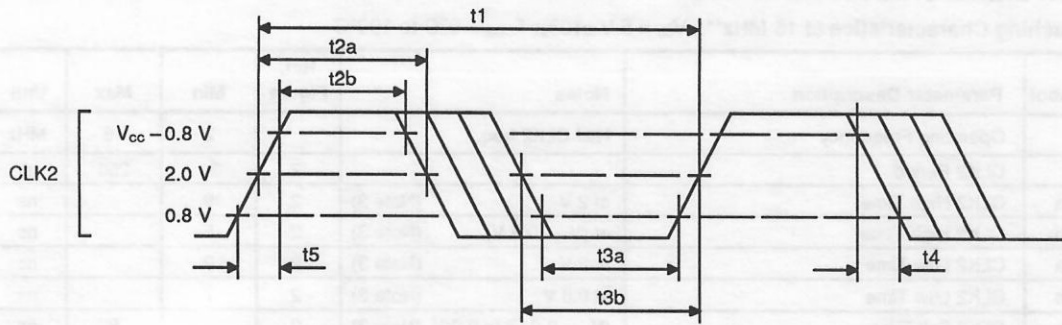
Switching Characteristics at 16 MHz**: $V_{CC} = 5 V \pm 10\%$; $T_{CASE} = 0^{\circ}C$ to $100^{\circ}C$

Symbol	Parameter Description	Notes	Ref. Figure	Min	Max	Unit
	Operating Frequency	Half CLK2 freq.		2	16	MHz
1	CLK2 Period		2	31	250	ns
2a	CLK2 High Time	at 2 V (Note 3)	2	9		ns
2b	CLK2 High Time	at ($V_{CC} - 0.8 V$) (Note 3)	2	5		ns
3a	CLK2 Low Time	at 2 V (Note 3)	2	9		ns
3b	CLK2 Low Time	at 0.8 V (Note 3)	2	7		ns
4	CLK2 Fall Time	($V_{CC} - 0.8 V$) to 0.8 V (Note 3)	2		8	ns
5	CLK2 Rise Time	0.8 V to ($V_{CC} - 0.8 V$) (Note 3)	2		8	ns
6	A23–A1 Valid Delay	$C_L = 120 pF$ (Note 4)	5	4	36	ns
7	A23–A1 Float Delay	(Note 1)	6	4	40	ns
8	\overline{BHE} , \overline{BLE} , \overline{LOCK} Valid Delay	$C_L = 75 pF$ (Note 4)	5	4	36	ns
9	\overline{BHE} , \overline{BLE} , \overline{LOCK} Float Delay	(Note 1)	6	4	40	ns
10	$\overline{W/\overline{R}}$, $\overline{M/\overline{IO}}$, $\overline{D/\overline{C}}$, \overline{ADS} Valid Delay	$C_L = 75 pF$ (Note 4)	5	4	33	ns
11	$\overline{W/\overline{R}}$, $\overline{M/\overline{IO}}$, $\overline{D/\overline{C}}$, \overline{ADS} Float Delay	(Note 1)	6	6	35	ns
12	D15–D0 Write Data Valid Delay	$C_L = 120 pF$ (Note 4)	5	4	40	ns
13	D15–D0 Write Data Float Delay	(Note 1)	6	4	35	ns
14	HLDA Valid Delay	$C_L = 75 pF$ (Note 4)	5	4	33	ns
15	\overline{NA} Setup Time		4	5		ns
16	\overline{NA} Hold Time		4	21		ns
19	\overline{READY} Setup Time		4	19		ns
20	\overline{READY} Hold Time		4	4		ns
21	D15–D0 Read Data Setup Time		4	9		ns
22	D15–D0 Read Data Hold Time		4	6		ns
23	HOLD Setup Time		4	26		ns
24	HOLD Hold Time		4	5		ns
25	RESET Setup Time		7	13		ns
26	RESET Hold Time		7	4		ns
27	NMI, INTR Setup Time	(Note 2)	4	16		ns
28	NMI, INTR Hold Time	(Note 2)	4	16		ns
29	\overline{PEREQ} , \overline{ERROR} , \overline{BUSY} , \overline{FLT}^* Setup Time	(Note 2)	4	16		ns
30	\overline{PEREQ} , \overline{ERROR} , \overline{BUSY} , \overline{FLT}^* Hold Time	(Note 2)	4	5		ns

Notes: *Float feature will be available in future revisions.

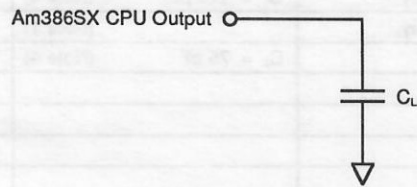
**Contact AMD for 16 MHz availability.

1. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not 100% tested.
2. These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.
3. These are not tested. They are guaranteed by design characterization.
4. Tested with C_L set at 50 pF and derated to support the indicated distributed capacitive load. See Figures 8–10 for the capacitive derating curve.



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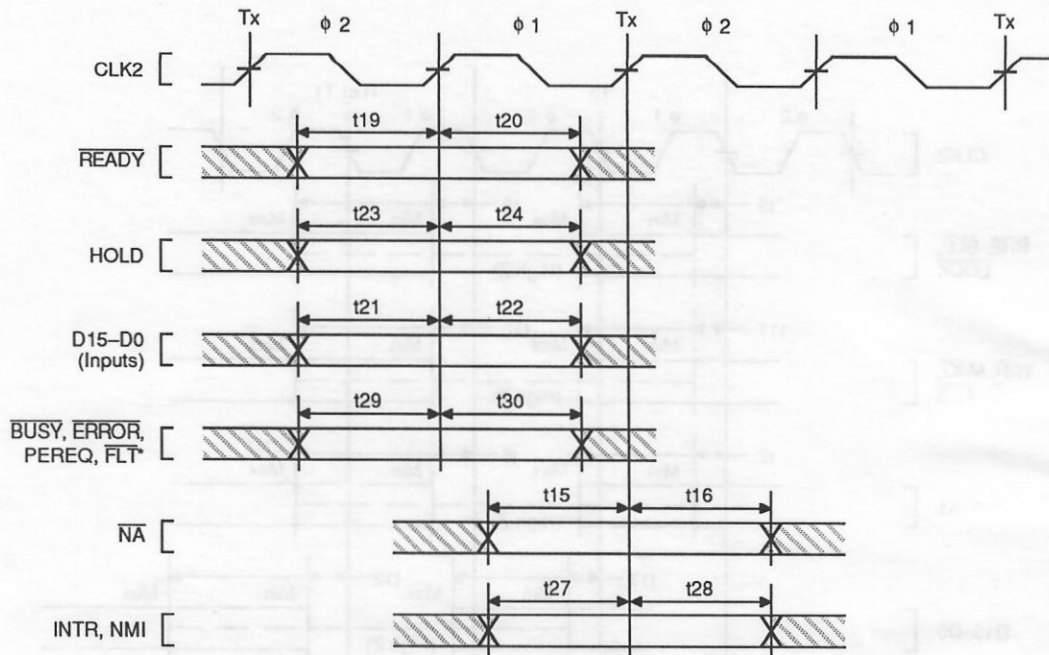
Figure 2. AC Test Waveform



15022B-032

Figure 3. AC Test Circuit

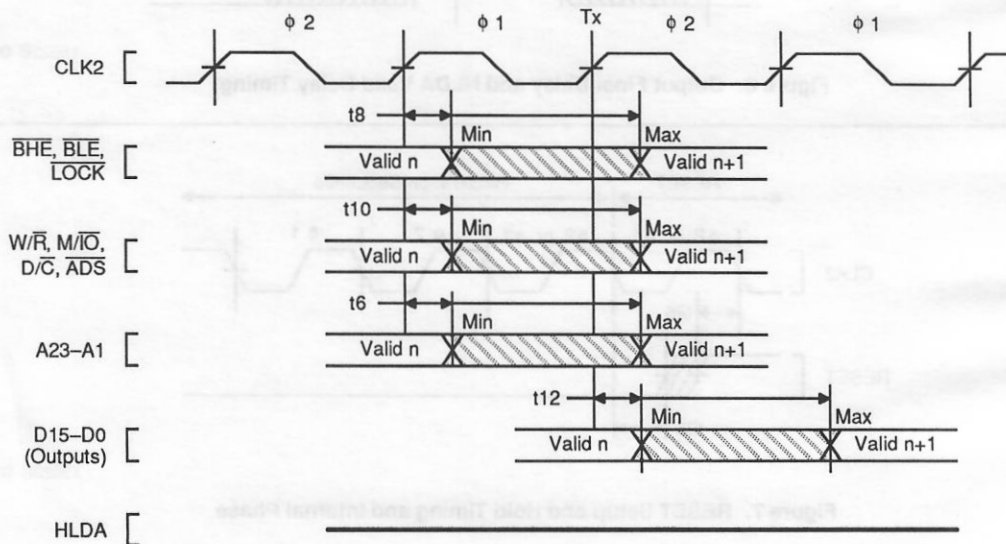
SWITCHING WAVEFORMS



*Float feature will be available in future revisions.

15022B-033

Figure 4. Input Setup and Hold Timing

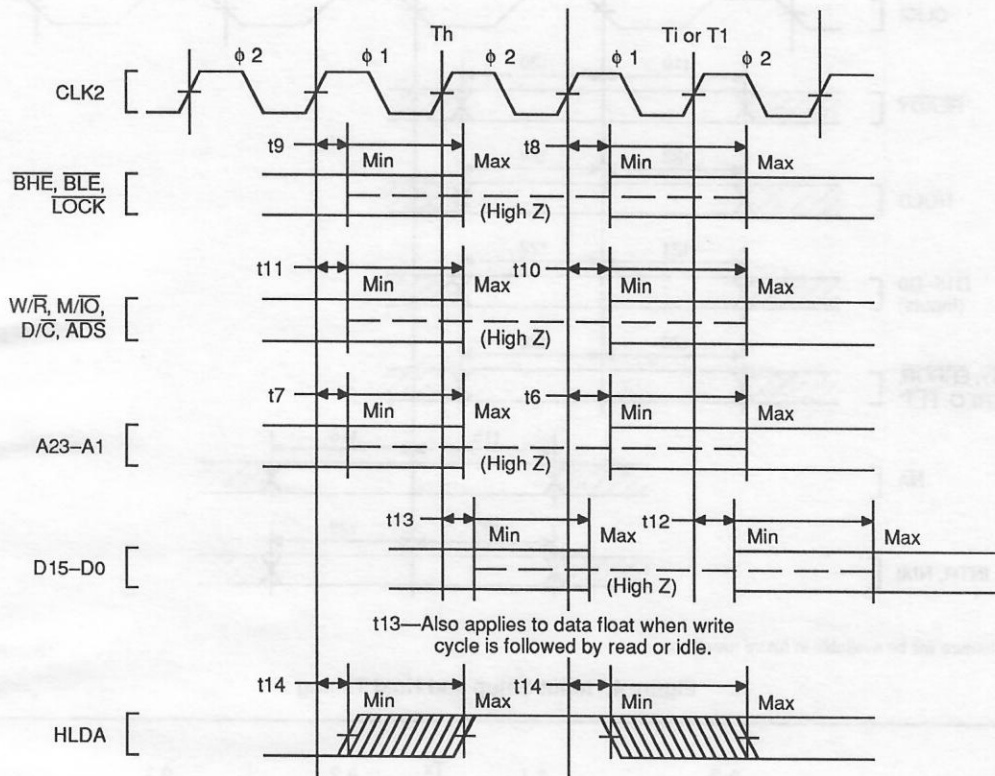


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Figure 5. Output Valid Delay Timing

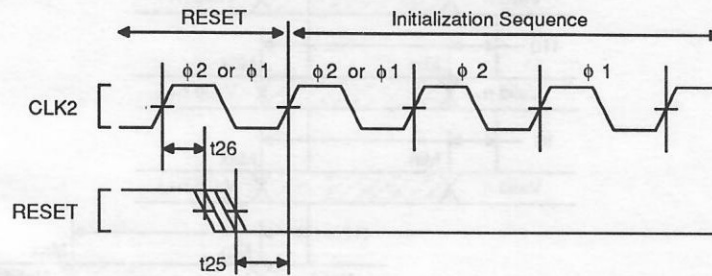


SWITCHING WAVEFORMS (continued)



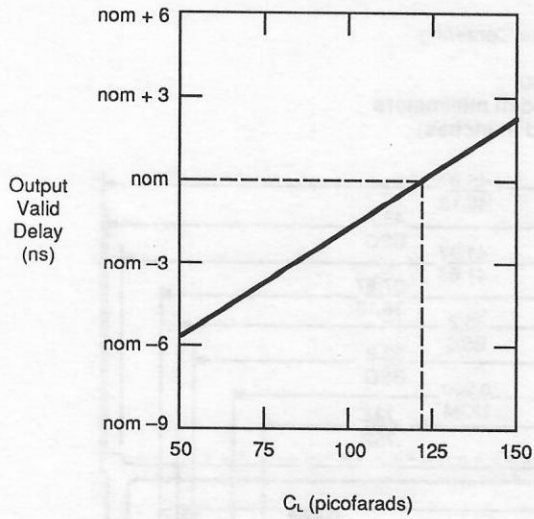
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Figure 6. Output Float Delay and HLDA Valid Delay Timing



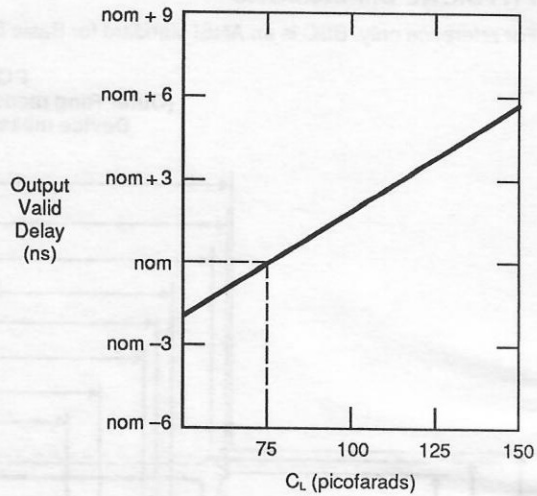
15022B-036

Figure 7. RESET Setup and Hold Timing and Internal Phase



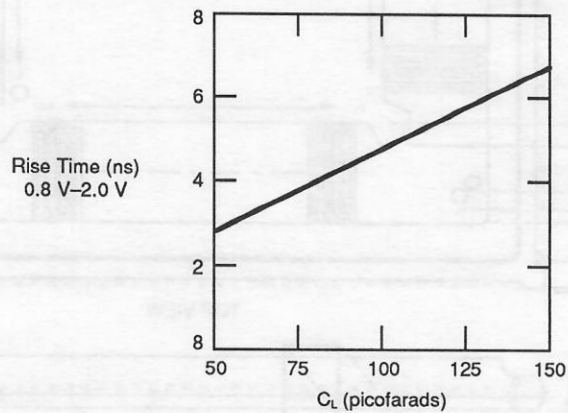
15022B-037

Figure 8. Typical Output Valid Delay Versus Load Capacitance at Maximum Operating Temperature ($C_L = 120$ pF)



15022B-038

Figure 9. Typical Output Valid Delay Versus Load Capacitance at Maximum Operating Temperature ($C_L = 75$ pF)



15022B-039

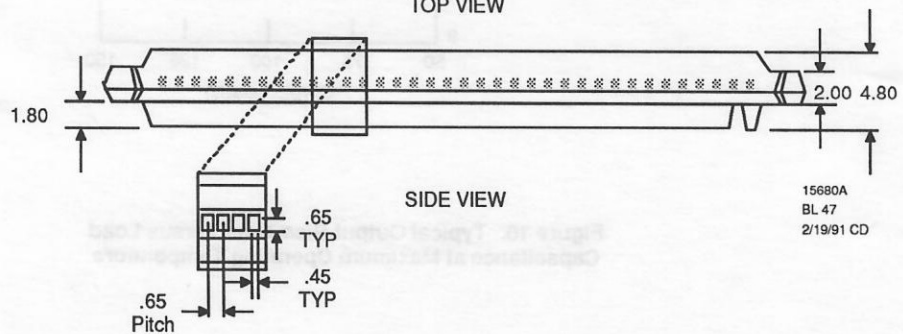
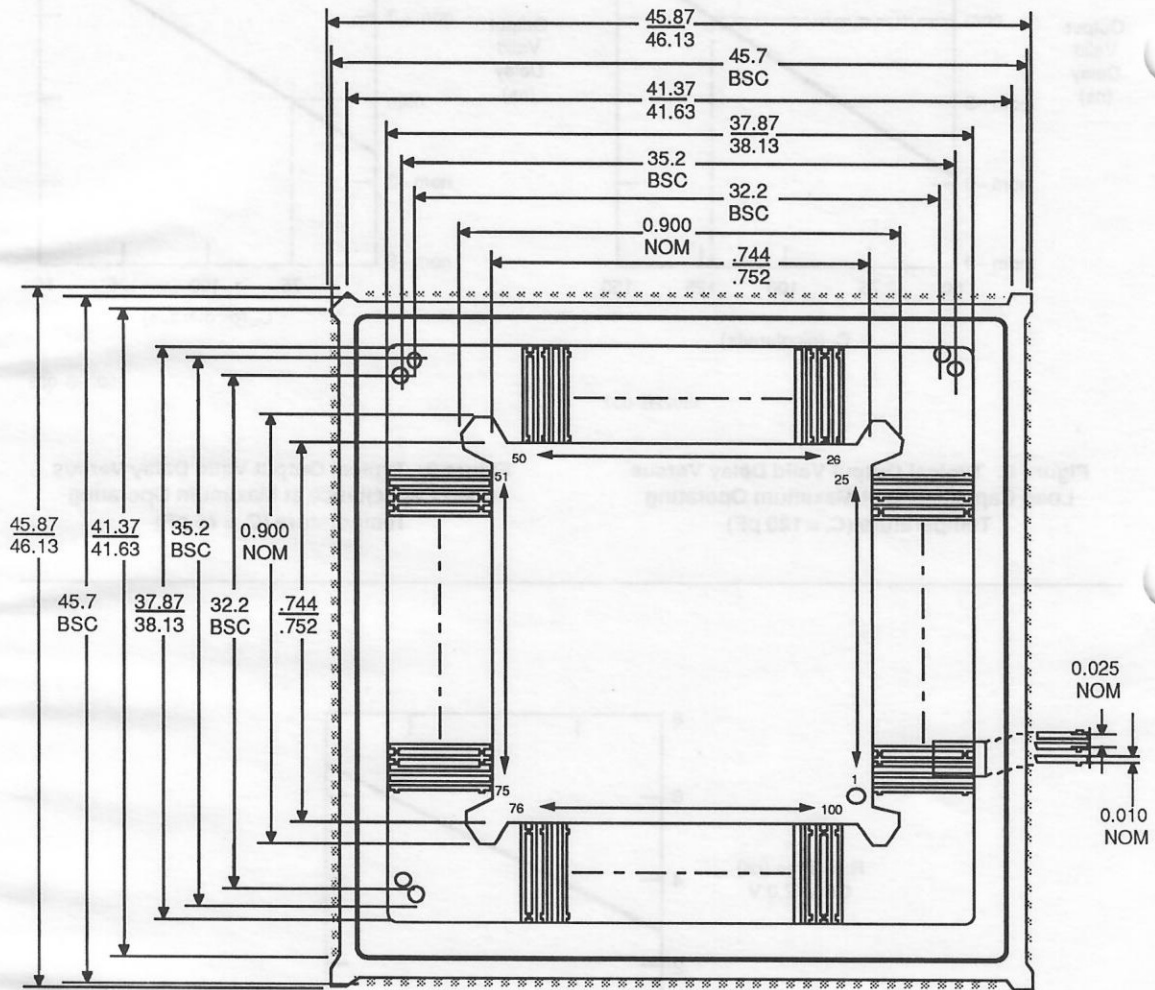
Figure 10. Typical Output Rise Time Versus Load Capacitance at Maximum Operating Temperature



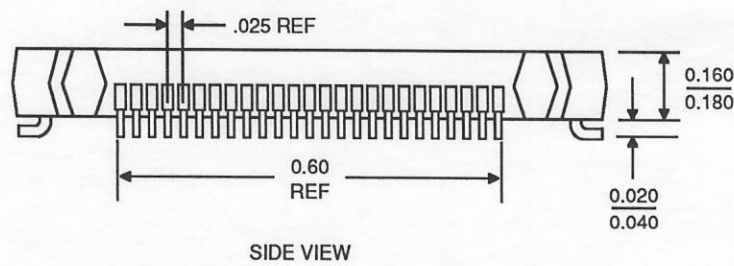
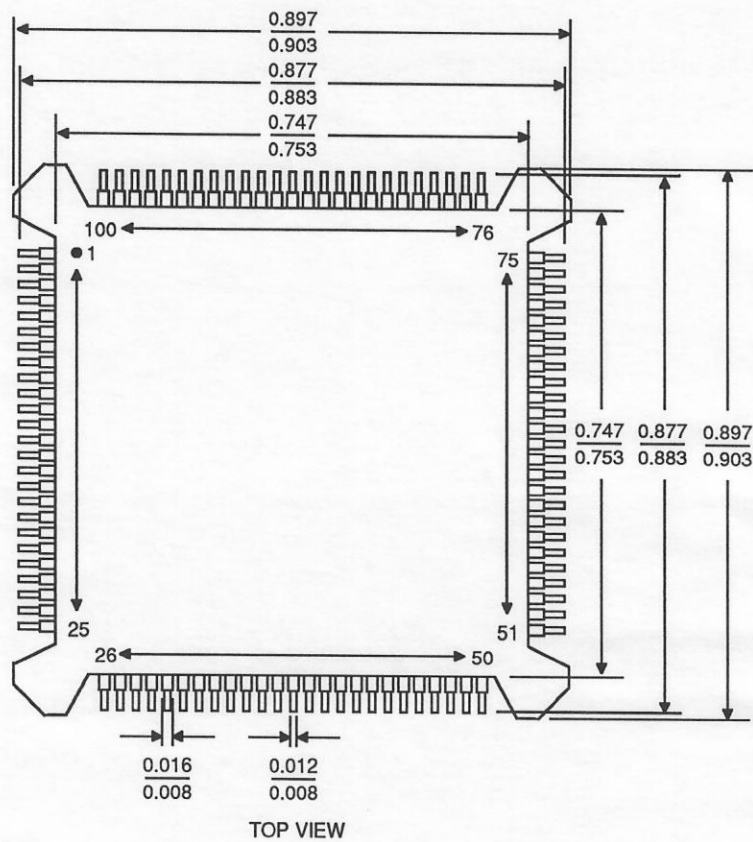
PHYSICAL DIMENSIONS

For reference only. BSC is an ANSI standard for Basic Space Centering.

PQB100
(Outer Ring measured in millimeters
Device measured in inches)



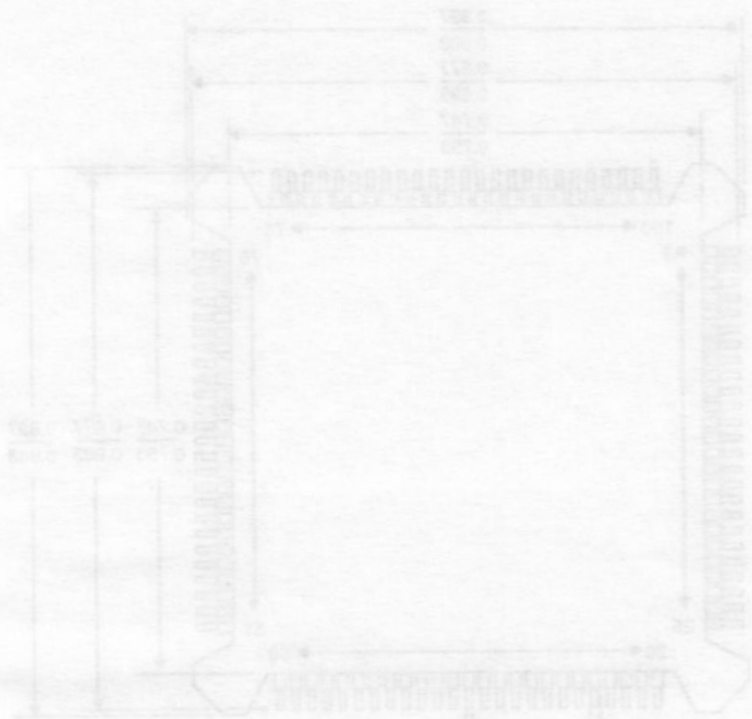
PQ100
(measured in inches)



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FIGURE 1
(continued on next page)



VIEW 1



VIEW 2

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